TF-331-AC / TF-331-ACL
Web Server Controller
Datasheet

DS_TF-331_001R014
Version: 2.08
2010/11/16

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Revision History

Revision	Date	Change Description
DS_TF-331_001R001	2004/6/10	Preliminary
DS_TF-331_001R002	2004/6/18	Preliminary
DS_TF-331_001R003	2004/6/24	Preliminary
DS_TF-331_001R004	2004/7/5	Preliminary
DS_TF-331_001R005	2004/10/28	Add power consumption and reset timing chart Modify the DC characteristic
DS_TF-331_001R006	2004/11/29	Modify the DC characteristic Modify to A2
DS_TF-331_001R007	2005/5/18	Add Lead-Free SoC
DS_TF-331_001R008	2006/3/16	Add RoHS
DS_TF-331_001R009	2006/4/17	Modify power consumption
DS_TF-331_001R010	2006/8/21	Modify ambient temperature
DS_TF-331_001R011	2009/5/21	Add power-on VS reset timing
DS_TF-331_001R012	2009/6/16	Remote internal 64KB ROM for TCP/IP protocol stack
DS_TF-331_001R013	2010/11/11	Add thermal information
DS_TF-331_001R014	2010/11/16	Add Junction Temperature, update Theta jc data

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CONTENTS

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1. Introduction

The TF-331 Web Server Controller provides a very low cost, high performance SoC solution for consumer, networking and industrial device manufacturers that require remote monitoring, control and management through the LAN or Internet using a Web browser via broadband or dial-up network.

The TF-331 includes two UARTs, (one supports high speed, up to 1Mbps), a 10/100M Ethernet MAC and five GPIO ports to connect different devices. The performance of the TF-331 is further improved with the use of hardware Protocol Accelerators and flexible DMA engines.

The hardware Protocol Accelerator in the TF-331 accelerates the handling of TCP, IP, UDP and ICMP protocols. Nine DMA channels are used for data transfer, no CPU intervention is required to serve these functions. The pipelined RISC CPU in the TF-331 is used for handling high-level protocol layer applications. Up to 4MB of SRAM and Flash memory can be addressed by the TF-331.

The HTTP server software and most applications can be run using the embedded 24KB of SRAM without adding any external memory.

The high speed UART interface can be used for connecting to devices such as Bluetooth or modem. The built-in 10/100Mbps Ethernet MAC on the TF-331 allows easy connection to the LAN. When connected to the LAN, the external flash write access capability can be used for online firmware update.

With the bundled HTTP Server software and the low memory requirements, the TF-331 is the most cost effective solution for implementing an embedded web server design.

Taifatech has already launched all products which complie with RoHS for protection of global environment. The marking for RoHS is different from a Non RoHS Product. The Non RoHS TF-331 has a packet designator of “AC” and the RoHS TF-331 has a packet designator of “ACL”. It is simply added a “L” to the old marking.

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1.1. Features

1) MCU:

- 8 bit pipelined RISC TF-390 core, up to 60MHz operating frequency
- Software compatible with standard 8051 and 80390
- Support 64K byte addressing space in **large** mode (8051 mode), up to 4M bytes with GPIO P4 used as address bus in **flat** mode (80390 mode, no banking is needed)
- 1-cycle per instruction
- Five 8-bit GPIO (P1, P3, P4, P5, P6) ports
- GPIO drive high before turning off the output buffer
- Dedicated 16/22 bit address and 8-bit data bus for external program, data memory
- Supports 16 bit IO for accessing 16 bits external IO device, Big Endian or Little Endian selectable

2) Embedded 24K bytes SRAM for packet buffer and MCU data memory

- Adjustable 4K~24K bytes for Ethernet packet buffer.
- Selectable 0K/4K/8K/16K bytes for zero-wait state program mirror (memory) execution.

3) Embedded 64K bytes ROM for production burn in test

4) Supports external flash write access for on-line firmware update

5) External flash and external SRAM swap for code update

6) Supports 9 DMA channels, one active at a time, up to 32K bytes each DMA session

- Internal memory to internal memory DMA

- Internal memory to IO DMA (8/16 bits)
- IO to internal memory DMA (8/16 bits)
- External flash to internal memory DMA
- External memory to internal memory DMA
- Internal memory to external memory DMA
- External memory to external memory DMA
- External memory to IO DMA
- IO to external memory DMA

7) Supports 256-byte / AUTO (4K-bytes) linear access window for fast access to ring buffer packet data, internal data for fast array and data structure access, packet parsing

8) Supports 5 transmit descriptors, four for MAC, one for modem (4 bytes each)

9) One built-in 10/100Mbps MAC

- Selectable MII or Reverse MII interface
- 802.3x flow control for full duplex mode and Jamming flow control for half duplex mode
- Supports H/W FCS check for RX packet and generation for TX packet
- Supports MAC local loop-back for self test.
- MDC/MDIO for external PHY registers access

10) Packet filtering

- RX packet with MY MAC only
- RX BPDU packet
- RX packet with MY IP only
- RX all packet
- RX packet with L4 protocol other then TCP, UDP, and ICMP
- RX IGMP packet
- RX L2 packet
- RX IPv6 packet
- Two additional MAC & three additional IP addresses for special usage

11) Built-in Internet Protocol Accelerator

12) Supports BIST for production internal memory test

- Status bit indicates the test result (fail or success)

13) Supports WDT for H/W and S/W fatal error protection

14) Software compatibility with TF-320.

15) Additional high speed (up to 1Mbps) UART interface, for application like Bluetooth module with auto hardware modem interface support

16) Power saving mode

17) Customer IDs support

18) 0.25 um CMOS technology, 2.5V internal operation, 3.3V IOs

19) Package type: LQFP-100pin

20) TF-331-ACL) complies with RoHS.

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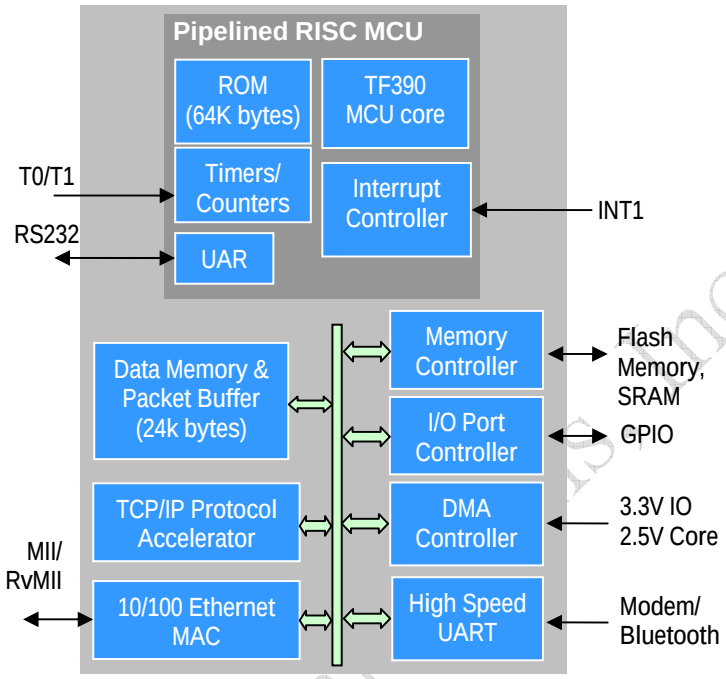
2. Block Diagram



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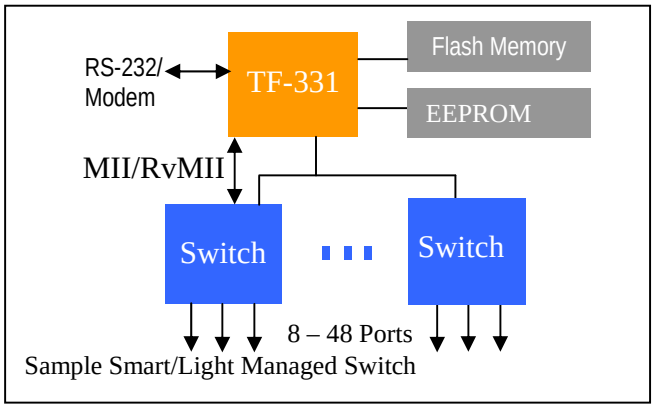
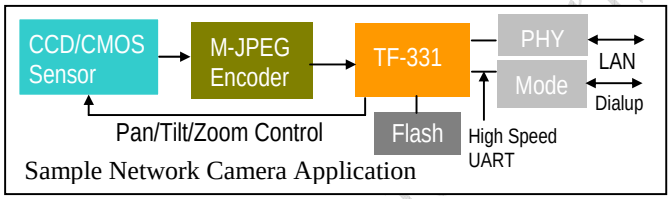
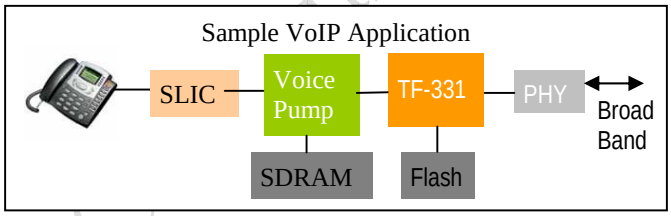
3. System Block Diagrams







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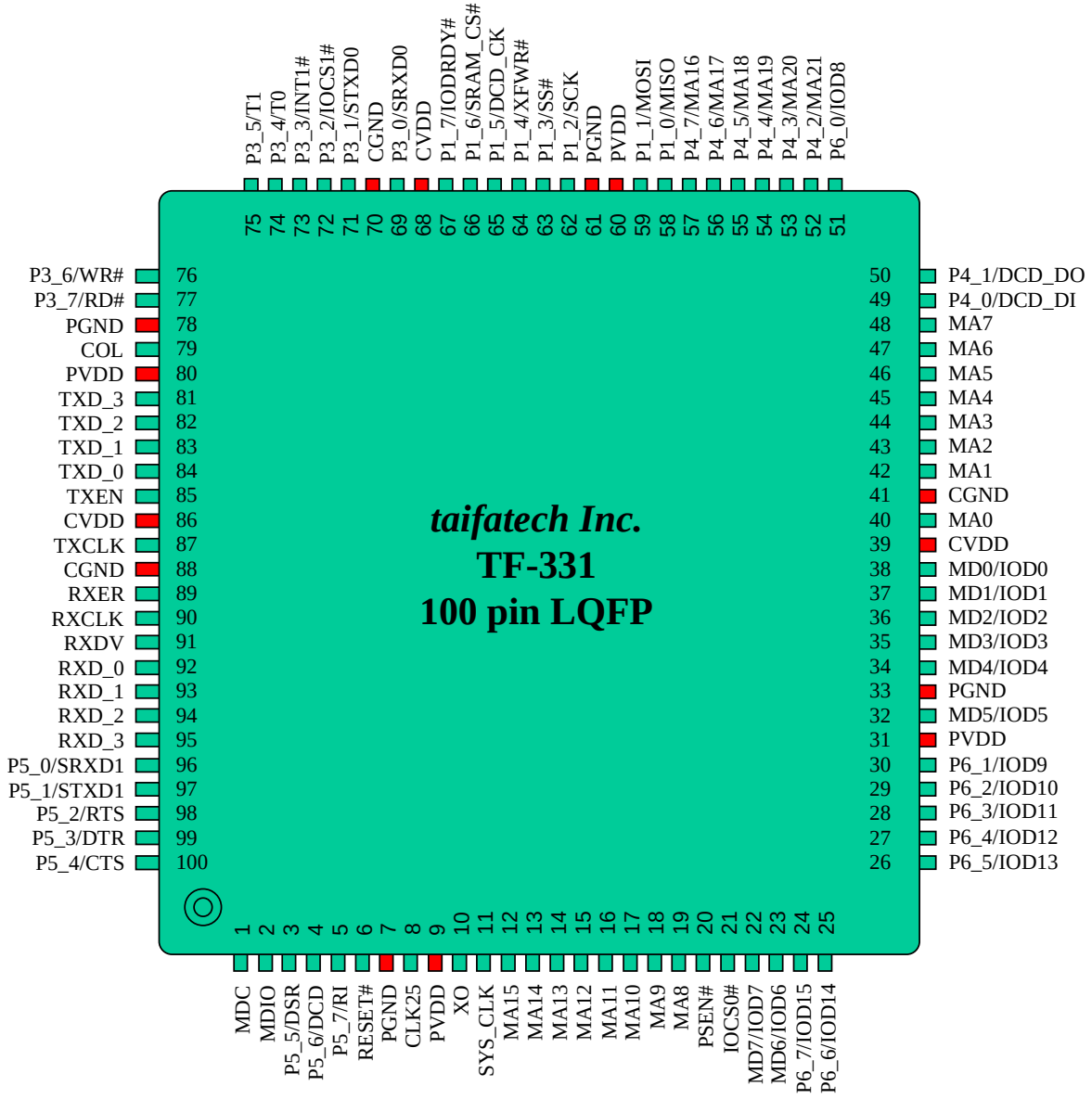
4. Pin Description



4.1 Memory/Peripheral Interface

Pin Name	No.	Type	Description
P3.7 / RD# **P3.6 / WR#** **P3.5 / T1** **P3.4 / T0** **P3.3 / INT1#** **P3.2 / IOCS1#** **P3.1 / STXD0** **P3.0 / SRXD0**	77 76 75 74 73 72 71 69	IU/OD	Port 3. 8-bit bi-directional I/O port. Alternate function: **RD#** :External Data Memory/external IO DMA read strobe output **WR#** :External Data Memory/external IO DMA write strobe output **T1** :Timer 1 external input **T0** :Timer 0 external input **INT1#** :External Interrupt input 1 **IOCS1#** :Extended IO chip select output **STXD0** :Serial Port Transmit output **SRXD0** :Serial Port Receive input
P1.7 / IODRDY# **P1.6 / SRAM_CS#** **P1.5 / DCD_CK** **P1.4 / XFWR#** **P1.3 / SS#** **P1.2 / SCK** **P1.1 / MOSI** **P1.0 / MISO**	67 66 65 64 63 62 59 58	IU/OD	Port 1. 8-bit bi-directional I/O port. Alternate function: **IODRDY#** : IO DMA ready input **SRAM_CS#** : External SRAM chip select **XFWR#** : External flash write strobe output **DCD_CK** : TF390 debugger clock output port <**SPI function**> : **SS#** : H/W SPI Chip Select output **SCK** : H/W SPI Clock output **MOSI** : H/W SPI Master Out Slave In output **MISO** : H/W SPI Master In Slave Out input
P4.7 / MA16 **P4.6 / MA17** **P4.5 / MA18** **P4.4 / MA19** **P4.3 / MA20** **P4.2 / MA21** **P4.1 / DCD_DO** **P4.0 / DCD_DI**	57 56 55 54 53 52 50 49	IU/OD	Port 4. 8-bit bi-directional I/O port. Alternate function: **MA[21:16]:** Extended external flash/ROM address bus **DCD_DO** : TF390 debugger data output port **DCD_DI** : TF390 debugger data input port
P5.7 / RI **P5.6 / DCD** **P5.5 / DSR** **P5.4 / CTS** **P5.3 / DTR** **P5.2 / RTS** **P5.1 / STXD1** **P5.0 / SRXD1**	5 4 3 100 99 98 97 96	IU/OD	Port 5. 8-bit bi-directional I/O port. Alternate function(Modem interface): **RI** : Ring indicator input **DCD** : Data carrier detect input **DSR** : Data set ready input **CTS** : Clear to send input **DTR** : Data terminal ready output **RTS** : Request to send output **STXD1** : Serial data output / High speed UART TXD **SRXD1** : Serial data input / High speed UART RXD

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P6.7 / IOD15 **P6.6 / IOD14** **P6.5 / IOD13** **P6.4 / IOD12** **P6.3 / IOD11** **P6.2 / IOD10** **P6.1 / IOD9** **P6.0 / IOD8**	24 25 26 27 28 29 30 51	IU/OD	Port 6. 8-bit bi-directional I/O port. Alternate function: **IO DMA** / **16-bit IO** data bus IOD[15:8] in 16-bit IO mode
PSEN#	20	O	**Program Store Enable Output**. This signal is commonly connected to optional external program memory as a chip enable. PSEN# provides an active low pulse and is driven high when external program memory is not being accessed.
MD[7:0] /IOD[7:0]	22, 23, 32, 34, 35, 36, 37, 38	I/O	Data bus. Alternate function: **16-bit IO/IO DMA** data bus IOD[7:0]
MA [7:0]	48, 47, 46, 45, 44, 43, 42, 40	I/O	External flash/ROM address bus. Alternate function(Power On strapped pin, internal pull high): **MA[0] :** External flash enable selection 1: Enables external Flash 0: Disables external Flash **MA[1] :** MII or Reverse MII selection. 1: MII interface 0: Reverse MII (RvMII) interface **MA[5] :** DOCD debugger port skip 1: Skips DOCO debugger port 0: Enables DOCD debugger port **MA[6] :** TF390 MA[21:16] control 1: P4.2 ~ P4.7 normal usage 0: P4.2 ~ P4.7 change to MA[21:16] **MA[7] :** TF390 MA[21:16] control 1: normal address 0: MA[21:16] = MA[21:16] -1 for shifting external flash 64Kbytes.
MA[15:8]	12, 13, 14, 15, 16, 17, 18, 19,	O	External flash/ROM address bus.
IOCS0#	21	O	**Extended IO chip select output**. Active low. Assert this signal together with RD# or WR# when external devices are accessed.

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4.2 MII/ RvMII Interface

Pin Name	No.	Type	Description
TXD [3:0]/ **RvRXD [3:0]**	81, 82, 83, 84	O	**MII Transmit Data.** TF-331 sources TXD [3:0] synchronous with TXCLK when TXEN is asserted. TXD[3:1] are also used for power on setting. **Reverse MII Receive Data**. TF-331 sources RvRXD [3:0] synchronous with **RvRXCLK** when **RvRXDV** is asserted.
TXCLK/ **RvRXCLK**	87	I/O	**MII Transmit Clock.** Continuous (25MHz/2.5MHz) clock input used to synchronize TXEN and TXD [3:0]. **Reverse MII Receive Clock**. Continuous (25MHz/2.5MHz) clock output used to synchronize **RvRXDV** and RvRXD [3:0].
TXEN/ **RvRXDV**	85	O	**MII Transmit Enable.** Indicates TF-331 has presented valid data on the TXD [3:0]. **Reverse MII Receive Data Valid**. Indicates TF-331 has presented valid data on the RvRXD [3:0].
RXD [3:0]/ **RvTXD [3:0]**	95, 94, 93, 92	I	**MII Receive Data.** External device (PHY) will source RXD [3:0] synchronous with RXCLK when RXDV is asserted. **Reverse MII Transmit Data**. External device (MAC) will source RvTXD [3:0] synchronous with **RvTXCLK** when **RvTXEN** is asserted.
RXCLK/ **RvTXCLK**	90	I/O	**MII Receive Clock (input).** Continuous (25MHz/2.5MHz) clock input used by MAC to synchronize RXDV, RXD [3:0] and RXER. **Reverse MII Transmit Clock (output)**.
RXDV/ **RvTXEN**	91	I	**MII Receive Data Valid (input).** While RXDV is asserted, it means the external PHY has presented valid recovered data on the RXD [3:0]. **Reverse MII Transmit Enable (input)**.
RXER/ **RvRXER**	89	I/O	**MII Receive Error.** Indicates external PHY has received invalid symbol data. **Reverse MII Receive Error**.
COL/ **RvCOL**	79	I/O	**MII Collision Detection (input).** Active when collision is detected. **Reverse MII Collision Detection (output)**.
MDC	1	O	**Management Data Clock.**
MDIO	2	I/O	**Management Data I/O.**

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4.3 Miscellaneous

Pin Name	No.	Type	Description
RESET#	6	IS	**System Reset input**. Active low
CLK25	8	O	**25MHz clock output**.
SYS_CLK	11	I	**SYS_CLK** and **XO** provide support for fundamental mode parallel resonant, AT cut crystals. XI also acts as an input if there is an external clock source, 50MHz in place of a crystal.
XO	10	O	
P-VDD	9, 31, 60, 80	3.3V IO power	
C-VDD	39, 68, 86	2.5V Core power	
P-GND **C-GND**	7, 33, 41, 61 70, 78, 88	Ground	
Note: # =active low signal; ID=input with internal pull-down; IU=input with internal pull-up; OD=open drain output; IS=input with Schmitt Trigger; NA=Not available			

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5. Electric Characteristics

5.1 Thermal Data

Item		Rating	Unit
Theta ja	0 m/s	57.9	℃/W
	1 m/s	50.7	℃/W
	2 m/s	48.6	℃/W
Psi jt		10.0	℃/W
Theta jc		31.96	℃/W

5.2 Absolute Maximum Ratings

(GND=0V)

Item	Symbol	Conditions	Rating	Unit
Ambient Temperature	T_A		0 ℃ to 70 ℃	℃
Junction Temperature	Tj	Power = 1W	81.99 ℃	℃
Case Temperature	Tc		41.37 ℃ to 82.01 ℃	℃
Storage Temperature	T_{STG}		-40 ℃ to 125 ℃	℃
Input Voltage	V_I		-0.3 to V_{DD}+0.5	V

5.3 DC Characteristics

(VDD=3.0V to 3.6V, Ta=-0℃ to +70℃)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
3.3V Power Supply	P-VDD		3.0	-	3.6	V
2.5V Power Supply	C-VDD		2.25	-	2.75	V
Input Low Voltage	V_{IL}		-	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2, 4, 8, 16, 24mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -2, -4, -8, -16, -24mA	2.4	-	-	V
Input Low Leakage Current	I_{LIL}	Input voltage = 0V	-10	-	10	uA
Input High Leakage Current	I_{LIH}	Input voltage = 3.6V	-	-	10	uA
Input Pin Capacitance	C_I	f=1MHz, V_{DD}=0V	-	-	10	pF
Output Pin Capacitance	C_O	f=1MHz, V_{DD}=0V	-	-	10	pF
Input/Output Pin Capacitance	C_{IO}	f=1MHz, V_{DD}=0V	-	-	10	pF
3.3V Active Current	$I_{DD3.3}$	f=50MHz (off load)	-	-	70	mA
2.5V Active Current	$I_{DD2.5}$	f=50MHz (off load)	-	-	80	mA

※ All input pins are 5V tolerance.

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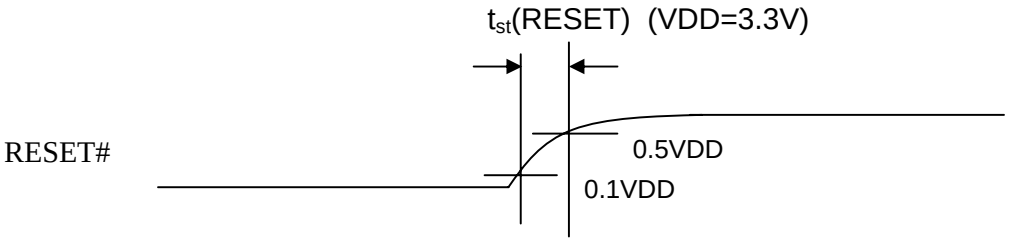
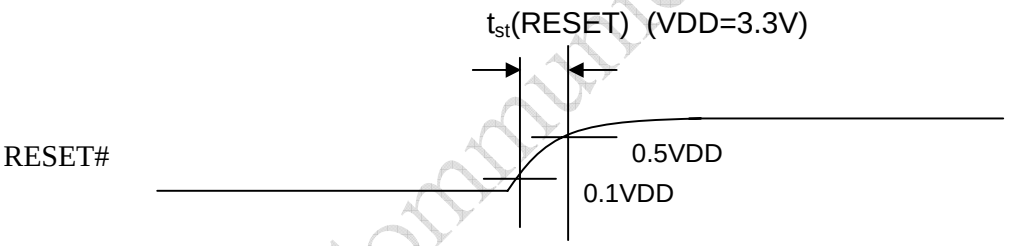
5.4 AC Characteristics Timing Chart

5.4.1 Power Up Timing



Item	Symbol	Min.	Max.	Unit
Power Up Delay time	t_{pd}(RESET)		5	ms

5.4.2 Reset Timing



Item	Symbol	Min.	Max.	Unit
RESET time	t_{st}(RESET)	1		us

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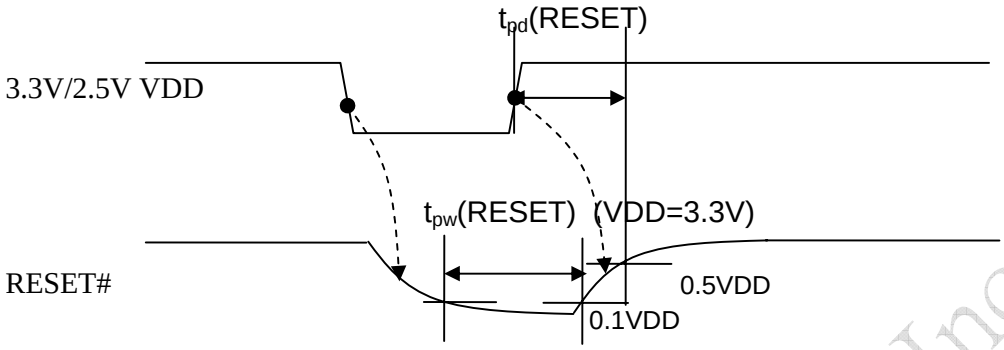
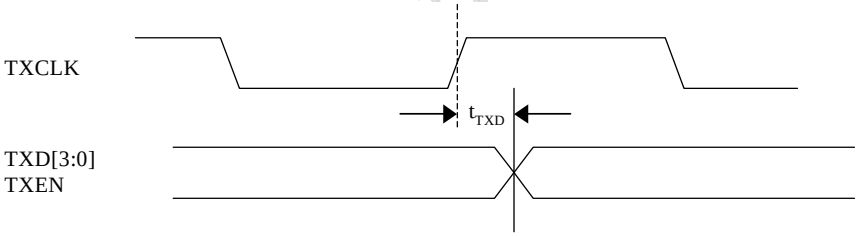
5.4.3 Power to Reset Timing



Item	Symbol	Min.	Max.	Unit
Minimum RESET Width after power down & up	t_{pw}(RESET)	5		us
Minimum Power Up to Reset Delay	t_{pd}(RESET)	3		us

5.4.4 MII Interface



Item	Symbol	Min.	Max.	Unit
MII output data delay time	t_{TXD}		10	ns

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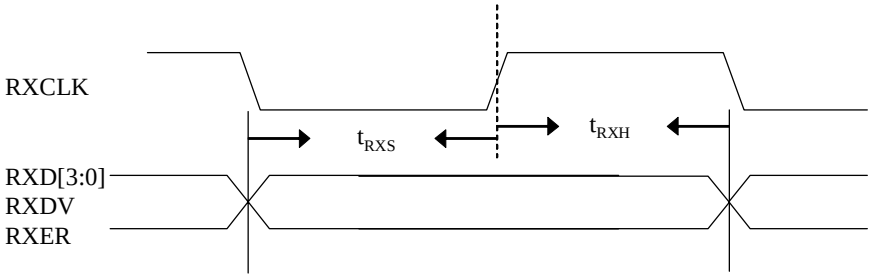

Item	Symbol	Min.	Max.	Unit
MII Input data setup time	t_{RXS}	5		ns
MII Input data hold time	t_{RXH}	2		ns

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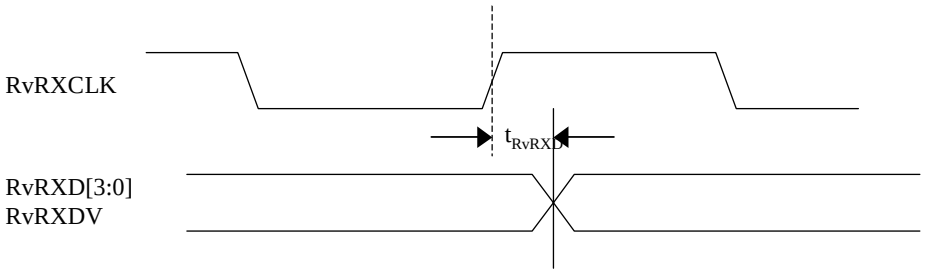
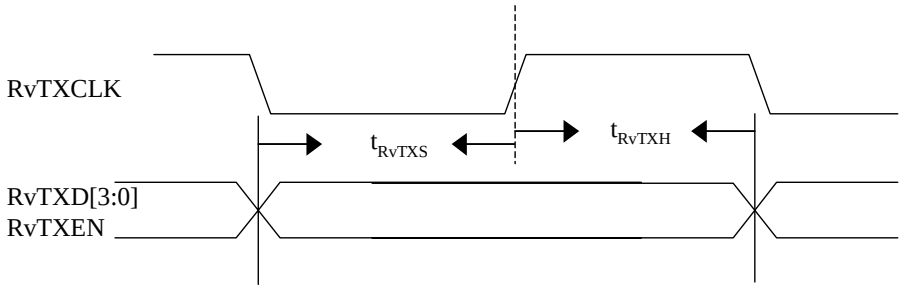
5.4.5 RvMII Interface



Item	Symbol	Min.	Max.	Unit
RvMII Output data (RX*) delay time	t_{RvRXD}	19	22	ns



Item	Symbol	Min.	Max.	Unit
RvMII Input data (TX*) setup time	t_{RvTXS}	10		ns
RvMII Input data (TX*) hold time	t_{RvTXH}	0		ns

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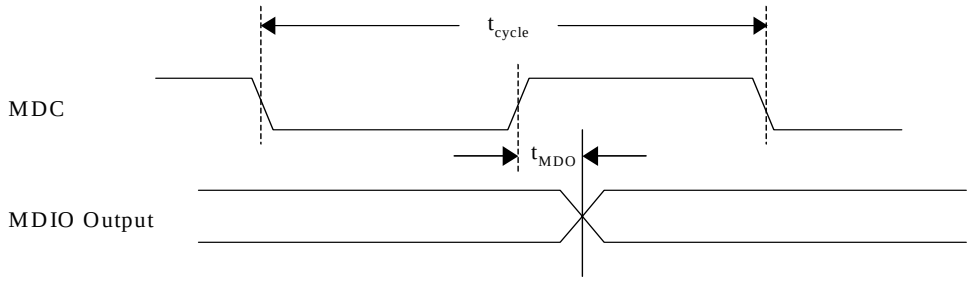
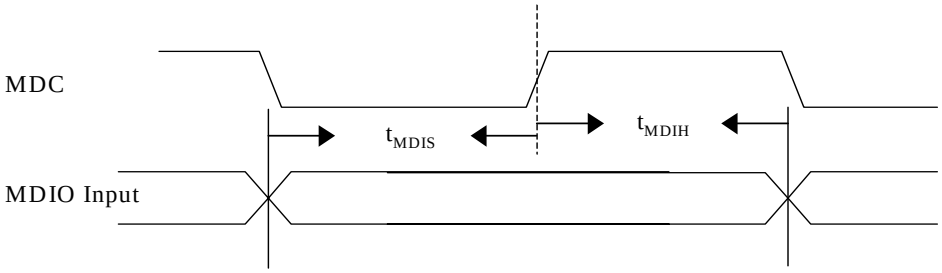
5.4.6 MDC/MDIO Interface



Item	Synbol	Min.	Max.	Unit
MDC/MDIO output data delay time	t_{MDO}	$(t_{cycle}/2)$	$(t_{cycle}/2)+10$	ns

Note: t_{cycle} is the cycle time of the MDC clock, which is configurable



Item	Symbol	Min.	Max.	Unit
MDIO Input data setup time	t_{MDIS}	2		ns
MDIO Input data hold time	t_{MDIH}	0		ns

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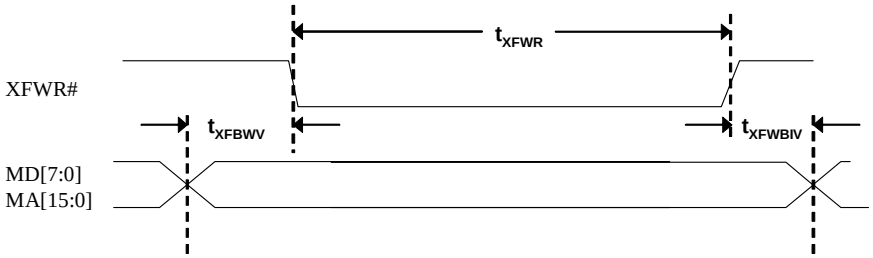
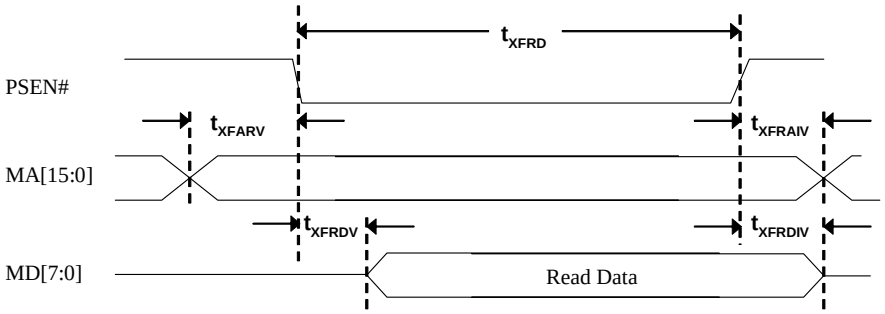
5.4.7 External Flash



Item	Symbol	Min.	Max.	Unit
External Flash Write Assert Width	t_{XFWR}	T+nT	-	ns
Data/Address Bus valid to Write Assert	t_{XFBWV}	4	8	ns
Write de-assert to Data/Address Bus de-assert	t_{XFWBIV}	11	13	ns

Note: **T** is the system clock cycle time.
n is the number of wait states.



Item	Symbol	Min.	Max.	Unit
External Flash Read Assert Width	t_{XFRD}	T+nT	-	ns
Address Bus valid to Read Assert	t_{XFARV}	16	20	ns
Read de-assert to Address Bus de-assert	t_{XFRAIV}	16	20	ns
Read assert to Data Bus assert	t_{XFRDV}	0	2+nT	ns
Read de-assert to Data Bus de-assert	t_{XFRDIV}	0	-	ns

Note:
1. **T** is the system clock cycle time.
2. n is the number of wait states.
3. The value of n depends on the value of t_{XFRDV}, for example, the max t_{XFRDV} is 30, then we should choose wait state 2.

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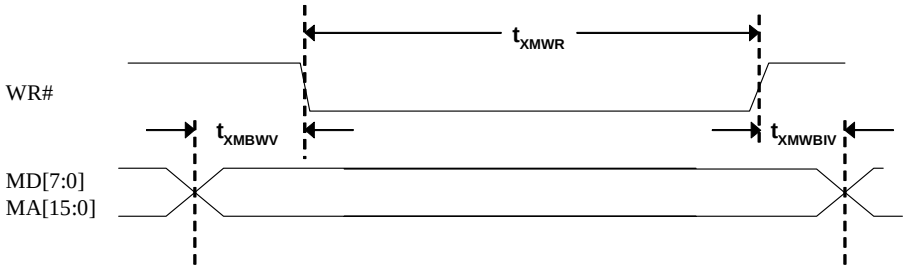
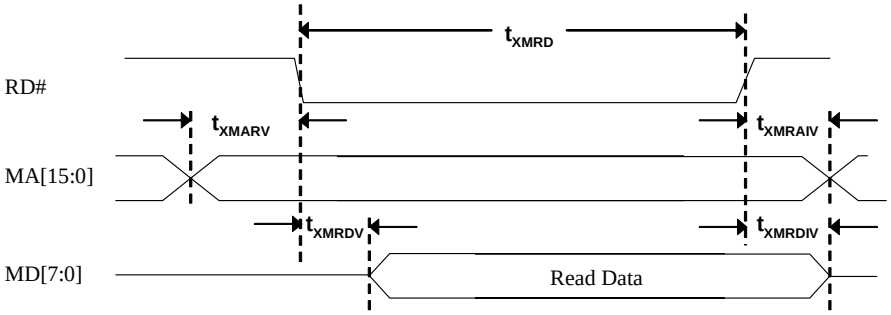
5.4.8 External RAM Interface



Item	Symbol	Min.	Max.	Unit
External Flash Write Assert Width	t_{XMWR}	T+nT	-	ns
Data/Address Bus valid to Write Assert	t_{XMBWV}	4	8	ns
Write de-assert to Data/Address Bus de-assert	t_{XMWBIV}	11	13	ns

Note: **T** is the system clock cycle time.
n is the number of wait states.



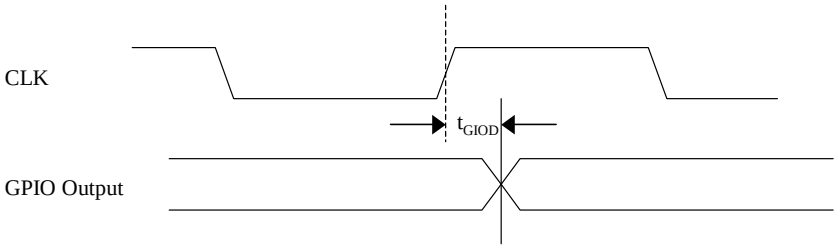
Item	Symbol	Min.	Max.	Unit
External RAM Read Assert Width	t_{XMRD}	T+nT	-	ns
Address Bus valid to XRAM Read Assert	t_{XMARV}	16	26	ns
XRAM Read de-assert to Address Bus de-assert	t_{XMRAIV}	12	18	ns
XRAM Read assert to Data Bus assert	t_{XMRDV}	0	3+nT	ns
XRAM Read de-assert to Data Bus de-assert	t_{XMRDIV}	0	-	ns

Note:
1. **T** is the system clock cycle time.
2. n is the number of wait states.
3. The value of n depends on the value of t_{XFRDV}, for example, the max t_{XFRDV} is 30, then we should choose wait state 2.

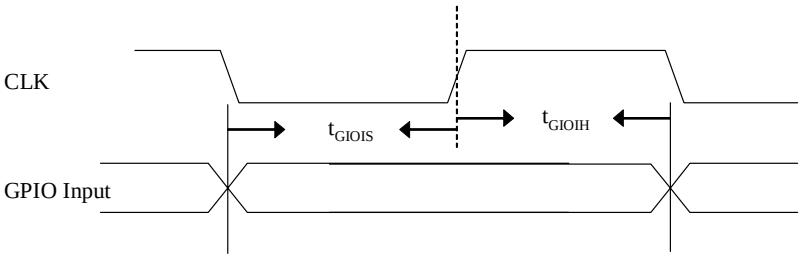
For Customer only

5.4.9 GPIO Interface

Measured conditions: External Pull-up resistor 4.7KΩ
V_{OH} = 2.0V
V_{OL}= 0.4V



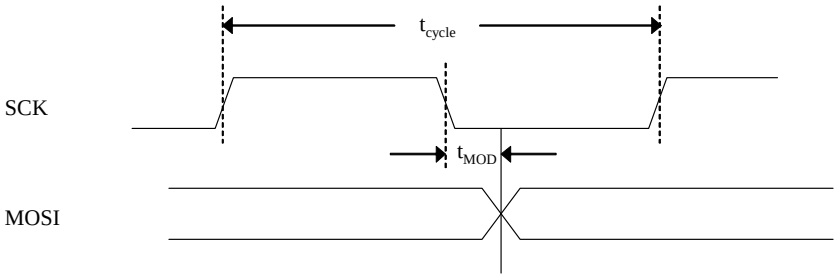
Item	Symbol	Min.	Max.	Unit
GPIO Output High data delay time	t_{GIOD}	30		ns
GPIO Output Low data delay time	t_{GIOD}	3		ns



Item	Symbol	Min.	Max.	Unit
GPIO Input data setup time	t_{GIOIS}	5	15	ns
GPIO Input data hold time	t_{GIOIH}	5	15	ns

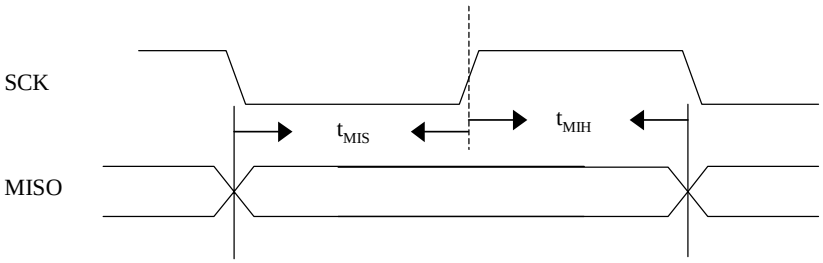
For C ... nc. only

5.4.10 HW SPI Interface



Item	Symbol	Min.	Max.	Note
MOSI output data delay time	t_{MOD}		$(t_{cycle}/2)+5$	

Note: t_{cycle} is the cycle time of the SPI clock, which is configurable

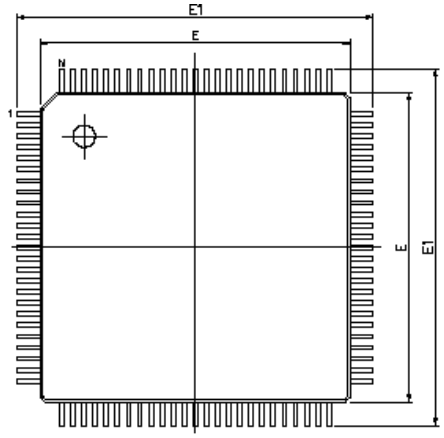


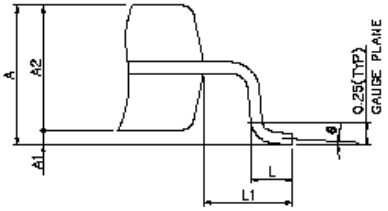
Item	Symbol	Min.	Max.	Note
MISO Input data setup time	t_{MIS}	15		
MISO Input data hold time	t_{MIH}	0		

For Ca... c. only

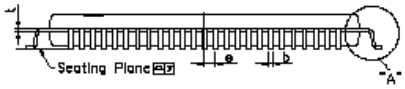
6. Mechanical Dimensions

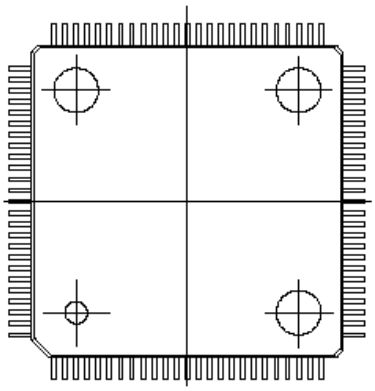
100-Pin LQFP -- Plastic QFP 100pin Body size 14 x 14 x 1.4mm





"A" VIEW





UNIT / SYMBOL	MM(BASE)
A	1.60(MAX)
A1	0.10±0.05
A2	1.40±0.05
E1	16.00±0.10
E	14.00±0.10
L	0.60±0.15
L1	1.00(REF)
t	0.127(TYP)
y	0.076(MAX)
θ	0°~7°

N / SYMBOL	80L
b	0.30±0.08
e	0.65(TYP)

N / SYMBOL	100L
b	0.22±0.05
e	0.50(TYP)

N / SYMBOL	128L
b	0.16±0.05
e	0.40(TYP)

For Ca... Only