Product List

OB59A128A1W80LP,
OB59A128A1W64VP,

Description

The OB59A128A1 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 128KB embedded Flash for program, and executes all ASM51 instructions fully compatible with MCS-51.

OB59A128A1 contains 4KB+256B on-chip RAM, up to 59 GPIOs (80L package), various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.

The high performance of OB59A128A1 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

OB59A128A1ihhkL YWW
i: process identifier { W = 2.2V ~ 5.5V}
hh: pin count
k: package type postfix {as table below }
L:PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y: Year Code
WW: Week Code (01-52)

Postfix	Package
V	LQFP

Features

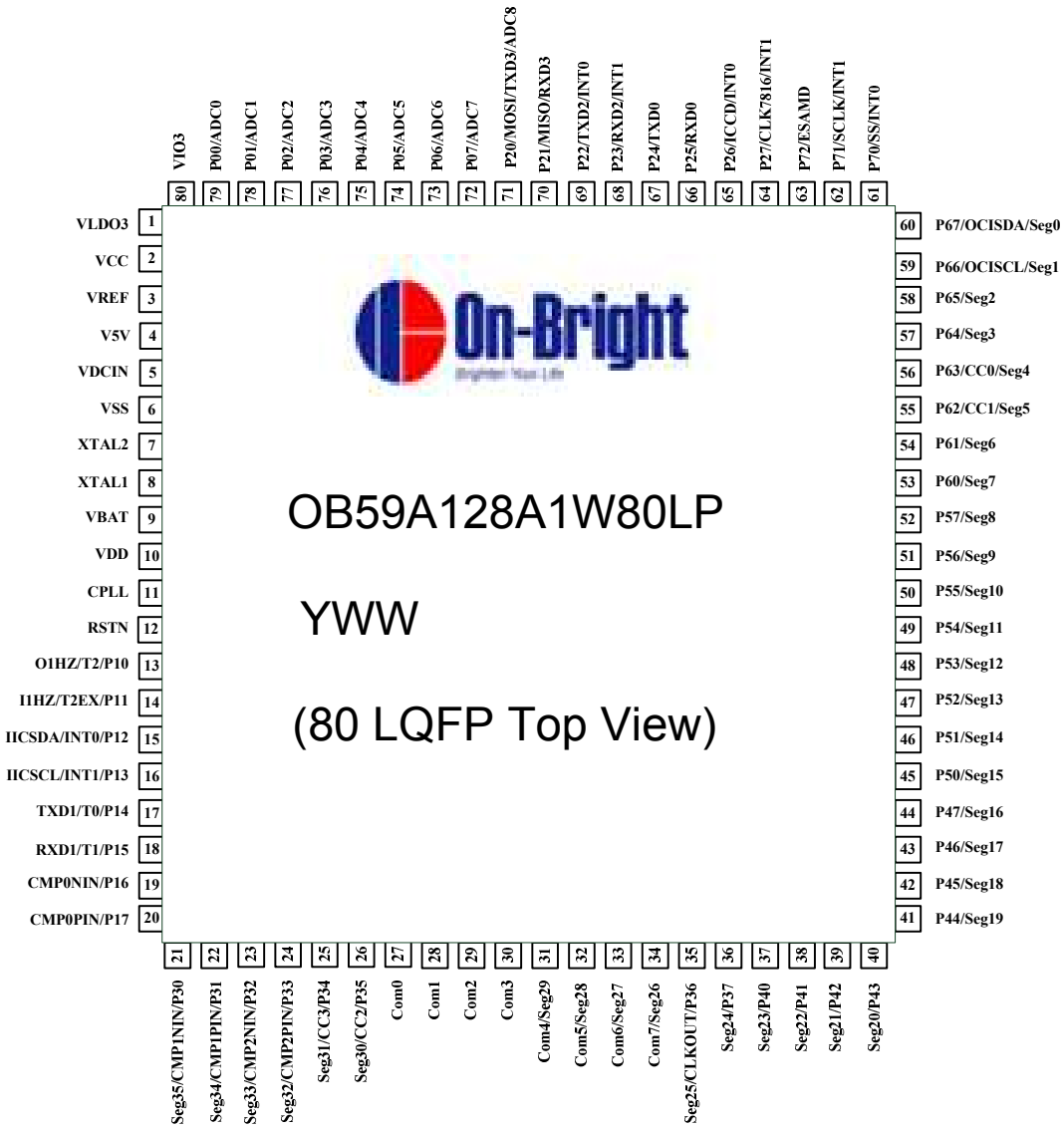
- Main Flash ROM 128KB(127KB for program memory or EEPROM and 1KB for Infomation block) , 1KB/page .
- Working voltage 2.2V~5.5V.
- High speed architecture of 1 clock/machine cycle runs up to 22.1184MHz.
- 256 bytes RAM as standard 8052, plus 4k bytes on-chip expandable SRAM
- Port 0~7,59 GPIO
- Dual 16-bit Data Pointers (DPTR0 & DPTR1).
- Four serial peripheral interfaces in full duplex mode (UART0 ~ UART3)
- Additional Baud Rate Generator for Serial port
- UART transmitter optionally modulated with 38KHz for IR
- Three 16-bit Timer/Counters. (Timer 0,1,2)
- Programmable watchdog timer.
- One IIC interface (Master/Slave mode).
- One SPI interface (Master/Slave mode).
- 3 On-Chip Comparator
- 4-channel 16-bit compare / capture functions.
  - Comparator out can be CCU input source internally.
  - Noise filter with CCU input with sample frequency select.
- 32768Hz low power crystal and high accuracy RTC
- 9.83MHZ system clock from PLL and Internal RC Oscillator.
- ISP/IAP/ICP functions.
- 2-channel ISO7816 interfaces for ESAM and IC Card.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- LVI/LVR (LVR deglitch 500ns).
- 16-bit Sigma-Delta ADC for Temperature sensor and Battery
- 9-channel 12-bit SAR ADC for external pin
- Build-in clock failure detection of 32KHz quartz oscillator
- On-chip Temperature sensor and voltage reference with individual voltage supply level
- On-chip 3.0V low-dropout regulator
- Configurable supply level (V5V/VIO3) for five SPI-related I/O port
- Power management unit for IDLE and power down

modes.

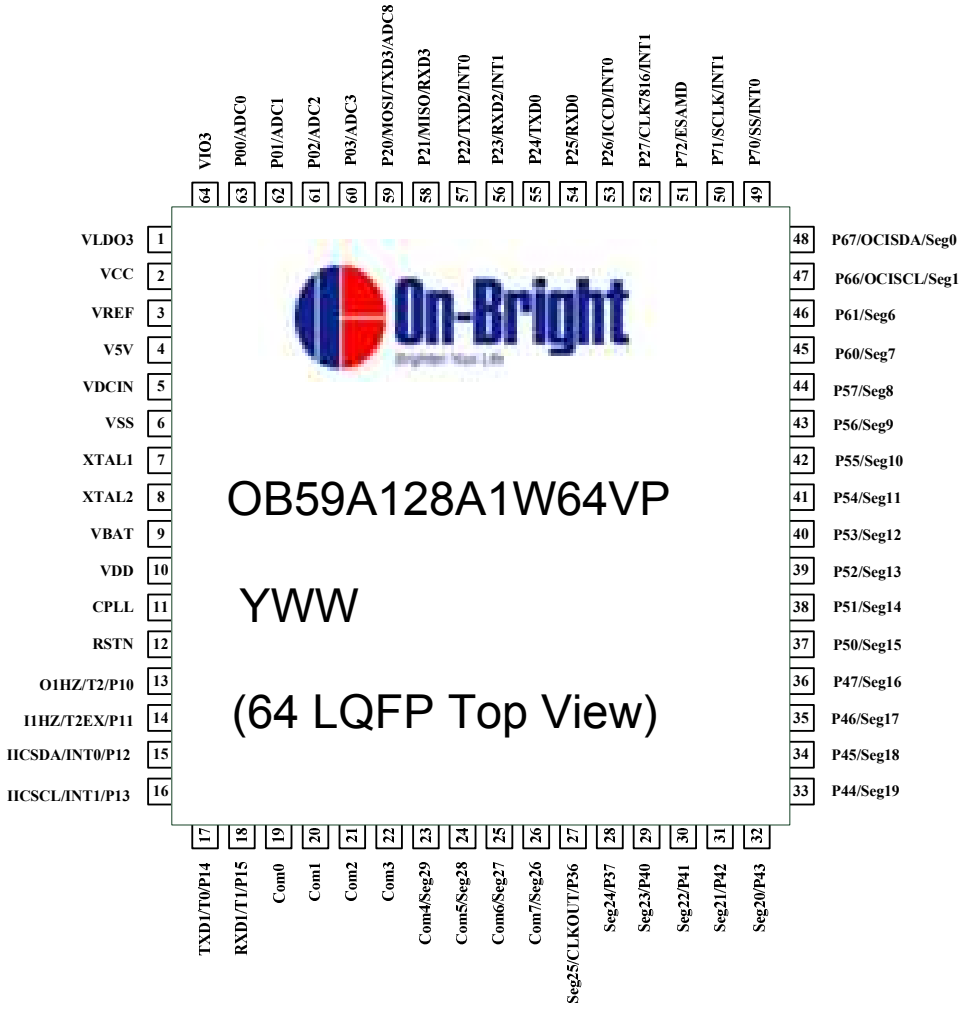
- LCD selectable duty : 1/8, 1/6, 1/4 , 1/3 , 1/2 or full-duty
- LCD maximum SEG-driver 36 pins, COM-driver 8pin
- LCD selectable 1/4, 1/3, 1/2 bias

Pin Configuration

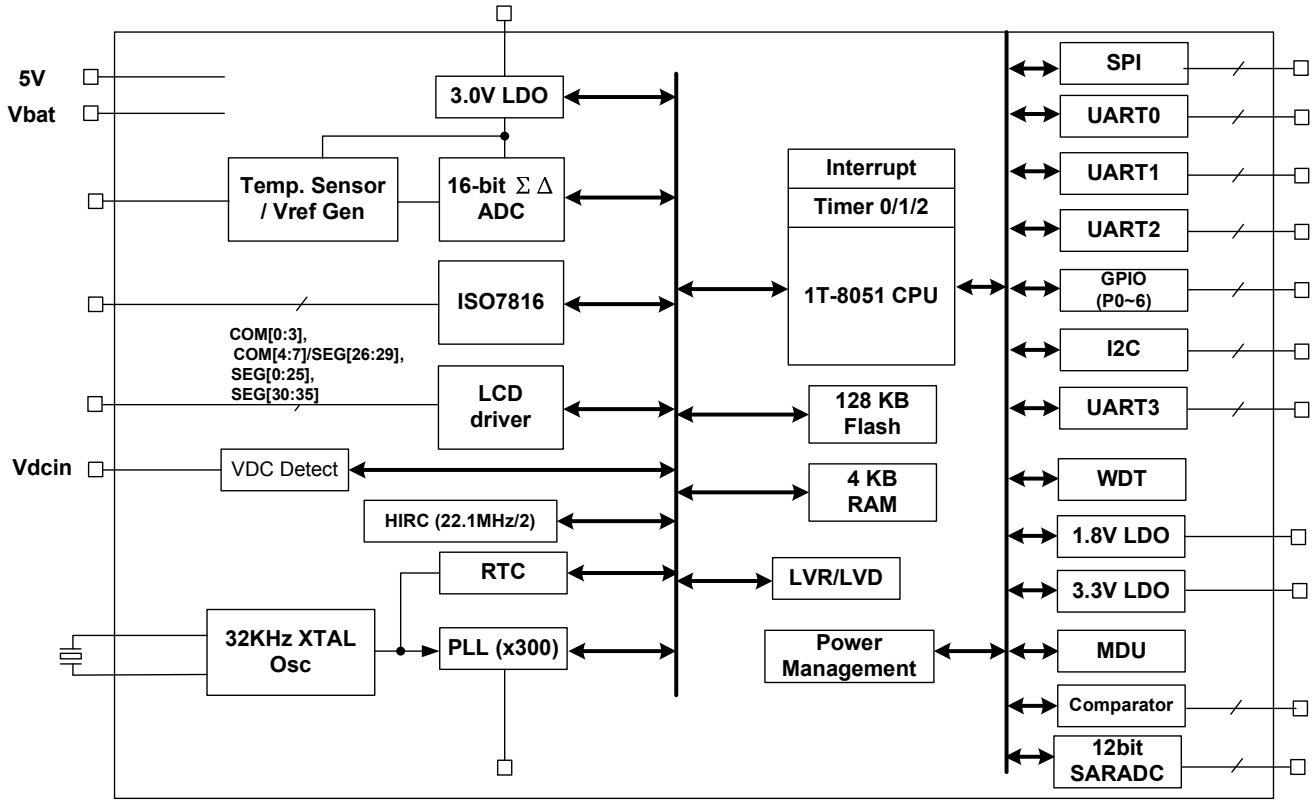
80 Pin LQFP



64 Pin SOP


VIO3 64
P00/ADC0 63
P01/ADC1 62
P02/ADC2 61
P03/ADC3 60
P20/MOSI/TXD3/ADC8 59
P21/MISO/RXD3 58
P22/TXD2/INT0 57
P23/RXD2/INT1 56
P24/TXD0 55
P25/RXD0 54
P26/ICCD/INT0 53
P27/CLK7816/INT1 52
P72/ESAMD 51
P71/SCLK/INT1 50
P70/SS/INT0 49
VLDO3 1
VCC 2
VREF 3
V5V 4
VDCIN 5
VSS 6
XTAL1 7
XTAL2 8
VBAT 9
VDD 10
CPLL 11
RSTN 12
O1HZ/T2/P10 13
I1HZ/T2EX/P11 14
IICSDA/INT0/P12 15
IICSCL/INT1/P13 16
48 P67/OCISDA/Seg0
47 P66/OCISCL/Seg1
46 P61/Seg6
45 P60/Seg7
44 P57/Seg8
43 P56/Seg9
42 P55/Seg10
41 P54/Seg11
40 P53/Seg12
39 P52/Seg13
38 P51/Seg14
37 P50/Seg15
36 P47/Seg16
35 P46/Seg17
34 P45/Seg18
33 P44/Seg19
17 TXD1/T0/P14
18 RXD1/T1/P15
19 Com0
20 Com1
21 Com2
22 Com3
23 Com4/Seg29
24 Com5/Seg28
25 Com6/Seg27
26 Com7/Seg26
27 Seg25/CLKOUT/P36
28 Seg24/P37
29 Seg23/P40
30 Seg22/P41
31 Seg21/P42
32 Seg20/P43
OB59A128A1W64VP
YWW
(64 LQFP Top View)

Block Diagram



OB59A128A1 Block Diagram

Pin Description

64L LQFP	80L LQFP	Symbol		I/O	Description
			LCD		
1	1	VLDO3		O	3.3V LDO output (need to add tantalum capacitor (0.1u~4.7uF))
2	2	VCC		O	3V power supply input for TSB, ADC; 3V LDO output (need to add tantalum capacitor (0.1u~4.7uF))
3	3	VREF		IO	Voltage reference (Recommended to add capacitor)
4	4	V5V		P	5V DC power supply (Primary power input pin, working voltage range :2.2V~5.5V)
5	5	VDCIN		I	low power detect
6	6	VSS		P	Digital Ground
7	7	XTAL1		O	Crystal output
8	8	XTAL2		I	Crystal input
9	9	VBAT		P	Battry power supply(Secondary power input ; power source of RTC, VDC Detector)
10	10	VDD		O	1.8V LDO output (need to add tantalum capacitor (0.1u~4.7uF))
11	11	CPLL		O	To connect decoupling capacitor for PLL
12	12	RSTN		I	Reset , low active
13	13	O1HZ/T2/P10		IO	RTC 1Hz output & Timer2 external input & bit0 of PORT1
14	14	I1HZ/T2EX/P11		IO	RTC 1Hz input ; Timer2 external capture/reload & bit1 of PORT1
15	15	IICSDA/P12/INT0		IO	IIC data pin & bit2 of PORT1 & External interrupt0(swap)
16	16	IICSCL/P13/INT1		IO	IIC clock pin & bit3 of PORT1 & External interrupt1(swap)
17	17	T0/P14/TXD1		IO	Timer0 external input & bit4 of PORT1
18	18	T1/P15/RXD1		IO	Timer1 external input & bit5 of PORT1
	19	CMP0NIN/P16		IO	Comparator0 negtive input & bit6 of PORT1
	20	CMP0PIN/P17		IO	Comparator0 positive input & bit7 of PORT1
	21	CMP1NIN/P30	Seg35	IO	Comparator1 negtive input & Bit0 of PORT3
	22	CMP1PIN/P31	Seg34	IO	Comparator1 positive input & Bit1 of PORT3
	23	CMP2NIN/P32	Seg33	IO	Comparator2 negtive input & Bit2 of PORT3
	24	CMP2PIN/P33	Seg32	IO	Comparator2 positive input &Bit3 of PORT3
	25	CC3/P34	Seg31	IO	Compare/capture channel3 & bit4 of PORT3
	26	CC2/P35	Seg30	IO	Compare/capture channel2 & bit5 of PORT3
19	27		Com0	IO	
20	28		Com1	IO	
21	29		Com2	IO	
22	30		Com3	IO	
23	31		Com4/Seg29	IO	
24	32		Com5/Seg28	IO	
25	33		Com6/Seg27	IO	
26	34		Com7/Seg26	IO	
27	35	P36/CLKOUT	Seg25	IO	Bit6 of PORT3 & system clock output
28	36	P37	Seg24	IO	Bit7 of PORT3
29	37	P40	Seg23	IO	Bit0 of PORT4
30	38	P41	Seg22	IO	Bit1 of PORT4
31	39	P42	Seg21	IO	Bit2 of PORT4
32	40	P43	Seg20	IO	Bit3 of PORT4
33	41	P44	Seg19	IO	Bit4 of PORT4
34	42	P45	Seg18	IO	Bit5 of PORT4
35	43	P46	Seg17	IO	Bit6 of PORT4
36	44	P47	Seg16	IO	Bit7 of PORT4
37	45	P50	Seg15	IO	Bit0 of PORT5
38	46	P51	Seg14	IO	Bit1 of PORT5
39	47	P52	Seg13	IO	Bit2 of PORT5

40	48	P53	Seg12	IO	Bit3 of PORT5
41	49	P54	Seg11	IO	Bit4 of PORT5
42	50	P55	Seg10	IO	Bit5 of PORT5
43	51	P56	Seg9	IO	Bit6 of PORT5
44	52	P57	Seg8	IO	Bit7 of PORT5
45	53	P60	Seg7	IO	Bit0 of PORT6
46	54	P61	Seg6	IO	Bit1 of PORT6
	55	CC1/P62	Seg5		Compare/capture channel1 & bit2 of PORT6
	56	CC0/P63	Seg4		Compare/capture channel0 & bit3 of PORT6
	57	P64	Seg3		bit4 of PORT6
	58	P65	Seg2		bit5 of PORT6
47	59	OCISCL/P66	Seg1		On chip instrument serial clock & Bit6 of PORT6
48	60	OCISDA/P67	Seg0		On chip instrument serial data & Bit7 of PORT6
49	61	SS/INT0/P70			SPI slave select & External interrupt0 & bit0 of PORT7
50	62	SCLK/INT1/P71			SPI clock & External interrupt1 & bit1 of PORT7
51	63	ESAMD/RXD1/P72			ISO7816 data to connect with ESAM & UART channel1 receive data & bit2 of PORT7
52	64	CLK7816/TXD1/P27 /INT1			ISO7816 clock & UART channel1 transmit data & bit7 of PORT2 & External interrupt1(swap)
53	65	ICCD/P26/INT0			ISO7816 data to connect with IC Card & bit6 of PORT2 & External interrupt0(swap)
54	66	RXD0/P25		IO	UART channel0 receive data & bit5 of PORT2
55	67	TXD0/P24		IO	UART channel0 transmit data with 38KHz modulation option & bit4 of PORT2
56	68	RXD2/P23/INT1		IO	UART channel2 receive data & bit3 of PORT2 & External interrupt1(swap)
57	69	TXD2/P22/INT0		IO	UART channel2 transmit data & bit2 of PORT2 & External interrupt0(swap)
58	70	MISO/RXD3/P21		IO	SPI master in slave out & UART channel3 receive data & bit1 of PORT2
59	71	MOSI/TXD3/P20/ADC 8		IO	SPI master out slave in & UART channel3 transmit data & bit0 of PORT2 & ADC input channel 7
	72	ADC7/P07		IO	ADC input channel 7 & bit7 of PORT0
	73	ADC6/P06		IO	ADC input channel 6 & bit6 of PORT0
	74	ADC5/P05		IO	ADC input channel 5 & bit5 of PORT0
	75	ADC4/P04		IO	ADC input channel 4 & bit4 of PORT0
60	76	ADC3/P03		IO	ADC input channel 3 & bit3 of PORT0
61	77	ADC2/P02		IO	ADC input channel 2 & bit2 of PORT0
62	78	ADC1/P01		IO	ADC input channel 1 & bit1 of PORT0
63	79	ADC0/P00		IO	ADC input channel 0 & bit0 of PORT0
64	80	VIO3		P	IO (P0,P2,P7) VDD power, Ex: 3V or 5V

Special Function Register (SFR)

A map of the Special Function Registers is shown as below:

Direct access Mode

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8	IICS	IICCTL	IICA1	IICA2	IICRWD	IICEBT	Cmp0CON	Cmp1CON	**FF**
F0	B	SPIC1	SPIC2	SPITXD	SPIRXD	SPIS	OpPin	TAKEY	**F7**
E8	P4	MD0	MD1	MD2	MD3	MD4	MD5	ARCON	**EF**
E0	ACC	ISPFAH	ISPFAL	ISPFD	ISPFC	INTS	LVC	SWRES	**E7**
D8	P5	PFCON	P3M0	P3M1	P4M0	P4M1	P5M0	P5M1	**DF**
D0	PSW	CCEN2	P0M0	P0M1	P1M0	P1M1	P2M0	P2M1	**D7**
C8	T2CON	CCCON	CRCL	CRCH	TL2	TH2	OpPin2	Cmp2CON	**CF**
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3	**C7**
B8	IEN1	IP1	S0RELH	S1RELH	S2RELH	PDP4	PDP5	PDP6	**BF**
B0	P3	S3CON	S3BUF	S3RELL	S3RELH	PSBS	WDTC	WDTK	**B7**
A8	IEN0	IP0	S0RELL			ISPBS	P7	PDP7	**AF**
A0	P2	RSTS	PDP0	PDP1	P7MD	P6M1	PDP2	PDP3	**A7**
98	S0CON	S0BUF	IEN2	S1CON	S1BUF	S1RELL	P6M0	INTLA	**9F**
90	P1	AUX	AUX2	S2CON	S2BUF	S2RELL	P6	IRCON2	**97**
88	TCON0	TMOD	TL0	TL1	TH0	TH1	CKCON	IFCON	**8F**
80	P0	SP	DPL	DPH	DPL1	DPH1	RCON	PCON	**87**
Hex\Bin	**X000**	**X001**	**X010**	**X011**	**X100**	**X101**	**X110**	**X111**	**Bin/Hex**

Note: Special Function Registers reset values and description for OB59A128A1.

Register	Location: 80h ~ 8Fh	Reset value	Description
SYSTEM			
SP	81h	07h	Stack Pointer
ACC	E0h	00h	Accumulator
PSW	D0h	00h	Program Status Word
B	F0h	00h	B Register
DPL	82h	00h	Data Pointer 0 Low Byte
DPH	83h	00h	Data Pointer 0 High Byte
DPL1	84h	00h	Data Pointer 1 Low Byte
DPH1	85h	00h	Data Pointer 1 High Byte
AUX	91h	00h	Auxiliary Register
PCON	87h	0Ch	Power Control
CKCON	8Eh	10h	Clock Control Register
INTERRUPT & PRIORITY			
IRCON	C0h	00h	Interrupt Request Control Register
IRCON2	97h	00h	Interrupt Request Control Register 2
IEN0	A8h	00h	Interrupt Enable Register 0
IEN1	B8h	00h	Interrupt Enable Register 1
IEN2	9Ah	00h	Interrupt Enable Register 2
IP0	A9h	00h	Interrupt Priority Register 0
IP1	B9h	00h	Interrupt Priority Register 1
INTS	E5h	11h	Interrupt Select
INTLA	9Fh	00h	Interrupt Input Latch
UART 0			
PCON	87h	0Ch	Power Control
S0CON	98h	00h	Serial Port 0, Control Register
S0BUF	99h	00h	Serial Port 0, Data Buffer
S0RELL	AAh	00h	Serial Port 0, Reload Register, Low Byte
S0RELH	BAh	00h	Serial Port 0, Reload Register, High Byte
AUX	91h	00h	Auxiliary register
UART 1			
S1CON	9Bh	00h	Serial port 1, Control Register
S1BUF	9Ch	00h	Serial port 1, Data Buffer
S1RELL	9Dh	00h	Serial port 1, Reload Register, Low Byte
S1RELH	BAh	00h	Serial port 1, Reload Register, High Byte
AUX	91h	00h	Auxiliary register
UART2			
S2CON	93H	00H	Serial port 2, Control Register
S2BUF	94H	00H	Serial port 2, Data Buffer
S2RELL	95H	00H	Serial port 2, reload register, low byte

Register	Location: 80h ~ 8Fh	Reset value	Description
S2RELH	BBH	00H	Serial port 2, reload register, high byte
UART3			
S3CON	B1h	00h	Serial port 3, Control Register
S3BUF	B2h	00h	Serial port 3, Data Buffer
S3RELL	B3h	00h	Serial port 3, Reload Register, Low Byte
S3RELH	B4h	00h	Serial port 3, Reload Register, High Byte
WDT			
RSTS	A1h	00h	Reset Status Register
WDTC	B6h	04h	Watchdog Timer Reset Control Register
WDTK	B7h	00h	Watchdog Timer Refresh Key.
TAKEY	F7h	00h	Time Access Key Register
TIMER0/TIMER1			
TCON	88h	00h	Timer/Counter Control
TMOD	89h	00h	Timer Mode Control
TL0	8Ah	00h	Timer 0, low byte
TL1	8Bh	00h	Timer 1, low byte
TH0	8Ch	00h	Timer 0, high byte
TH1	8Dh	00h	Timer 1, high byte
PFCON	D9h	00h	Peripheral Frequency control register
PCA(TIMER2)			
AUX2	92h	00h	Auxiliary 2 register
CCEN	C1h	00h	Compare/Capture Enable Register
CCL1	C2h	00h	Compare/Capture Register 1, Low Byte
CCH1	C3h	00h	Compare/Capture Register 1, High Byte
CCL2	C4h	00h	Compare/Capture Register 2, Low Byte
CCH2	C5h	00h	Compare/Capture Register 2, High Byte
CCL3	C6h	00h	Compare/Capture Register 3, Low Byte
CCH3	C7h	00h	Compare/Capture Register 3, High Byte
T2CON	C8h	00h	Timer 2 Control Register
CCCON	C9h	00h	Compare/Capture Control Register
CRCL	CAh	00h	Compare/Reload/Capture Register, Low Byte
CRCH	CBh	00h	Compare/Reload/Capture Register, High Byte
TL2	CCh	00h	Timer 2, Low Byte Register
TH2	CDh	00h	Timer 2, High Byte Register
CCEN2	D1h	00h	Compare/Capture Enable 2 register
GPIO			
P0	80h	User define	Port 0
P1	90h	FFh	Port 1
P2	A0h	FFh	Port 2
P3	B0h	FFh	Port 3

Register	Location: 80h ~ 8Fh	Reset value	Description
P4	E8h	FFh	Port 4
P5	D8h	FFh	Port 5
P6	96h	FFh	Port 6
P7	AEh	FFh	Port 7
P0M0	D2h	00h	Port 0 output mode 0
P0M1	D3h	00h	Port 0 output mode 1
P1M0	D4h	00h	Port 1 output mode 0
P1M1	D5h	00h	Port 1 output mode 1
P2M0	D6h	00h	Port 2 output mode 0
P2M1	D7h	00h	Port 2 output mode 1
P3M0	DAh	00h	Port 3 output mode 0
P3M1	DBh	00h	Port 3 output mode 1
P4M0	DCh	00h	Port 4 output mode 0
P4M1	DDh	00h	Port 4 output mode 1
P5M0	DEh	00h	Port 5 output mode 0
P5M1	DFh	00h	Port 5 output mode 1
P6M0	9Eh	00h	Port 6 output mode 0
P6M1	A5h	00h	Port 6 output mode 1
P7MD	A4h	00h	Port 7 output mode 0,1
PDP0	A4h	00h	Power Down Port 0
PDP1	A5h	00h	Power Down Port 1
PDP2	A6h	00h	Power Down Port 2
PDP3	A7h	00h	Power Down Port 3
PDP4	BDh	00h	Power Down Port 4
PDP5	BEh	00h	Power Down Port 5
PDP6	BFh	00h	Power Down Port 6
PDP7	AFh	00h	Power Down Port 7
ISP/IAP/EEPROM			
IFCON	8Fh	00h	Interface Control Register
ISPFAH	E1h	FFh	ISP Flash Address-High Register
ISPFAL	E2h	FFh	ISP Flash Address-Low Register
ISPFD	E3h	FFh	ISP Flash Data Register
ISPFC	E4h	00h	ISP Flash control register
TAKEY	F7h	00h	Time Access Key Register
LVI/LVR/SOFTRESET			
RSTS	A1h	00h	Reset StatusRegister
LVC	E6h	60h	Low Voltage Control Register
SWRES	E7h	00h	Software Reset Register
TAKEY	F7h	00h	Time Access Key Register
SPI			
SPIC1	F1h	08h	SPI control register 1

Register	Location: 80h ~ 8Fh	Reset value	Description
SPIC2	F2h	00h	SPI control register 2
SPITXD	F3h	00h	SPI Transmit data buffer
SPIRXD	F4h	00h	SPI receive data buffer
SPIS	F5h	40h	SPI status register
IIC			
AUX	91h	00h	Auxiliary register
IICS	F8h	00h	IIC Status Register
IICCTL	F9h	04h	IIC Control Register
IICA1	FAh	A0h	IIC Channel Address 1 Register
IICA2	FBh	60h	IIC Channel Address 2 Register
IICRWD	FCh	00h	IIC Channel Read / Write Data Buffer
IICEBT	FDh	00h	IIC0 Enable Bus Transaction Register
MDU			
PCON	87h	0Ch	Power Control
ARCON	EFh	00h	Arithmetic Control register
MD0	E9h	00h	IIC status register
MD1	EAh	00h	IIC control register
MD2	EBh	00h	IIC channel 1 Address 1 register
MD3	ECh	00h	IIC channel 1 Address 2 register
MD4	EDh	00h	IIC channel 1 Read / Write Data buffer
MD5	EEh	00h	IIC Enable Bus Transaction register
COMP			
OPPIN	F6h	00h	Comparator Pin Select register
OPPIN2	CEh	00h	Comparator Pin Select2 register
CMP0CON	FEh	00h	Comparator 0 Control register
CMP1CON	FFh	00h	Comparator 1 Control register
CMP2CON	CFh	00h	Comparator 2 Control register
ISO7816			
CTL	FE01h	00h	7816 control register
FRAME_CTL_1	FE02h	38h	Frame control register 1
FRAME_CTL_2	FE03h	01h	Frame control register 2
CCLK	FE04h	02h	Clock output frequency setting register
ETUCLK	FE05h	0Bh	ETU period setting register
EGT	FE06h	00h	Extra guard time setting register
DATA_BUF	FE07h	00h	7816 data buffer register
INT	FE08h	00h	7816 interrupt setting register
INFO	FE09h	00h	7816 Tx/Rx data status register
RTC			
WTKEY	FF01h	**h	Write Time Key
SECONDS	FF02h	00h	Seconds
MINUTES	FF03h	00h	Minutes

Register	Location: 80h ~ 8Fh	Reset value	Description
HOURS	FF04h	00h	Hours
DATES	FF05h	01h	Dates
DAYS	FF06h	00h	Days
MONTHS	FF07h	01h	Months
YEARS	FF08h	00h	Years
RTCLATCH	FF09h	**h	RTL latch
ADJUSTL	FF0Ah	00h	Adjust (Calibration)
ADJUSTM	FF0Bh	00h	Adjust (Calibration)
INTENABLE	FF0Ch	00h	Interrupt Enable
INTFLAG	FF0Dh	00h	Interrupt Flag
ALMS	FF0Eh	00h	Alarm Seconds
ALMM	FF0Fh	00h	Alarm Minutes
ALMH	FF10h	00h	Alarm Hours
CTRSTA	FF1Fh	00h	Control Status
RCCH	FF20h	**h	Calibration Counter[23:16]
RCCM	FF21h	**h	Calibration Counter[15:8]
RCCL	FF22h	**h	Calibration Counter[7:0]
RCCS	FF23h	00h	Calibration Control/Status
RTC auto temp Cal			
Calibra_en	FF40h	00h	RTC Calibration enable
ref_h	FF41h	4Ah	REF High Byte Register
ref_l	FF42h	3Dh	REF Low Byte Register
t_turn_flag	FF43h	00h	Top Turn flag
t_turn	FF44h	14h	Top Turn
offset_turn	FF45h	00h	Top Turn offset
cofe_a[15:8]	FF46h	00h	Cofe a
Cofe_a[7:0]	FF47h	00h	Cofe a
Cofe_b[15:8]	FF48h	00h	Cofe b
Cofe_b[7:0]	FF49h	00h	Cofe b
Cofe_c[15:8]	FF4Ah	00h	Cofe c
Cofe_c[7:0]	FF4Bh	00h	Cofe c
fix_dis_a	FF4Ch	00h	temperature sensor fix value a
fix_dis_b	FF4Dh	00h	temperature sensor fix value b
fix_dis_c	FF4Eh	00h	temperature sensor fix value c
i_data_cvt_spc	FF4Fh	00h	special temperature value input
o_data_cvt_spc	FF50h	00h	special temperature value output
cvt_spc_avl	FF51h	00h	special temperature value output available
t_data_cvt	FF52h	00h	actual temperature value (sign number)
Data_calibra[15:8]	FF53h	00h	RTC calibration number [15:8]
Data_calibra [7:0]	FF54h	00h	RTC calibration number [7:0]
calibra_done	FF55h	00h	flag of RTC calibration done

Register	Location: 80h ~ 8Fh	Reset value	Description
calibra_duration	FF56h	00h	
IR			
IRTPRL	FF60h	00h	IR Tx Period Register, Low byte
IRTPRH	FF61h	00h	IR Tx Period Register, High byte
IRTDRL	FF62h	00h	IR Tx Duty Register, Low byte
IRTDRH	FF63h	00h	IR Tx Duty Register, High byte
LCD			
SYC	FF80h	00h	System Control Register
FRC	FF81h	08h	Frame-Rate Control Register
LCDCLKDIV	FF82h	00h	LCD Clock Divide Register
VLC	FF83h	90h	LCD Clock Divide Register
LCDC0	FF84h	00h	LCD/GPIO Configuration
LCDC1	FF85h	00h	LCD/GPIO Configuration
LCDC2	FF86h	00h	LCD/GPIO Configuration
LCDC3	FF87h	00h	LCD/GPIO Configuration
LCDC4	FF88h	00h	LCD/GPIO Configuration
TSB			
TSBCTL	FFE0h	40h	TSB control Register
TSB_VREF_V	FFE1h	00h	TSB VREF_V trimng Register
TSB_VREF_T	FFE2h	00h	TSB VREF_T trimng Register
ADC			
SADCC1	FFF0h	00h	SADC Control 1
ADCC2	FFE8h	08h	ADC Control 2 Register
ADCDH	FFE9h	00h	ADC data high byte
ADCDL	FFEAh	00h	ADC data low byte
SADC			
SADCC1	FFF0h	00h	SADC Control 1
SADCC2	FFF1h	00h	SADC Control 2
SADCDH	FFF2h	00h	SADC Data High
SADCDL	FFF3h	00h	SADC Data Low
SADCCS	FFF4h	00h	SADC Clock Select
SADCSH	FFF5h	00h	SADC Sample and Hold Time
SADCCT0	FFF8h	00h	SADC Calibration Tolerance 0
SADCCT1	FFF9h	00h	SADC Calibration Tolerance 1
SADCCT2	FFFAh	00h	SADC Calibration Tolerance 2
SADCCT3	FFFBh	00h	SADC Calibration Tolerance 3
SADCCT4	FFFCh	00h	SADC Calibration Tolerance 4
SADCCT5	FFFDh	00h	SADC Calibration Tolerance 5
SADCOVS	FFFEh	00h	SADC Overflow Status
SADCCAL	FFFFh	02h	SADC Calibration

Function Description

1. General Features

OB59A128A1 is an 8-bit micro-controller. All of its functions and the detailed meanings of SFR will be given in the following sections.

1.1 Embedded Flash

The program can be loaded into the embedded 128KB Flash memory via its writer or In-System Programming (ISP). The high-quality Flash has a 100K-write cycle life，suitable for re-programming and data recording as EEPROM.

1.2 IO Pads

The OB59A128A1 has Seven I/O ports: Port 0~7. Port 0~6 are 8-bit ports and Port 7 are 3-bit ports. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. As description in section 5.

All the pads for P0~P7 are with slew rate to reduce EMI. The IO pads can withstand 4KV ESD in human body mode guaranteeing the OB59A128A1's quality in high electro-static environments.

1.3 Instruction timing Selection

The conventional 52-series MCUs are 12T, i.e., 12 oscillator clocks per machine cycle. OB59A128A1 is a 1T to 8T MCU, i.e., its machine cycle is one-clock to eight-clock. In the other words, it can execute one instruction within one clock to only eight clocks.

Mnemonic: CKCON **Address: 8Eh**

7	6	5	4	3	2	1	0	Reset
-	ITS[2:0]			-	PLLRDY	CLKOUT[1:0]		10H

ITS: Instruction timing select.

ITS [2:0]	Instruction timing
000	1T mode
001	2T mode (default)
010	3T mode
011	4T mode
100	5T mode
101	6T mode
110	7T mode
111	8T mode

The default is in 2T mode, and it can be changed to another Instruction timing mode if CKCON [6:4] (at address 8Eh) is change any time. Not every instruction can be executed with one machine cycle. The exact machine cycle number for all the instructions are given in the next section.

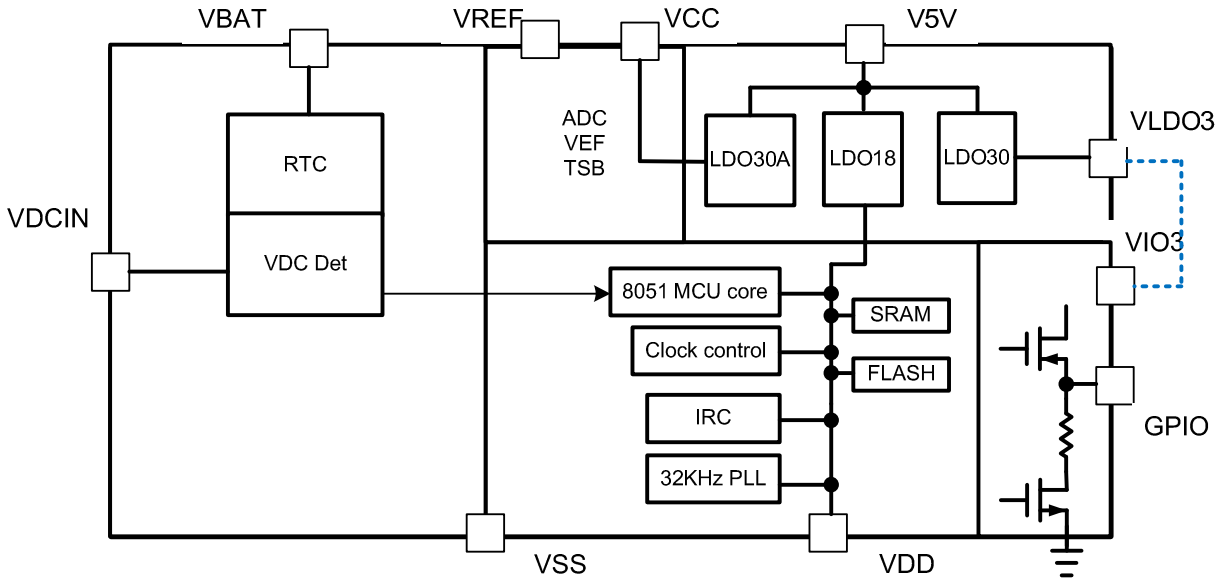
1.4 Power

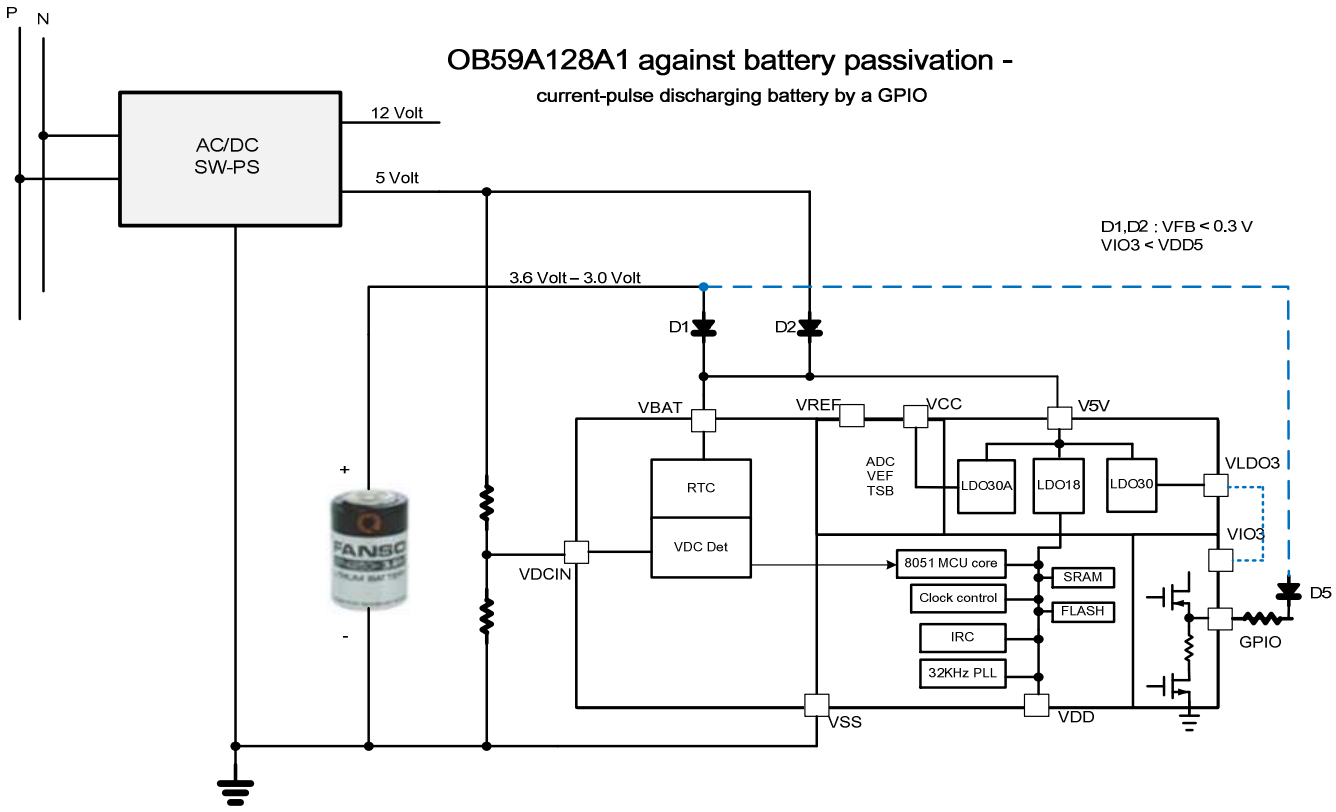
There are 2 power supply input which are V5V and VBAT on OB59A128A1. It support 2 power saving mode and 1 normal operating mode.

Power Source

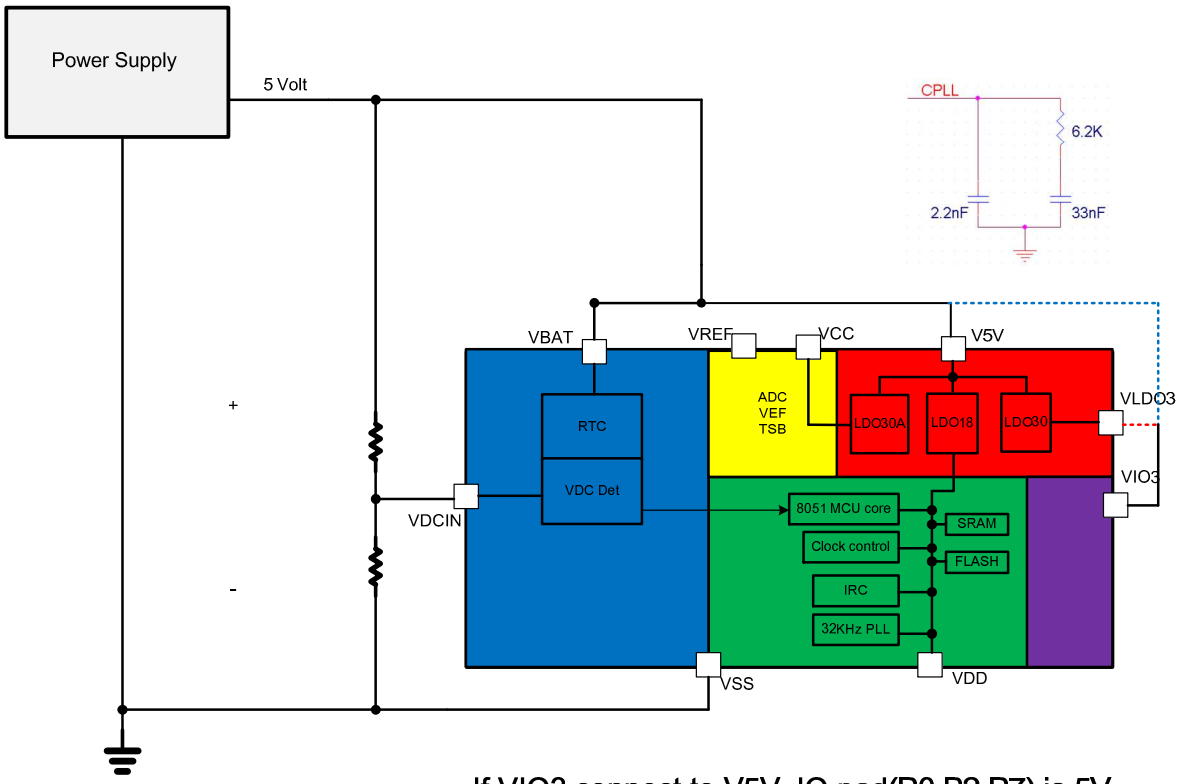
Chip main power: V5V supply 5V for chip main power.

Chip backup power: VBAT for RTC and VDC Detector.




OB59A128A1 against battery passivation -
current-pulse discharging battery by a GPIO
P
N
AC/DC
SW-PS
12 Volt
5 Volt
3.6 Volt – 3.0 Volt
D1,D2 : VFB < 0.3 V
VIO3 < VDD5
D1
D2
VBAT
VREF
VCC
V5V
RTC
VDC Det
VDCIN
ADC
VEF
TSB
LDO30A
LDO18
LDO30
VLDO3
VIO3
8051 MCU core
Clock control
IRC
32KHz PLL
SRAM
FLASH
GPIO
D5
VSS
VDD
+
-

OB59A128A1 Application Diagram



If VIO3 connect to V5V, IO pad(P0,P2,P7) is 5V
If VIO3 connect to VLDO3, IO pad(P0,P2,P7) is 3.3V

1.4.1 Power Domain

V5V: power source of 5V IO, LDO30, LDO30A and LDO18 (Primary power input pin, working voltage range :2.2V~5.5V)

VBAT: power source of RTC, VDC Detector(Secondary power input; power source of RTC, VDC Detector)

VLDO3: LDO30 output (3.3V) (Need to add tantalum capacitor (0.1u~4.7uF))

VCC: LDO30A output (3V) & supply ADC, TSB power (Need to add tantalum capacitor (0.1u~4.7uF))

VIO3: supply 3V IO power

VDD: supply 1.8V PLL, Flash, RAM and MCU digital power (Need to add tantalum capacitor (0.1u~4.7uF))

1.4.2 Power Mode

Supprt 3 operating mode

Normal mode: all modules are in normal operating. PCON[1:0]=00b

Idle mode: CPU stop, peripheral interface working. PCON[1:0]=01b

Stop mode: all functions' clock excepting PMU/RTC/WDT turn off, the related registers keep contents before entering Stop mode. PCON[1]=1b

Mnemonic: PCON **Address: 87h**

7	6	5	4	3	2	1	0	Reset
SMOD	MDUF	-	VDCIS	PDALDO3	PDLDO3	STOP	IDLE	40H

1.5 RESET

1.5.1 Software RESET function

OB59A128A1 provides one software reset mechanism to reset whole chip. To perform a software reset, the firmware must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the Software Reset register (SWRES) write attribute. After SWRES register obtain the write authority, the firmware can write FFh to the SWRES register. The hardware will decode a reset signal that "OR" with the other hardware reset. The SWRES register is self-reset at the end of the software reset procedure.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Software Reset function											
RSTS	Reset status register	A1h	CFRF	PRRF	LVRLPF	PDRF	WDTRF	SWRF	LVRF	PORF	00H
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
SWRES	Software Reset register	E7h	SWRES [7:0]								00H

1.5.2 Reset status

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
CFRF	PRRF	LVRLPF	PDRF	WDTR	SWRF	LVRF	PORF	00H

CFRF Clock failure reset flag.

When Clock failure reset event occur, CFRF is set to 1. This flag can be clear by software.

PRRF Power recovery reset flag.

When VDCIN falling (Vil ≒ 1.0V , Vih ≒ 1.1V), PRRF is set to 1. This flag can be clear by software.

LVRLPF Low voltage reset(Low Power) flag.

When MCU is reset by LVR(Low Power), LVRLPF flag will be set to one by hardware. This flag clear by software. Low power LVR is a source of Brown out reset.

PDRF: Pad reset flag.

When MCU is reset by reset pad, PDRF flag will be set to one by hardware. This flag clear by software.

WDTF: Watchdog timer reset flag.

When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software.

SWRF: Software reset flag.

When MCU is reset by software, SWRF flag will be set to one by hardware. This flag clear by software.

LVRF: Low voltage reset flag.

When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.

PORF: Power on reset flag.

When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

1.5.3 Time Access Key register (TAKEY)

Mnemonic: TAKEY **Address:F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Software reset register (SWRES) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the SWRES register write attribute.

That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

1.5.4 Software Reset register (SWRES)

Mnemonic: SWRES **Address:E7H**

7	6	5	4	3	2	1	0	Reset
SWRES [7:0]								00H

SWRES [7:0]: Software reset register bit. These 8-bit is self-reset at the end of the reset procedure.

SWRES [7:0] = FFh, software reset.

SWRES [7:0] = 00h ~ FEh, MCU no action.

1.5.5 Example of software reset

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah     ; enable SWRES write attribute
MOV SWRES, #0FFh ; software reset MCU
```

1.6 Clocks

The default clock is the 11.0592MHz Internal OSC. This clock is used during the initialization stage. The major work of the initialization stage is to determine the clock source used in normal operation. When chip wake up from Stop or Sleep, the system clock will start with internal OSC. then switch to PLL (if user select) as PLL stable.

The system clock sources are from the PLL or the internal OSC as shown in Table 1 1，the clock source can be set by writer or ICP.

Table 1-1: Selection of clock source

OP4 FCLK[1:0]	System clock	Frequency
11	Internal PLL	9.83MHz
10	Internal RC	22.1184MHz
01, 00	Internal RC	22.1184/2 = 11.0592MHz

There may be having a little variance in the frequency from the internal OSC. The max variance as giving in Table 1-2.

Table 1-2: Temperature with variance

Temperature	**Max Variance**
25℃	±2%

The OB59A128A1 can Generator a clock out signal at P3.6， when user use PLL or internal OSC as system clock. The CKCON [1:0] (at address 8Eh) can change any time.

CLKOUT: Clock output select

CKCON [1:0]	**Mode.**
00	GPIO(default)
01	Fosc
10	Fosc/2
11	Fosc/4

2. Instruction Set

All OB59A128A1 instructions are binary code compatible and perform the same functions as they do with the industry standard 8051. The following tables give a summary of the instruction set cycles of the OB59A128A1 Microcontroller core.

Table 2-1: Arithmetic operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	28-2F	1	1
ADD A,direct	Add direct byte to accumulator	25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	26-27	1	2
ADD A,#data	Add immediate data to accumulator	24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	38-3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	36-37	1	2
ADDC A,#data	Add immediate data to A with carry flag	34	2	2
SUBB A,Rn	Subtract register from A with borrow	98-9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	96-97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	94	2	2
INC A	Increment accumulator	04	1	1
INC Rn	Increment register	08-0F	1	2
INC direct	Increment direct byte	05	2	3
INC @Ri	Increment indirect RAM	06-07	1	3
INC DPTR	Increment data pointer	A3	1	1
DEC A	Decrement accumulator	14	1	1
DEC Rn	Decrement register	18-1F	1	2
DEC direct	Decrement direct byte	15	2	3
DEC @Ri	Decrement indirect RAM	16-17	1	3
MUL AB	Multiply A and B	A4	1	5
DIV	Divide A by B	84	1	5
DA A	Decimal adjust accumulator	D4	1	1

Table 2-2: Logic operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	58-5F	1	1
ANL A,direct	AND direct byte to accumulator	55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	56-57	1	2
ANL A,#data	AND immediate data to accumulator	54	2	2
ANL direct,A	AND accumulator to direct byte	52	2	3
ANL direct,#data	AND immediate data to direct byte	53	3	4
ORL A,Rn	OR register to accumulator	48-4F	1	1
ORL A,direct	OR direct byte to accumulator	45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	46-47	1	2
ORL A,#data	OR immediate data to accumulator	44	2	2
ORL direct,A	OR accumulator to direct byte	42	2	3
ORL direct,#data	OR immediate data to direct byte	43	3	4
XRL A,Rn	Exclusive OR register to accumulator	68-6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	66-67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	63	3	4
CLR A	Clear accumulator	E4	1	1
CPL A	Complement accumulator	F4	1	1
RL A	Rotate accumulator left	23	1	1
RLC A	Rotate accumulator left through carry	33	1	1
RR A	Rotate accumulator right	03	1	1
RRC A	Rotate accumulator right through carry	13	1	1
SWAP A	Swap nibbles within the accumulator	C4	1	1

Table 2-3: Data transfer

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	E8-EF	1	1
MOV A,direct	Move direct byte to accumulator	E5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	E6-E7	1	2
MOV A,#data	Move immediate data to accumulator	74	2	2
MOV Rn,A	Move accumulator to register	F8-FF	1	2
MOV Rn,direct	Move direct byte to register	A8-AF	2	4
MOV Rn,#data	Move immediate data to register	78-7F	2	2
MOV direct,A	Move accumulator to direct byte	F5	2	3
MOV direct,Rn	Move register to direct byte	88-8F	2	3
MOV direct1,direct2	Move direct byte to direct byte	85	3	4
MOV direct,@Ri	Move indirect RAM to direct byte	86-87	2	4
MOV direct,#data	Move immediate data to direct byte	75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	F6-F7	1	3
MOV @Ri,direct	Move direct byte to indirect RAM	A6-A7	2	5
MOV @Ri,#data	Move immediate data to indirect RAM	76-77	2	3
MOV DPTR,#data16	Load data pointer with a 16-bit constant	90	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	93	1	3
MOVC A,@A+PC	Move code byte relative to PC to accumulator	83	1	3
MOVX A,@Ri	Move external RAM (8-bit addr) to A	E2-E3	1	3
MOVX A,@DPTR	Move external RAM (16-bit addr) to A	E0	1	3
MOVX @Ri,A	Move A to external RAM (8-bit addr)	F2-F3	1	4
MOVX @DPTR,A	Move A to external RAM (16-bit addr)	F0	1	4
PUSH direct	Push direct byte onto stack	C0	2	4
POP direct	Pop direct byte from stack	D0	2	3
XCH A,Rn	Exchange register with accumulator	C8-CF	1	2
XCH A,direct	Exchange direct byte with accumulator	C5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator	C6-C7	1	3
XCHD A,@Ri	Exchange low-order nibble indir. RAM with A	D6-D7	1	3

Table 2-4: Program branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	xxx11	2	6
LCALL addr16	Long subroutine call	12	3	6
RET	from subroutine	22	1	4
RETI	from interrupt	32	1	4
AJMP addr11	Absolute jump	xxx01	2	3
LJMP addr16	Long iump	02	3	4
SJMP rel	Short jump (relative addr.)	80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	73	1	2
JZ rel	Jump if accumulator is zero	60	2	3
JNZ rel	Jump if accumulator is not zero	70	2	3
JC rel	Jump if carry flag is set	40	2	3
JNC	Jump if carry flag is not set	50	2	3
JB bit,rel	Jump if direct bit is set	20	3	4
JNB bit,rel	Jump if direct bit is not set	30	3	4
JBC bit,direct rel	Jump if direct bit is set and clear bit	10	3	4
CJNE A,direct rel	Compare direct byte to A and jump if not equal	B5	3	4
CJNE A,#data rel	Compare immediate to A and jump if not equal	B4	3	4
CJNE Rn,#data rel	Compare immed. to reg. and jump if not equal	B8-BF	3	4
CJNE @Ri,#data rel	Compare immed. to ind. and jump if not equal	B6-B7	3	4
DJNZ Rn,rel	Decrement register and jump if not zero	D8-DF	2	3
DJNZ direct,rel	Decrement direct byte and jump if not zero	D5	3	4
NOP	No operation	00	1	1

Table 2-5: Boolean manipulation

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	C3	1	1
CLR bit	Clear direct bit	C2	2	3
SETB C	Set carry flag	D3	1	1
SETB bit	Set direct bit	D2	2	3
CPL C	Complement carry flag	B3	1	1
CPL bit	Complement direct bit	B2	2	3
ANL C,bit	AND direct bit to carry flag	82	2	2
ANL C,/bit	AND complement of direct bit to carry	B0	2	2
ORL C,bit	OR direct bit to carry flag	72	2	2
ORL C,/bit	OR complement of direct bit to carry	A0	2	2
MOV C,bit	Move direct bit to carry flag	A2	2	2
MOV bit,C	Move carry flag to direct bit	92	2	3

3. Memory Structure

3.1 Program Memory .

The OB59A128A1 has 128KB on-chip flash memory, using bank select method(by program SFR(PSBS)), user can access (128-1)K program memory, on which include up to 8K byte specific ISP service program memory space. The address range for the (128-1)K byte is $0_0000 to $1_FC00. The address range for the ISP service program is $1_DC00 to $1_FBFF. The ISP service program size can be partitioned as N blocks of 1K byte (N=0 to 8). When N=0 means no ISP service program space available, total (128-1)K byte memory used as program memory. When N = 1 means address $1_F800 to $1_FBFF reserved for ISP service program. When N=2 means memory address $1_F400 to $1_FBFF reserved for ISP service program…etc. Value N can be set and programmed into OB59A128A1 information block by writer. As shown in Fig. 3-1

The OB59A128A1 also can be used without bank select. at this moment, 64KB (0x0000~0xFFFF) program memory can be used, the other flash memory can be used as EEPROM and ISP(0x1_DC00~0x1_FBFF).

The OB59A128A1 always use the top 1KB(0x1_FC00~0x1_FFFF) as Information Block page1.

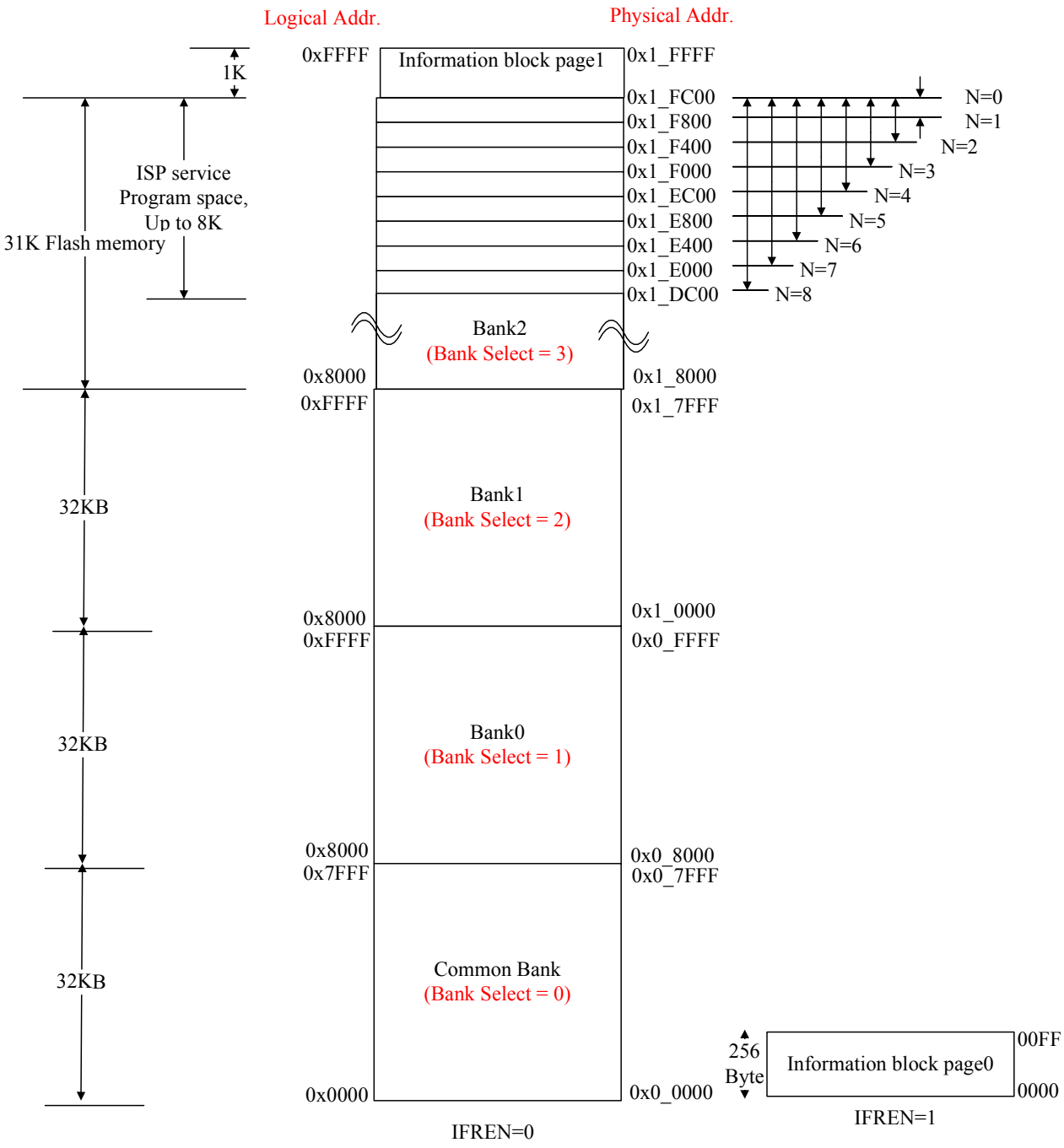


Fig. 3-1: OB59A128A1 programmable Flash

3.2 Data Memory

The OB59A128A1 has 4K + 256B on-chip SRAM, 256B of it are the same as general 8052 internal memory structure while the expanded 4K Bytes on-chip SRAM can be accessed by external memory addressing method (by instruction MOVX.). As shown in Fig. 3-2

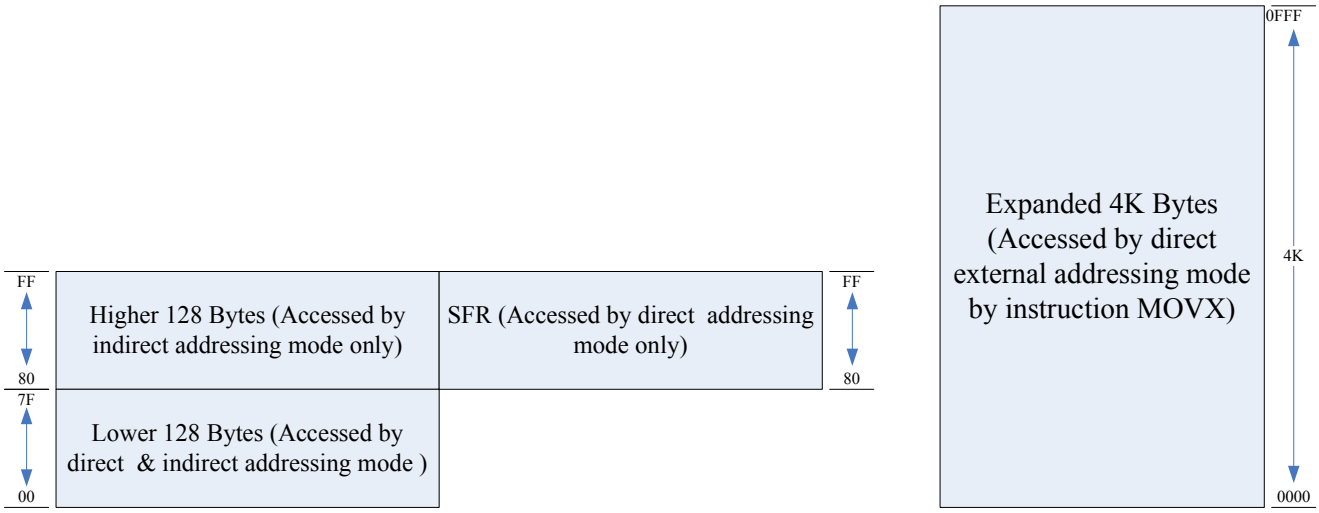


Fig. 3-2: RAM architecture

3.3 Data memory - lower 128 byte (00h to 7Fh)

Data memory 00h to FFh is the same as 8052.
The address 00h to 7Fh can be accessed by direct and indirect addressing modes.
Address 00h to 1Fh is register area.
Address 20h to 2Fh is memory bit area.
Address 30h to 7Fh is for general memory area.

3.4 Data memory - higher 128 byte (80h to FFh)

The address 80h to FFh can be accessed by indirect addressing mode.
Address 80h to FFh is data area.

3.5 Data memory - Expanded 4K Bytes (0000 to 0x0FFFh)

From external address 0000h to 0FFFh is the on-chip expanded SRAM area, total 4K Bytes. This area can be accessed by external direct addressing mode (by instruction MOVX).

The address space of instruction MOVX @Ri, i=0, 1 is determined by RCON [3:0] of special function register 86h RCON (internal RAM control register). The default setting of RCON [3:0] is 00h (page0). One page of data RAM is 256 bytes.

MOVX @Ri, A MOVX A,@Ri	$0 \leqq$ RCON[7:0] $\leqq$ 0x0F

4. CPU Engine

The OB59A128A1 engine is composed of four components:

(1) Control unit
(2) Arithmetic – logic unit
(3) Memory control unit
(4) RAM and SFR control unit

The OB59A128A1 engine allows to fetch instruction from program memory and to execute using RAM or SFR. The following chapter describes the main engine register.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
8051 Core											
ACC	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00H
B	B register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00H
PSW	Program status word	D0h	CY	AC	F0	RS[1:0]		OV	PSW.1	P	00H
SP	Stack Pointer	81h	SP[7:0]								07H
DPL	Data pointer low 0	82h	DPL[7:0]								00H
DPH	Data pointer high 0	83h	DPH[7:0]								00H
DPL1	Data pointer low 1	84h	DPL1[7:0]								00H
DPH1	Data pointer high 1	85h	DPH1[7:0]								00H
AUX	Auxiliary register	91h	BRGS	P2IIC	-	-	-	-	P42S3	DPS	00H
CKCON	Clock control register	8Eh	-	ITS[2:0]			-	PLLRDY	CLKOUT[1:0]		10H
IFCON	Interface control register	8Fh	-	CDPR	-	-	Flag1A	Flag0B	Flag0A	ISPE	00H

4.1 Accumulator

ACC is the Accumulator register. Most instructions use the accumulator to store the operand.

Mnemonic: ACC **Address: E0h**

7	6	5	4	3	2	1	0	Reset
ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h

ACC[7:0]: The A (or ACC) register is the standard 8052 accumulator。

4.2 B Register

The B register is used during multiply and divide instructions. It can also be used as a scratch pad register to store temporary data.

Mnemonic: B **Address: F0h**

7	6	5	4	3	2	1	0	Reset
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h

B[7:0]: The B register is the standard 8052 register that serves as a second accumulator.

4.3 Program Status Word

Mnemonic: PSW **Address: D0h**

7	6	5	4	3	2	1	0	Reset
CY	AC	F0	RS [1:0]		OV	F1	P	00h

CY: Carry flag.

AC: Auxiliary Carry flag for BCD operations.

F0: General purpose Flag 0 available for user.

RS[1:0]: Register bank select, used to select working register bank.

RS[1:0]	Bank Selected	Location
00	Bank 0	00h – 07h
01	Bank 1	08h – 0Fh
10	Bank 2	10h – 17h
11	Bank 3	18h – 1Fh

OV: Overflow flag.

F1: General purpose Flag 1 available for user.

P: Parity flag, affected by hardware to indicate odd/even number of “one” bits in the Accumulator, i.e. even parity.

4.4 Stack Pointer

The stack pointer is a 1-byte register initialized to 07h after reset. This register is incremented before PUSH and CALL instructions, causing the stack to start from location 08h.

Mnemonic: SP **Address: 81h**

7	6	5	4	3	2	1	0	Reset
SP [7:0]								07h

SP[7:0]: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

4.5 Data Pointer

The data pointer (DPTR) is 2-bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (e.g. MOV DPTR, #data16) or as two separate registers (e.g. MOV DPL,#data8). It is generally used to access the external code or data space (e.g. MOVC A, @A+DPTR, @DPTR respectively).

Mnemonic: DPL **Address: 82h**

7	6	5	4	3	2	1	0	Reset
DPL [7:0]								00h

DPL[7:0]: Data pointer Low 0

Mnemonic: DPH **Address: 83h**

7	6	5	4	3	2	1	0	Reset
DPH [7:0]								00h

DPH [7:0]: Data pointer High 0

4.6 Data Pointer 1

The Dual Data Pointer accelerates the moves of data block. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the OB59A128A1 core the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located in LSB of AUX register (DPS).

The user switches between pointers by toggling the LSB of AUX register. All DPTR-related instructions use the currently selected DPTR for any activity.

Mnemonic: DPL1 **Address: 84h**

7	6	5	4	3	2	1	0	Reset
DPL1 [7:0]								00h

DPL1[7:0]: Data pointer Low 1

Mnemonic: DPH1 **Address: 85h**

7	6	5	4	3	2	1	0	Reset
DPH1 [7:0]								00h

DPH1[7:0]: Data pointer High 1

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	P2IIC	-	-	-	-	P42S3	DPS	00H

DPS: Data Pointer selected register.

DPS = 1 – Selected DPTR1.

4.7 Clock control register

Mnemonic: CKCON **Address: 8Eh**

7	6	5	4	3	2	1	0	Reset
-	ITS[2:0]			-	PLLRDY	CLKOUT[1:0]		10H

ITS[2:0]: Instruction timing select.

ITS [2:0]	Mode
000	1T mode
001	2T mode (default)
010	3T mode
011	4T mode
100	5T mode
101	6T mode
110	7T mode
111	8T mode

PLLRDY: 1: Indicate PLL stable, PLL is the system clock.

0: Indicate internal OSC is the system clock.

CLKOUT[1:0]: Clock output select.

CLKOUT[1:0]	Mode
00	GPIO(default)
01	Fosc
10	Fosc/2
11	Fosc/4

It can be used when the system clock is the internal RC oscillator.

4.8 Interface control register

Mnemonic: IFCON **Address: 8Fh**

7	6	5	4	3	2	1	0	Reset
-	CDPR	-	-	-	-	-	ISPE	00H

CDPR: Code protect (Read Only)

ISPE: ISP function enable bit.

ISPE = 1, enable ISP function

ISPE = 0, disable ISP function

5. GPIO

The OB59A128A1 has four I/O ports: Port 0, Port 1, Port 2, Port 3. Ports 0, 1, 2 are 8-bit ports ,Ports 2 are 7-bit ports , and Ports 3 are 6-bit ports. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin. All I/O port pins on the OB59A128A1 may be configured by software to one fo four types on a pin-by-pin basis, shown as below:

Mnemonic	Description	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
I/O port function register											
P0M0	Port 0 output mode 0	D2h	P0M0 [7:0]								00H
P0M1	Port 0 output mode 1	D3h	P0M1[7:0]								00H
P1M0	Port 1 output mode 0	D4h	P1M0[7:0]								00H
P1M1	Port 1 output mode 1	D5h	P1M1[7:0]								00H
P2M0	Port 2 output mode 0	D6h	P2M0[7:0]								00H
P2M1	Port 2 output mode 1	D7h	P2M1[7:0]								00H
P3M0	Port 3 output mode 0	DAh	P3M0[7:0]								00H
P3M1	Port 3 output mode 1	DBh	P3M1[7:0]								00H
P4M0	Port 4 output Mode 0	DCh	P4M0[7:0]								00H
P4M1	Port 4 output Mode 1	DDh	P4M1[7:0]								00H
P5M0	Port 5 output Mode 0	DEh	P5M0[7:0]								00H
P5M1	Port 5 output mode 1	DFh	P5M1[7:0]								00H
P6M0	Port 6 output Mode 0	9Eh	P6M0[7:0]								00H
P6M1	Port 6 output Mode 0	A5h	P6M1[7:0]								00H
P7MD	Port 7 output mode 0,1	A4h	-	P7M1[2:0]			-	P7M0[2:0]			00H

*OP40~OP43, OP48~OP4B by writer programming set.

PxM1.y	PxM0.y	Port output mode
0	0	Quasi-bidirectional (standard 8051 port outputs) (pull-up)
0	1	Push-pull
1	0	Input only (high-impedance)
1	1	Open drain

For general-purpose applications, every pin can be assigned to either high or low independently. As shown below:

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Ports											
Port 7	Port 7	AEh	-	-	-	-	-	P7.2	P7.1	P7.0	07h
Port 6	Port 6	96h	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0	FFh
Port 5	Port 5	D8h	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0	FFh
Port 4	Port 4	E8h	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	FFh

Port 3	Port 3	B0h	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh
Port 2	Port 2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
Port 1	Port 1	90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh
Port 0	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh
AUX	Auxiliary register	91h	BRGS		-	-	-	-		DPS	00h

Mnemonic: P0 **Address: 80h**

7	6	5	4	3	2	1	0	Reset
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

P0.7~ 0: Port0 [7] ~ Port0[0]

Mnemonic: P1 **Address: 90h**

7	6	5	4	3	2	1	0	Reset
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh

P1.7~ 0: Port1 [7] ~ Port1 [0]

Mnemonic: P2 **Address: A0h**

7	6	5	4	3	2	1	0	Reset
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	7Fh

P2.7~ 0: Port2 [7] ~ Port2 [0]

Mnemonic: P3 **Address: B0h**

7	6	5	4	3	2	1	0	Reset
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	7Fh

P3.7~ 0: Por3 [7] ~ Port3 [0]

Mnemonic: P4 **Address: E8h**

7	6	5	4	3	2	1	0	Reset
P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	FFh

P4.7~ 0: Port4 [7] ~ Port4 [0]

Mnemonic: P5 **Address: D8h**

7	6	5	4	3	2	1	0	Reset
P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0	FFh

P5.7~ 0: Port5 [7] ~ Port5 [0]

Mnemonic: P6 **Address: 96h**

7	6	5	4	3	2	1	0	Reset
P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0	FFh

P6.7~ 0: Port6 [7] ~ Port6 [0]

Mnemonic: P7 **Address: E9h**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	P7.2	P7.1	P7.0	07h

P7.2~ 0: Port7 [2] ~ Port7 [0]

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS		-	-	-	-		DPS	00H

To disable IO input buffer and set Hi-Z to related PAD for VDCIN low detection.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Ports											
PDP7	Power down port 7	AFh	-	-	-	-	-	PDP7.2	PDP7.1	PDP7.0	00h
PDP6	Power down port 6	BFh	PDP6.7	PDP6.6	PDP6.5	PDP6.4	PDP6.3	PDP6.2	PDP6.1	PDP6.0	00h
PDP5	Power down port 5	BEh	PDP5.7	PDP5.6	PDP5.5	PDP5.4	PDP5.3	PDP5.2	PDP5.1	PDP5.0	00h
PDP4	Power down port 4	BDh	PDP4.7	PDP4.6	PDP4.5	PDP4.4	PDP4.3	PDP4.2	PDP4.1	PDP4.0	00h
PDP3	Power down port 3	A7h	PDP3.7	PDP3.6	PDP3.5	PDP3.4	PDP3.3	PDP3.2	PDP3.1	PDP3.0	00h
PDP2	Power down port 2	A6h	PDP2.7	PDP2.6	PDP2.5	PDP2.4	PDP2.3	PDP2.2	PDP2.1	PDP2.0	00h
PDP1	Power down port 1	A5h	PDP1.7	PDP1.6	PDP1.5	PDP1.4	PDP1.3	PDP1.2	PDP1.1	PDP1.0	00h
PDP0	Power down port 0	A4h	PDP0.7	PDP0.6	PDP0.5	PDP0.4	PDP0.3	PDP0.2	PDP0.1	PDP0.0	00h

Mnemonic: PDP0 **Address: A4h**

7	6	5	4	3	2	1	0	Reset
PDP0.7	PDP0.6	PDP0.5	PDP0.4	PDP0.3	PDP0.2	PDP0.1	PDP0.0	00h

PDP0.7~ 0: To disable IO input buffer and set Hi-Z to Port0 [7] ~ Port0[0]

Mnemonic: PDP1 **Address: A5h**

7	6	5	4	3	2	1	0	Reset
PDP1.7	PDP1.6	PDP1.5	PDP1.4	PDP1.3	PDP1.2	PDP1.1	PDP1.0	00h

PDP1.7~ 0: To disable IO input buffer and set Hi-Z to Port1 [7] ~ Port1 [0]

Mnemonic: PDP2 **Address: A6h**

7	6	5	4	3	2	1	0	Reset
PDP2.7	PDP2.6	PDP2.5	PDP2.4	PDP2.3	PDP2.2	PDP2.1	PDP2.0	00h

PDP2.7~ 0: To disable IO input buffer and set Hi-Z to Port2 [7] ~ Port2 [0]

Mnemonic: PDP3 **Address: A7h**

7	6	5	4	3	2	1	0	Reset
PDP3.7	PDP3.6	PDP3.5	PDP3.4	PDP3.3	PDP3.2	PDP3.1	PDP3.0	00h

PDP3.7~ 0: To disable IO input buffer and set Hi-Z to Port3[7]~Port3[0]

Mnemonic: PDP4 **Address: BDh**

7	6	5	4	3	2	1	0	Reset
PDP4.7	PDP4.6	PDP4.5	PDP4.4	PDP4.3	PDP4.2	PDP4.1	PDP4.0	00h

PDP4.7~ 0: To disable IO input buffer and set Hi-Z to Port4[7]~Port4[0]

Mnemonic: PDP5 **Address: BEh**

7	6	5	4	3	2	1	0	Reset
PDP5.7	PDP5.6	PDP5.5	PDP5.4	PDP5.3	PDP5.2	PDP5.1	PDP5.0	00h

PDP5.7~ 0: To disable IO input buffer and set Hi-Z to Port5[7]~Port5[0]

Mnemonic: PDP6 **Address: BFh**

7	6	5	4	3	2	1	0	Reset
PDP6.7	PDP6.6	PDP6.5	PDP6.4	PDP6.3	PDP6.2	PDP6.1	PDP6.0	00h

PDP6.7~ 0: To disable IO input buffer and set Hi-Z to Port6[7]~Port6[0]

Mnemonic: PDP7 **Address: AFh**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	PDP7.2	PDP7.1	PDP7.0	00h

PDP7.3~ 0: To disable IO input buffer and set Hi-Z to Port7[2]~Port7[0]

6. Multiplication Division unit

This on-chip arithmetic unit provides 32-bit division, 16-bit multiplication, shift and normalize features. All operations are unsigned integer operation.

Table 6-1 Multiplication Division Register

Mnemonic	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Multiplication Division Unit											
PCON	Power control	87H	SMOD	MDUF	-	VDCIS	PDALDO3	PDLDO3	STOP	IDLE	40H
ARCON	Arithmetic Control register	EFh	MDEF	MDOV	SLR	SC[4:0]					00H
MD0	Multiplication/Division Register 0	E9h	MD0[7:0]								00H
MD1	Multiplication/Division Register 1	EAh	MD1[7:0]								00H
MD2	Multiplication/Division Register 2	EBh	MD2[7:0]								00H
MD3	Multiplication/Division Register 3	ECh	MD3[7:0]								00H
MD4	Multiplication/Division Register 4	EDh	MD4[7:0]								00H
MD5	Multiplication/Division Register 5	EEh	MD5[7:0]								00H

6.1 Operation of the MDU

The MDU is handled by eight registers, which are memory mapped as special function registers. The arithmetic unit allows operations concurrently to and independent of the CPU's activity. Operands and results registers are MD0 to MD5. Control register is ARCON. Any calculation of the MDU overwrites its operands.

1 Mnemonic: ARCON **2 Address: EFh**

7	6	5	4	3	2	1	0	Reset
MDEF	MDOV	SLR	SC[4:0]					00H

MDEF- Multiplocation Division Errot Flag.

The MDEF is an error flag. The error flag is read only. The error flag indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation). The error flag mechanism is automatically enabled with the first write to MD0 and disabled with the final read instruction from MD3 multiplication or shift/normalizing) or MD5 (division) in phase three.

The error flag is set when:

Phase two in process and write access to mdx registers (restart or interrupt calculations)

The error flag is reset only if:

Phase two finished (arithmetic operation successful completed) and read access to MDx registers.

MDOV - Multiplication Division Overflow flag. The overflow flag is read only.

The overflow flag is set when:

Division by Zero

Multiplication with a result greater then 0000FFFFh

Start of normalizing if the most significant bit of MD3 is set(MD3.7 = 1)

The overflow flag is reset when:

Write access to MD0 register (Start Phase one)

SLR - Shift direction bit.

SLR = 0 – shift left operation.

SLR = 1 – shift right operation.

SC[4:0] - Shift counter.

When preset with 00000b, normalizing is selected. After normalize sc.0 – sc.4 contains the number of normalizing shifts performed. When sc.4 – sc.0 ≠ 0, shift- operation is started. The number of shifts performed is determined by the count written to sc.4 to sc.0. sc.4 – MSB ... sc.0 – LSB

6.2 Operation of the MDU

Operations of the MDU consist of three phases:

6.2.1 First phase: Loading the MDx registers.

The type of calculation the MDU has to perform is selected following the order in which the mdx registers are written to.

Table 6-1 MDU registers write sequence

Operation	32bit/16bit	16bit/16bit	16bit x 16bit	shift/normalizing
First write	MD0 Dividend Low	MD0 Dividend Low	MD0 Multiplicand Low	MD0 LSB
	MD1 Dividend	MD1 Dividend High	MD4 Multiplicator Low	MD1
	MD2 Dividend		MD1 Multiplicand High	MD2
	MD3 Dividend High			MD3 MSB
	MD4 Divisor Low	MD4 Divisor Low		
Last write	MD5 Divisor High	MD5 Divisor High	MD5 Multiplicator High	ARCON start conversion

A write to md0 is the first transfer to be done in any case. Next writes must be done as shown in Table 6- to determine MDU operation. Last write finally starts selected operation.

6.2.2 Second phase: Executing calculation.

During executing operation, the MDU works on its own parallel to the CPU. When MDU is finished, the MDUF register will be set to one by hardware and the flag will clear at next calculation.

Mnemonic: PCON **Address: 87h**

7	6	5	4	3	2	1	0	Reset
SMOD	MDUF		VDCIS	PDAL DO3	PDLD O3	STOP	IDLE	40H

MDUF: MDU finish flag.

When MDU is finished, the MDUF will be set by hardware and the bit will clear by hardware at next calculation.

Table 6-2 MDU execution times

Operation	Number of Tclk
Division 32bit/16bit	17 clock cycles
Division 16bit/16bit	9 clock cycles
Multiplication	11 clock cycles

Shift	min 3 clock cycles , max 18 clock cycles
Normalize	min 4 clock cycles , max 19 clock cycles

6.2.1 Third phase: Reading the result from the MDx registers.

Read out sequence of the first MDx registers is not critical but the last read (from MD5 - division and MD3 - multiplication, shift and normalizing) determines the end of a whole calculation (end of phase three).

Table 6-3 MDU registers read sequence

Operation	32Bit/16Bit	16Bit/16Bit	16Bit x 16Bit	shift/normalizing
First read	MD0 Quotient Low	MD0 Quotien Low	MD0 Product Low	MD0 LSB
	MD1 Quotient	MD1 Quotien High	MD1 Product	MD1
	MD2 Quotient		MD2 Product	MD2
	MD3 Quotient High			
	MD4 Remainder L	MD4 Remainder Low		
Last read	MD5 Remainder H	MD5 Remainder High	MD3 Product High	MD3 MSB

6.3 Normalizing

All reading zeroes of integers variables in registers MD0 to MD3 are removed by shift left operations. The whole operation is completed when the MSB (most significant bit) of MD3 register contains a '1'. After normalizing, bits ARCON.4 (MSB) to ARCON.0 (LSB) contain the number of shift left operations, which were done.

6.4 Shifting

SLR bit (ARCON.5) has to contain the shift direction, and ARCON.4 to ARCON.0 the shift count (which must not be 0). During shift, zeroes come into the left or right end of the registers MD0 or MD3, respectively.

7. Timer 0 and Timer 1

The OB59A128A1 has three 16-bit timer/counter registers: Timer 0, Timer 1 and Timer 2. All can be configured for counter or timer operations.

In timer mode, the Timer 0 register or Timer 1 register is incremented every 1/12/96 machine cycles, which means that it counts up after every 1/12/96 periods of the clk signal. It's dependent on SFR(PFCON).

In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function registers (TMOD and TCON) are used to select the appropriate mode.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Timer 0 and 1											
TL0	Timer 0 , low byte	8Ah	TL0[7:0]								00H
TH0	Timer 0 , high byte	8Ch	TH0[7:0]								00H
TL1	Timer 1 , low byte	8Bh	TL1[7:0]								00H
TH1	Timer 1 , high byte	8Dh	TH1[7:0]								00H
TMOD	Timer Mode Control	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
TCON	Timer/Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
PFCON	Peripheral Frequency control register	D9h	-	-	-	-	T1PS[1:0]		T0PS[1:0]		00H

7.1 Timer/counter control register (TMOD)

Mnemonic: TMOD **Address: 89h**

7	6	5	4	3	2	1	0	Reset
GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
Timer 1				Timer 0				

GATE: If set, enables external gate control (pin INT0 or INT1 for Counter 0 or 1, respectively). When INT0 or INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on T0 or T1 input pin.

C/T: Selects Timer or Counter operation. When set to 1, a counter operation is performed, when cleared to 0, the corresponding register will function as a timer.

M1	M0	Mode	Function
0	0	Mode0	13-bit counter/timer, with 5 lower bits in TL0 or TL1 register and 8 bits in TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are hold at zero.
0	1	Mode1	16-bit counter/timer.
1	0	Mode2	8-bit auto-reload counter/timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.

1	1	Mode3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8 bit timers / counters.

7.2 Timer/counter control register (TCON)

Mnemonic: TCON0 **Address: 88h**

7	6	5	4	3	2	1	0	Reset
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

TF1: Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR1: Timer 1 Run control bit. If cleared, Timer 1 stops.

TF0: Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR0: Timer 0 Run control bit. If cleared, Timer 0 stops.

IE1: Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.

IT1: IT1=0: INT1 select level trigger.(high or low dependent on ENHIT1)
IT1=1: INT1 select edge trigger.(falling or rising or both edge dependent on ENHIT1).

IE0: Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT0 is observed. Cleared when interrupt is processed.

IT0: IT0=0: INT0 select level trigger.(high or low dependent on ENHIT0)
IT0=1: INT0 select edge trigger.(falling or rising or both edge dependent on ENHIT0)

7.3 Peripheral Frequency control register

Mnemonic: PFCON **Address: D9h**

7	6	5	4	3	2	1	0	Reset
-	-			T1PS[1:0]		T0PS[1:0]		00H

T1PS[1:0]: Timer1 Prescaler select

T1PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

T0PS[1:0]: Timer0 Prescaler select

T0PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

7.4 Mode 0 (13-bit Counter/Timer)

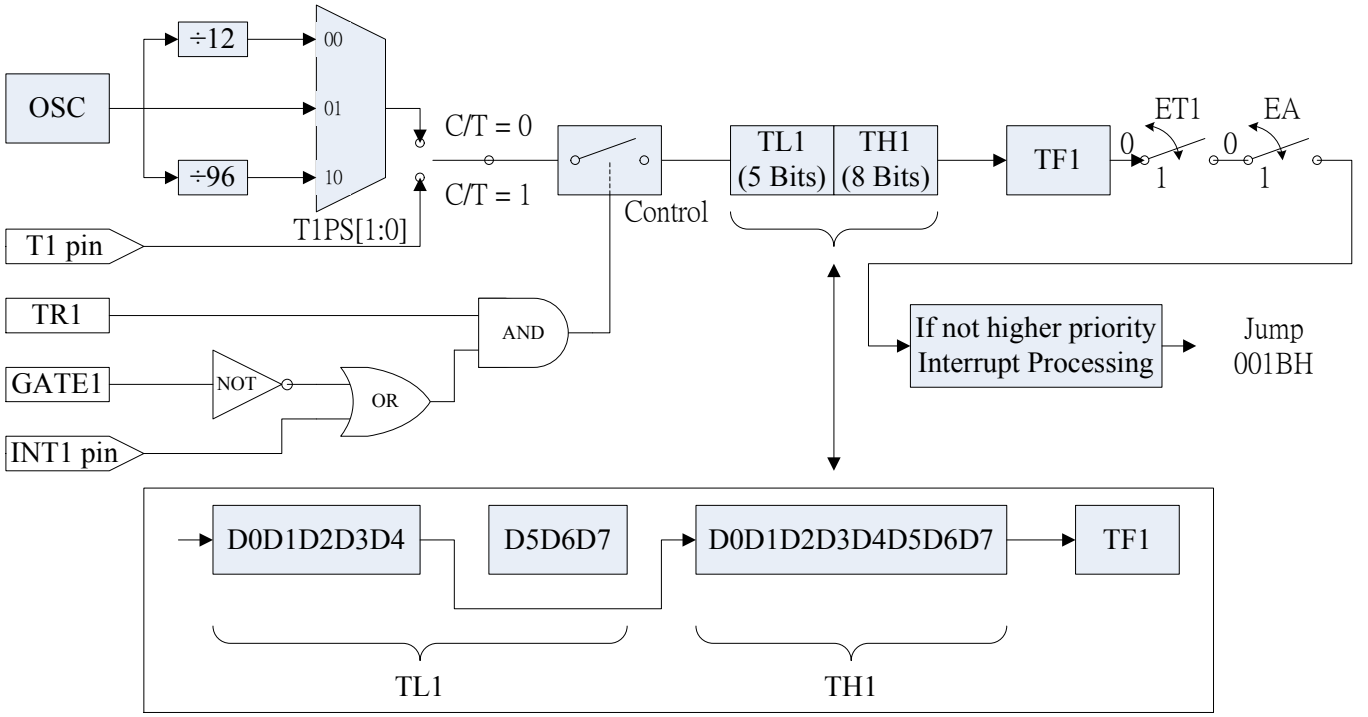


Fig. 7-1: Mode 0 -13 bit Timer / Counter operation

7.5 Mode 1 (16-bit Counter/Timer)

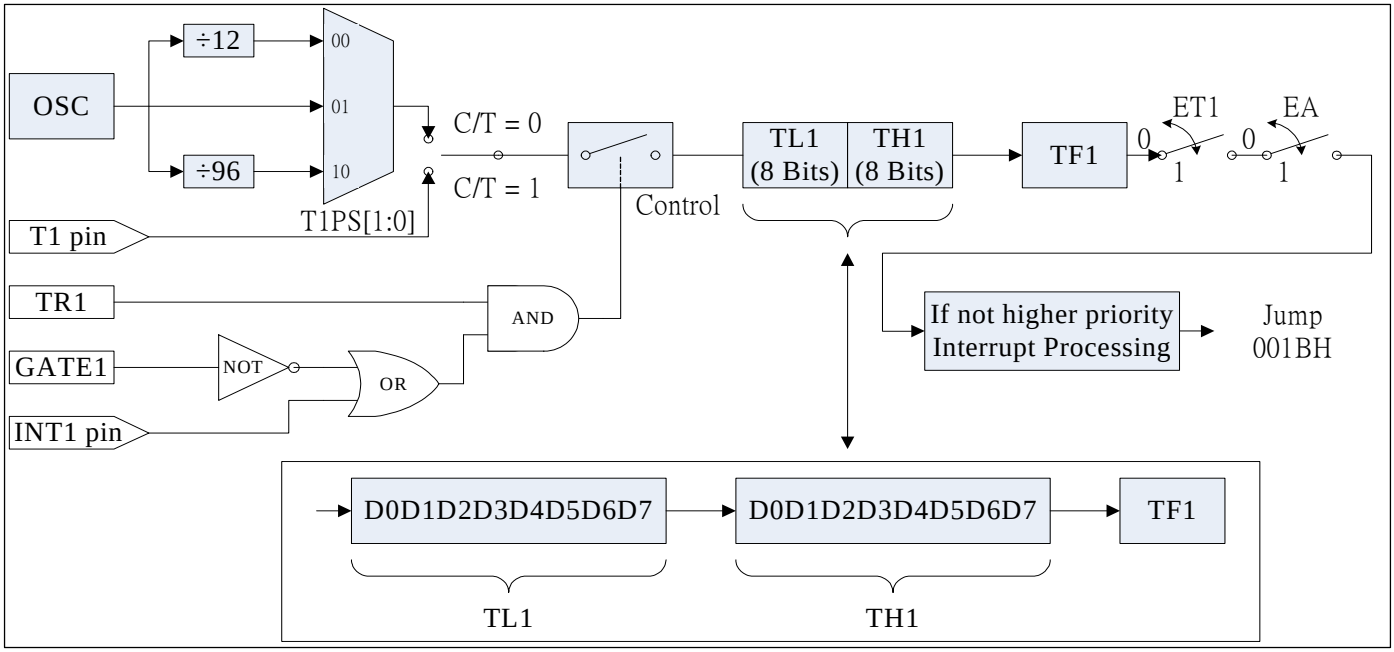


Fig. 7-2: Mode 1 16 bit Counter/Timer operation

7.6 Mode 2 (8-bit auto-reload Counter/Timer)

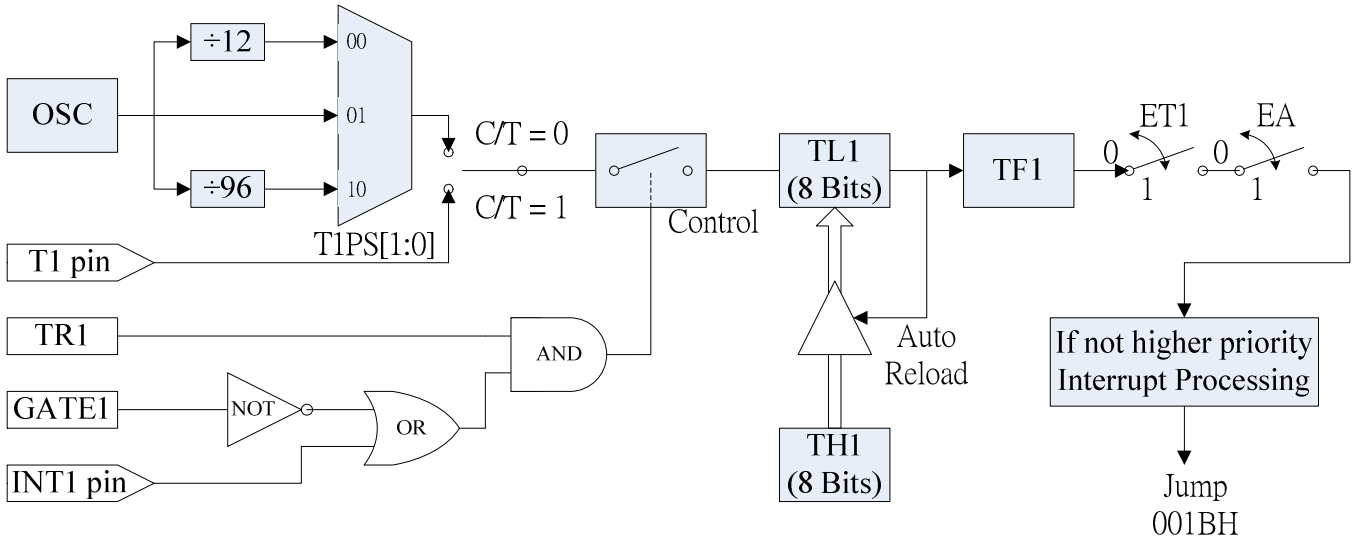


Fig. 7-3: Mode 2 8-bit auto-reload Counter/Timer operation.

7.7 Mode 3 (Timer 0 acts as two independent 8 bit Timers / Counters)

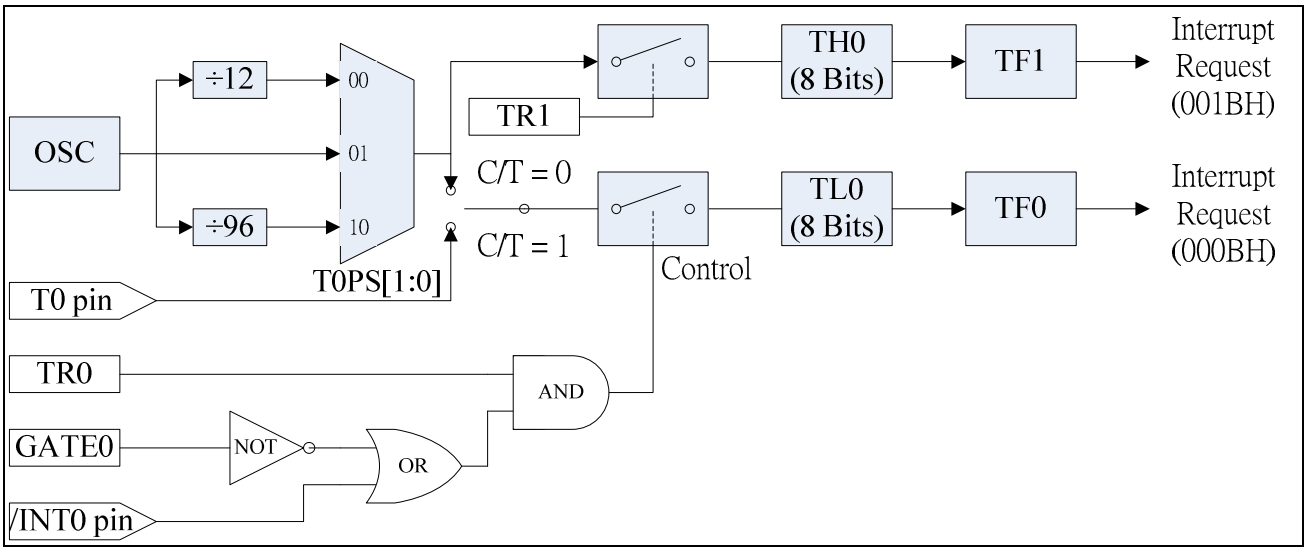
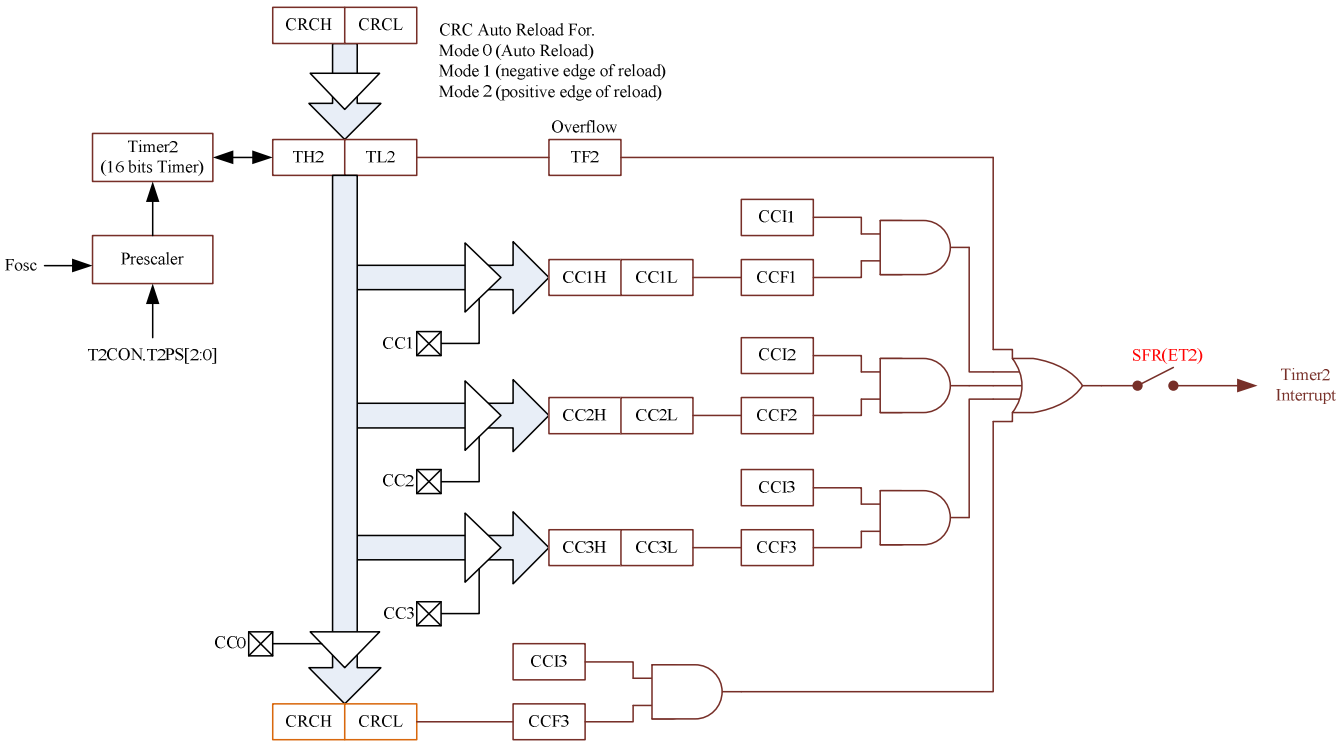


Fig. 7-4: Mode 3 Timer 0 acts as two independent 8 bit Timers / Counters operatin

8. Timer 2 and Capture Compare Unit

Timer 2 is not only a 16-bit timer, also a 4-channel unit with compare, capture and reload functions. It is very similar to the programmable counter array (PCA) in some other MCUs except pulse width modulation (PWM).



Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Timer 2 and Capture Compare Unit											
AUX2	Auxiliary 2 register	92h	CCU3 Source	CCU2 Source	CCU1 Source		CCUINF[1:0]		CCUINFCLK[1:0]		00H
T2CON	Timer 2 control	C8h	T2PS[2:0]			T2R[1:0]		T2CS	T2I[1:0]		00H
CCCON	Compare/Capture Control	C9h	CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H
CCEN	Compare/Capture Enable register	C1h	-	COCAM1[2:0]			-	COCAM0[2:0]			00H
CCEN2	Compare/Capture Enable 2 register	D1h	-	COCAM3[2:0]			-	COCAM2[2:0]			00H
TL2	Timer 2, low byte	CCh	TL2[7:0]								00H
TH2	Timer 2, high byte	CDh	TH2[7:0]								00H
CRCL	Compare/Reload/ Capture register, low byte	CAh	CRCL[7:0]								00H
CRCH	Compare/Reload/ Capture register, high byte	CBh	CRCH[7:0]								00H
CCL1	Compare/Capture register 1, low byte	C2h	CCL1[7:0]								00H
CCH1	Compare/Capture register 1, high byte	C3h	CCH1[7:0]								00H
CCL2	Compare/Capture	C4h	CCL2[7:0]								00H

	register 2, low byte			
CCH2	Compare/Capture register 2, high byte	C5h	CCH2[7:0]	00H
CCL3	Compare/Capture register 3, low byte	C6h	CCL3[7:0]	00H
CCH3	Compare/Capture register 3, high byte	C7h	CCH3[7:0]	00H

Mnemonic: AUX2 **Address: 92h**

7	6	5	4	3	2	1	0	Reset
CCU3 Source	CCU2 Source	CCU1 Source		CCUINF[1:0]		CCUINFCLK[1:0]		00H

CCU3: Capture input source 3:

CCU3 = 0 - external Pin to be CCU3 capture input source

CCU3 = 1 - analog comparator 2 output to be CCU3 capture input source.

CCU2: Capture input source 2:

CCU2 = 0 - external Pin to be CCU2 capture input source

CCU2 = 1 - analog comparator 1 output to be CCU2 capture input source

CCU1: Capture input source 1:

CCU1= 0 - external Pin to be CCU1 capture input source

CCU1=1 - analog comparator 0 output to be CCU1 capture input source

CCUINF[1:0] CCU capture input Noise Filter(CCU1,CCU2,CCU3):

: CCUINF[1:0] = 00 - 1 consecutive same value recognize as valid data.

CCUINF[1:0] = 01 - 2 consecutive same value recognize as valid data.

CCUINF[1:0] = 10 - 4 consecutive same value recognize as valid data.

CCUINF[1:0] = 11 - 8 consecutive same value recognize as valid data.

CCUINFCLK[1:0] CCU capture input Noise Filter(CCU1,CCU2,CCU3) frequency select:

: CCUINFCLK[1:0] = 00 - Freq/1.

CCUINFCLK[1:0] = 01 - Freq/4.

CCUINFCLK[1:0] = 10 - Freq/8

CCUINFCLK[1:0] = 11 - Freq/1.6

Mnemonic: T2CON **Address: C8h**

7	6	5	4	3	2	1	0	Reset
T2PS[2:0]			T2R[1:0]			T2I[1:0]		00H

T2PS[2:0]: Prescaler select bit:

T2PS = 000 – timer 2 is clocked with the oscillator frequency.

T2PS = 001 – timer 2 is clocked with 1/2 of the oscillator frequency.

T2PS = 010 – timer 2 is clocked with 1/4 of the oscillator frequency.

T2PS = 011 – timer 2 is clocked with 1/6 of the oscillator frequency.

T2PS = 100 – timer 2 is clocked with 1/8 of the oscillator frequency.

T2PS = 101 – timer 2 is clocked with 1/12 of the oscillator frequency.

T2PS = 110 – timer 2 is clocked with 1/24 of the oscillator frequency.

T2R[1:0]: Timer 2 reload mode selection

T2R[1:0] = 00 – Reload disabled.

T2R[1:0] = 01 – Mode 2:T2EX Rising Edge Reload.

T2R[1:0] = 10 – Mode 0: Auto Reload.

T2R[1:0] = 11 – Mode 1: T2EX Falling Edge Reload.

T2I[1:0]: Timer 2 input selection

T2I[1:0] = 00 – Timer 2 stop.

T2I[1:0] = 01 – Input frequency from prescaler (T2PS[2:0]).

T2I[1:0] = 10 – Timer2 is incremented by external signal at pin T2.

T2I[1:0] = 11 – internal clock input is gated to the Timer 2.

Mnemonic: CCCON **Address: C9h**

7	6	5	4	3	2	1	0	Reset
CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H

CCI3: Compare/Capture 3 interrupt control bit.

CCI3 = 1 is enable.

CCI2: Compare/Capture 2 interrupt control bit.

CCI3 = 1 is enable.

CCI1: Compare/Capture 1 interrupt control bit.

CCI3 = 1 is enable.

CCI0: Compare/Capture 0 interrupt control bit.

CCI3 = 1 is enable.

CCF3: Compare/Capture 3 flag set by hardware. This flag can be cleared by software.

CCF2: Compare/Capture 2 flag set by hardware. This flag can be cleared by software.

CCF1: Compare/Capture 1 flag set by hardware. This flag can be cleared by software.

CCF0: Compare/Capture 0 flag set by hardware. This flag can be cleared by software.

Compare/Capture interrupt share T2 interrupt vector.

Mnemonic: CCEN **Address: C1h**

7	6 5 4	3	2 1 0	Reset
-	COCAM1[2:0]	-	COCAM0[2:0]	00H

COCAM1[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC1.

101 - Capture on falling edge at pin CC1.

110 - Capture on both rising and falling edge at pin CC1.

111 - Capture on write operation into register CC1.

COCAM0[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC0.

101 - Capture on falling edge at pin CC0.

110 - Capture on both rising and falling edge at pin CC0.

111 - Capture on write operation into register CC0.

Mnemonic: CCEN2 **Address: D1h**

7	6 5 4	3	2 1 0	Reset
-	COCAM3[2:0]	-	COCAM2[2:0]	00H

COCAM3[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC3.

101 - Capture on falling edge at pin CC3.

110 - Capture on both rising and falling edge at pin CC3.

111 - Capture on write operation into register CC3.

COCAM2[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC2.

101 - Capture on falling edge at pin CC2.

110 - Capture on both rising and falling edge at pin CC2.

111 - Capture on write operation into register CC2.

8.1 Timer 2 function

Timer 2 can operate as timer, event counter, or gated timer as explained later.

8.1.1 Timer mode

In this mode Timer 2 can by incremented in various frequency that depending on the prescaler. The prescaler is selected by bit T2PS[2:0] in register T2CON. As shown in Fig. 7-1

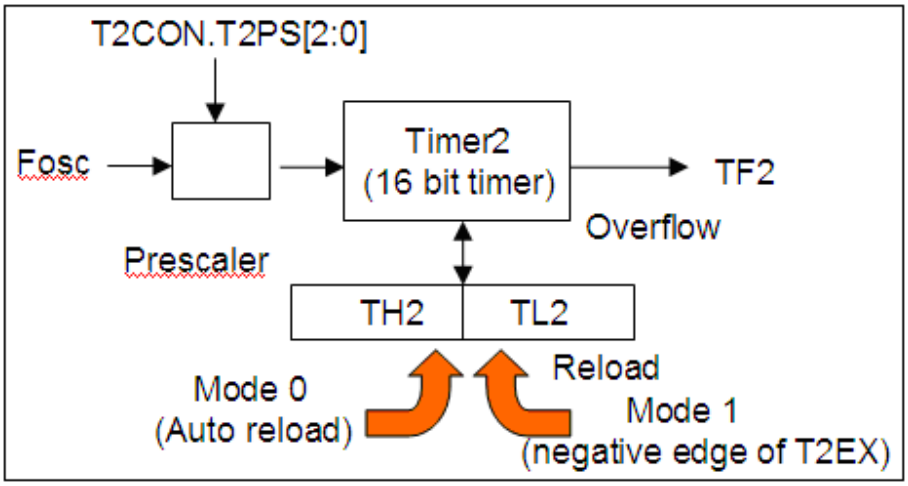


Fig. 9-1: Timer mode and Reload mode function

8.1.2 Event counter mode

In this mode, the timer is incremented when external signal T2 change value from 1 to 0. The T2 input is sampled in every cycle. Timer 2 is incremented in the cycle following the one in which the transition was detected. As shown in Fig. 9-2.

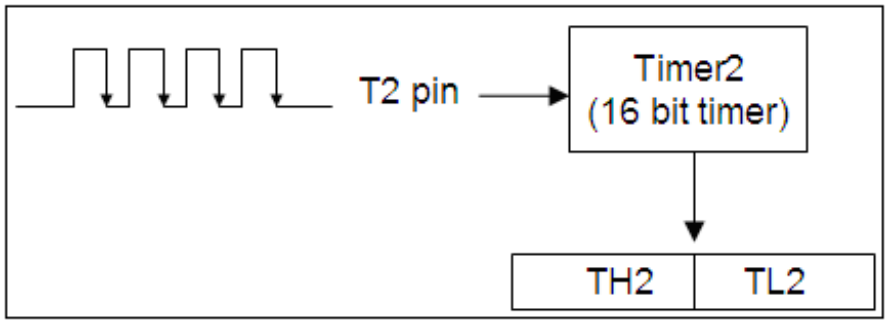


Fig. 9-2: Event counter mode function

8.1.3 Gated timer mode

In this mode, the internal clock which incremented timer 2 is gated by external signal T2. As shown in Fig. 9-3

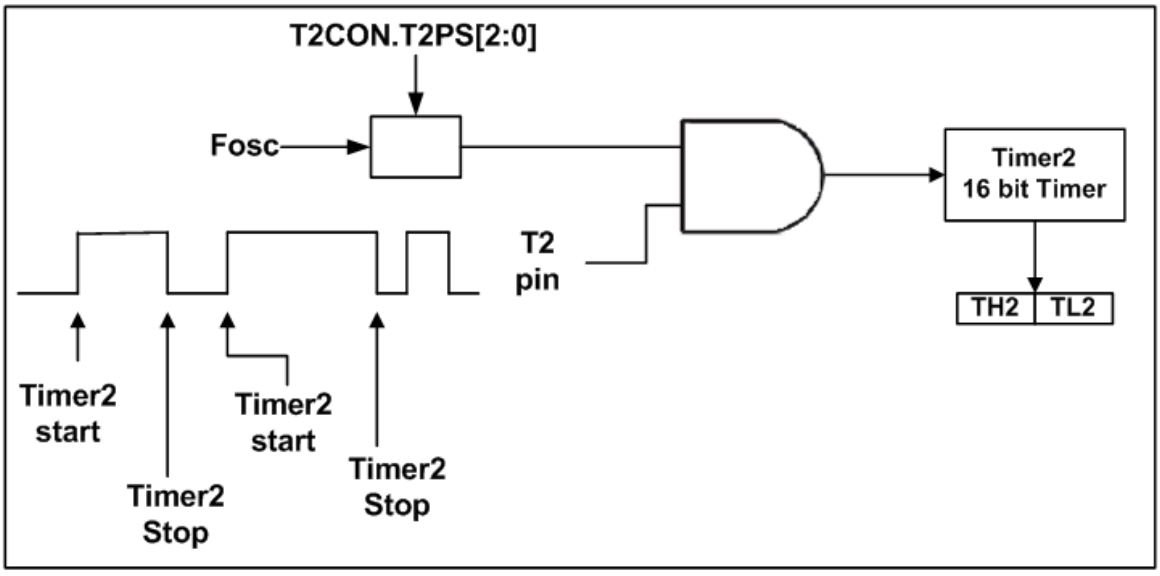


Fig. 9-3: Gated timer mode function

8.1.4 Reload of Timer 2

Reload (16-bit reload from the crc register) can be executed in the following two modes:

Mode 0: Reload signal is generate by a Timer 2 overflows – autoreload.

Mode 1: Reload signal is generate by a negative transition at the corresponding input pin T2EX.

8.2 Compare function

In the four independent comparators, the value stored in any compare/capture register is compared with the contents of the timer register. The compare modes 0 and 1 are selected by bits C0CAMx. In both compare modes, the results of comparison arrives at Port 1 within the same machine cycle in which the internal compare signal is activated.

8.2.1 Compare Mode 0

In mode 0, when the value in Timer 2 equals the value of the compare register, the output signal changes from low to high. It goes back to a low level on timer overflow. In this mode, writing to the port will have no effect, because the input line from the internal bus and the write-to-latch line are disconnected. As shown in Fig. 9-4 illustrates the function of compare mode 0.

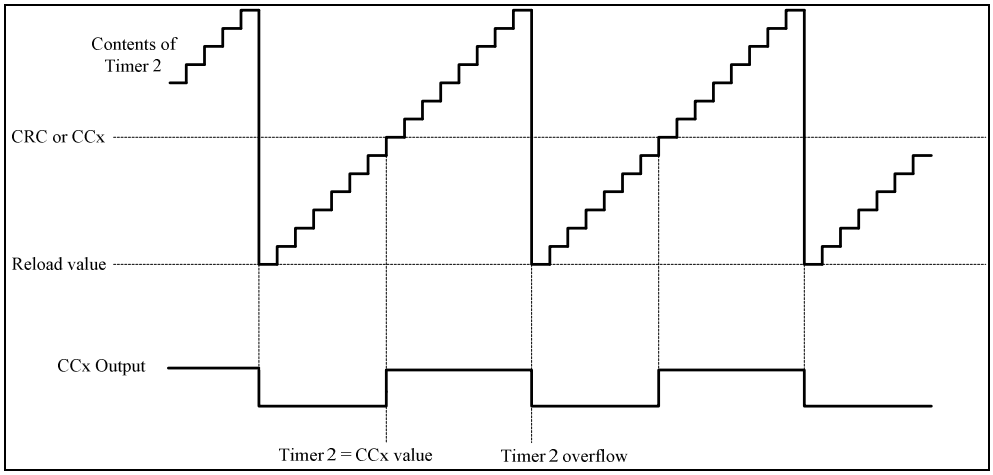


Fig. 9-4: Compare mode 0 function

8.2.2 Compare Mode 1

In compare mode 1, the transition of the output signal can be determined by software. A timer 2 overflow causes no output change. In this mode, both transitions of a signal can be controlled. As shown in Fig. 9-5 and Fig. 9-6 a functional diagram of a register/port configuration in compare Mode 1. In compare Mode 1, the value is written first to the “Shadow Register”, when compare signal is active, this value is transferred to the output register.

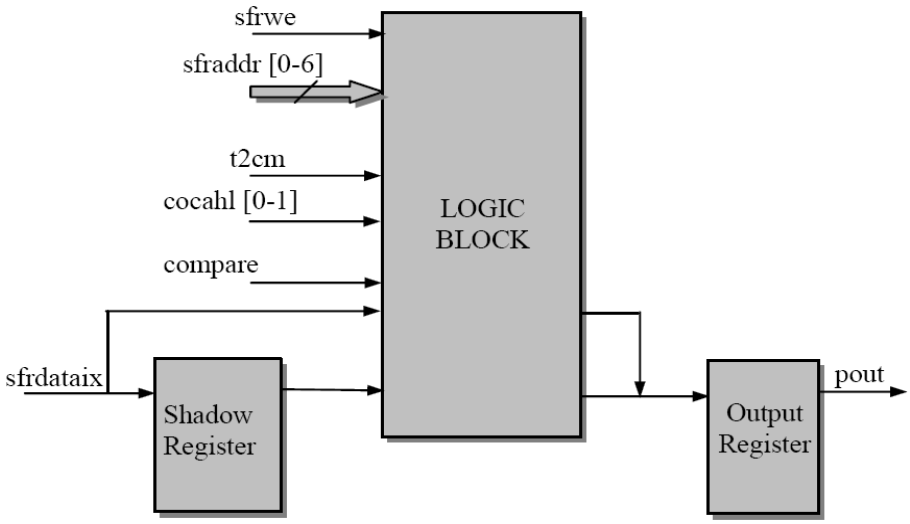


Fig. 9-5: Mode 1 Register/Port Function

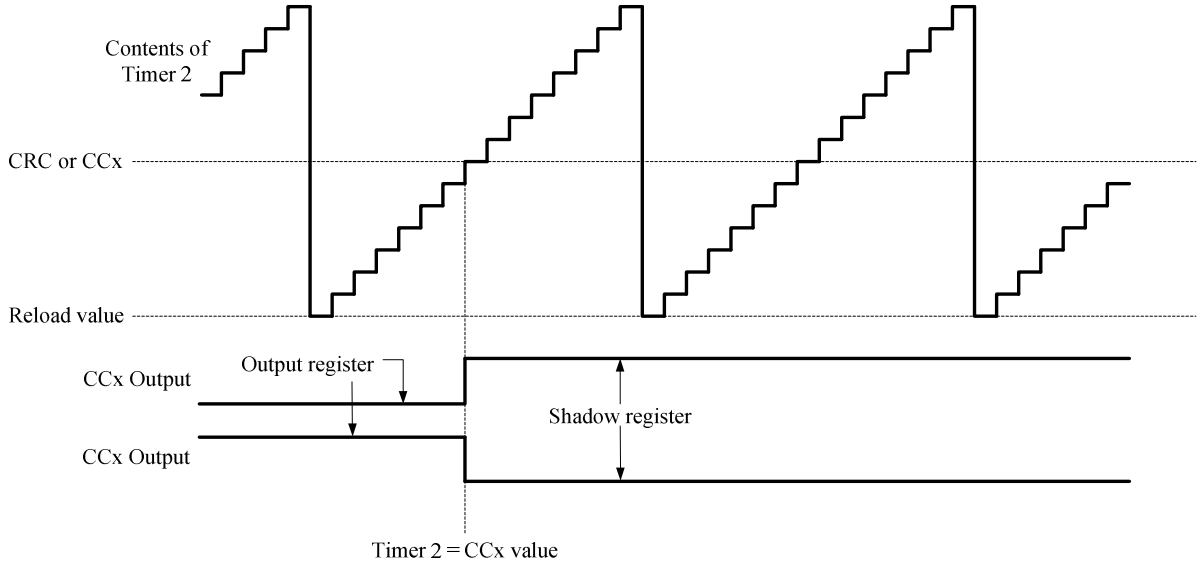


Fig. 9-6: Compare mode 1 function

8.3 Capture function

Actual timer/counter contents can be saved into registers CCx or CRC upon an external event (mode 0) or a software write operation (mode 1).

8.3.1 Capture Mode 0 (by Hardware)

In mode 0, value capture of Timer 2 is executed when:

(1) Rising edge on input CC0-CC3
(2) Falling edge on input CC0-CC3
(3) Both rising and falling edge on input CC0-CC3

The contents of Timer 2 will be latched into the appropriate capture register. As shown in Fig. 9-7

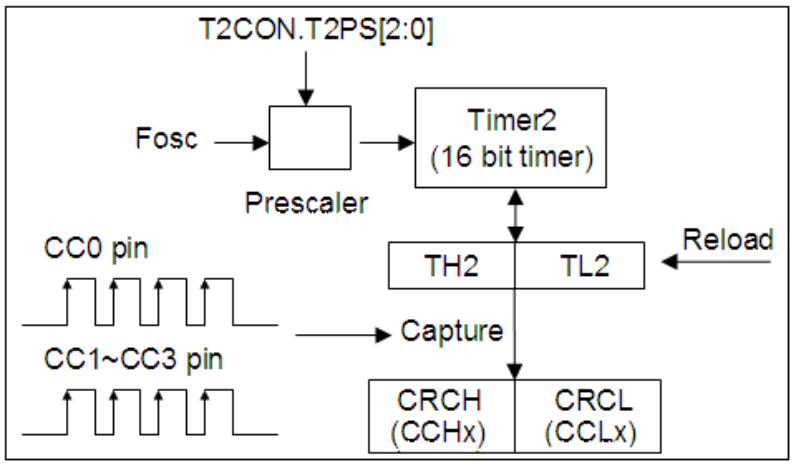


Fig. 9-7: Capture mode 0 function

8.3.2 Capture Mode 1(by Software)

In mode 1, value capture of timer 2 is caused by writing any value into the low-order byte of the dedicated capture register. The value written to the capture register is irrelevant to this function. The contents of Timer 2 will be latched into the appropriate capture register. As shown in Fig. 9-8

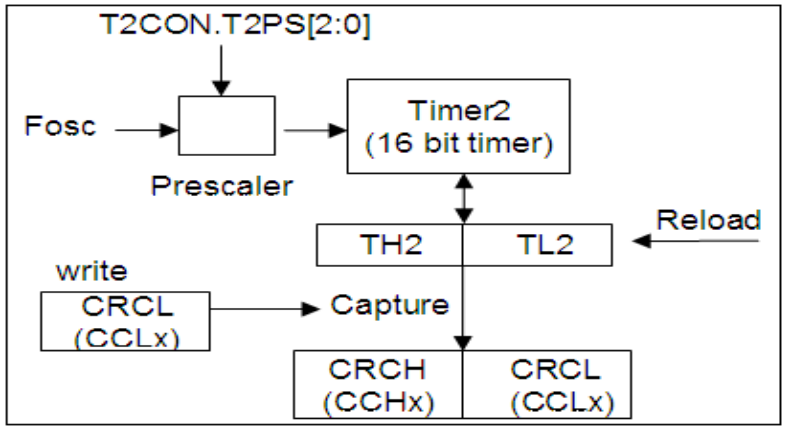


Fig. 9-8: Capture mode 1 function

9. Serial interface

There are two serial interfaces for data communication in OB59A128A1, they are the so called UART0 and UART1.

As the conventional UART, the communication speed can be selected by configuring the baud rate in SFRs.
These two serial buffers consists of two separate registers, a transmit buffer and a receive buffer. Writing data to the SFR S0BUF or S1BUF sets this data in serial output buffer and starts the transmission. Reading from the S0BUF or S1BUF reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the second byte before the transmission of the first byte is completed.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Serial interface 0											
PCON	Power control	87h	SMOD	MDUF	-	VDCIS	PDALDO3	PDLDO3-	STOP	IDLE	00H
AUX	Auxiliary register	91h	BRGS	P2IIC	-	-	-	-	P42S3	DPS	00H
S0CON	Serial port-0 control register	98h	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
S0RELL	Serial port-0 reload register low byte	AAh	S0REL[7:0]								00H
S0RELH	Serial port-0 reload register high byte	BAh	-	-	-	-	-	-	S0REL[9:8]		00H
S0BUF	Serial port-0 data buffer	99h	S0BUF[7:0]								00H
Serial interface 1											
S1CON	Serial port-1 control register	DCh	S1M		S1M2	REN1	TB81	RB81	TI1	RI1	00H
S1RELL	Serial port-1 reload register low byte	DEh	S1REL[7:0]								00H
S1RELH	Serial port-1 reload register high byte	DFH	-	-	-	-	-	-	S1REL[9:8]		00H
S1BUF	Serial port-1 data buffer	DDh	S1BUF[7:0]								00H
Serial interface 2											
S2CON	Serial port-2 control register	93h	S2M		S2M2	REN2	TB82	RB82	TI2	RI2	00H
S2RELL	Serial port-2 reload register low byte	95h	S2REL.7	S2REL.6	S2REL.5	S2REL.4	S2REL.3	S2REL.2	S2REL.1	S2REL.0	00H
S2RELH	Serial port-2 reload register high byte	BCh	-	-	-	-	-	-	S2REL.9	S2REL.8	00H
S2BUF	Serial port-2 data buffer	94h	S2BUF[7:0]								00H
Serial interface 3											
S3CON	Serial port-3 control register	B1h	S3M		S3M2	REN3	TB83	RB83	TI3	RI3	00H
S3RELL	Serial port-3 reload register low byte	B3h	S3REL.7	S3REL.6	S3REL.5	S3REL.4	S3REL.3	S3REL.2	S3REL.1	S3REL.0	00H
S3RELH	Serial port-3 reload register high byte	B4h							S3REL.9	S3REL.8	00H
S3BUF	Serial port-3 data buffer	B2h	S3BUF[7:0]								00H

9.1 Serial interface 0

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	P2IIC	-	-	-	-	P42S3	DPS	00H

BRGS: Baud rate generator.

BRGS = 0 - baud rate generator from Timer 1.

BRGS = 1 - baud rate generator by S0REL.

Mnemonic: S0CON **Address: 98h**

7	6	5	4	3	2	1	0	Reset
SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H

SM0, SM1: Serial Port 0 mode selection.

SM0	SM1	Mode
0	0	0
0	1	1
1	0	2
1	1	3

The 4 modes in UART, Mode 0 ~ 3, are explained later.

SM2: Enables multiprocessor communication feature

REN: If set, enables serial reception. Cleared by software to disable reception.

TB8: The 9th transmitted data bit in modes 2 and 3. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB8: In modes 2 and 3, it is the 9th data bit received. In mode 1, if SM2 is 0, RB8 is the stop bit. In mode 0, this bit is not used. Must be cleared by software.

TI: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

The Serial Interface 0 can operate in the following 4 modes:

SM0	SM1	Mode	Description	Board Rate
0	0	0	Shift register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Variable

Here Fosc is the crystal or oscillator frequency.

9.1.1 Mode 0

Pin RXD0 serves as input and output. TXD0 outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI = 0 and REN = 1. In other modes, a start bit when REN = 1 starts receiving serial data. As shown in **錯誤! 找不到參照來源。** and **錯誤! 找不到參照來源。**

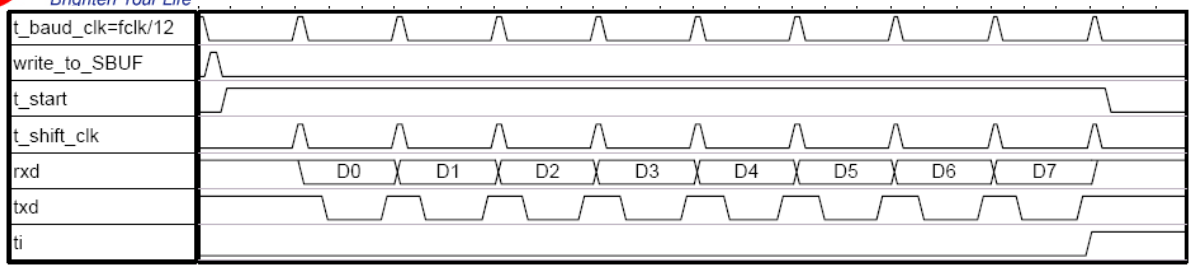


Fig.10-1:Transmit mode 0

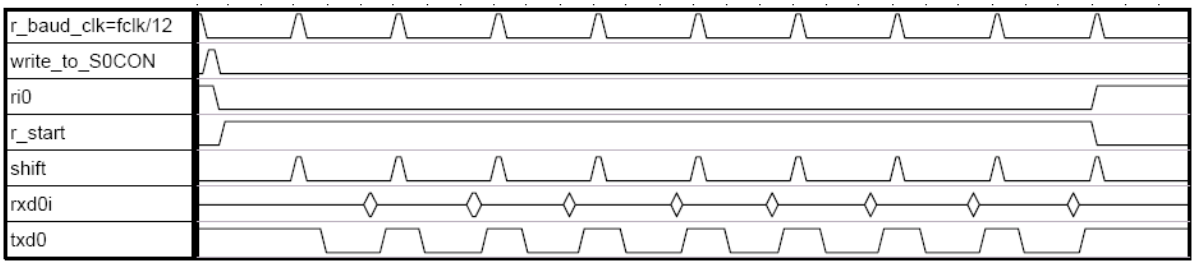


Fig.10-1: Receive mode 0

9.1.2 Mode 1

Pin RXD0 serves as input, and TXD0 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading SBUF, and stop bit sets the flag RB8 in the Special Function Register S0CON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate. As shown in **錯誤! 找不到參照來源。** and **錯誤! 找不到參照來源。**

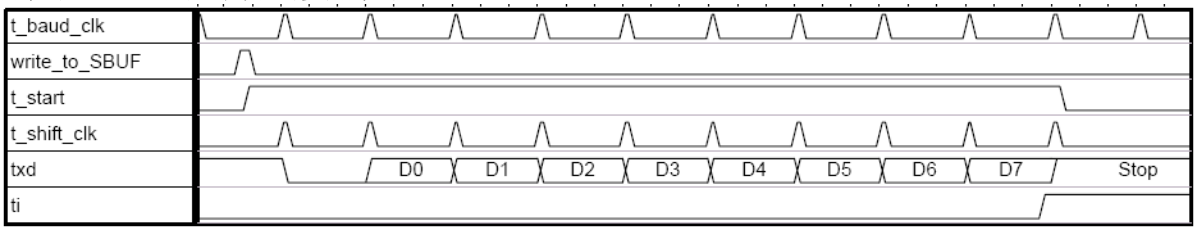


Fig.10-2: Transmit mode 1

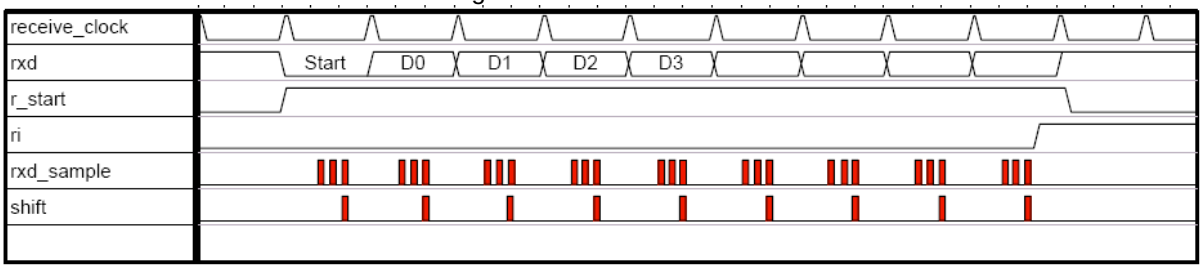


Fig.10-3: Receive mode 1

9.1.3 Mode 2

This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 (SMOD=1) or 1/64(SMOD=0) of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB8 in S0CON is output as the 9th bit, and at receive, the 9th bit affects RB8 in Special Function Register S0CON.

9.1.4 Mode 3

The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be use to specify baud rate. As shown in 錯誤! 找不到參照來源。 and 錯誤! 找不到參照來源。.

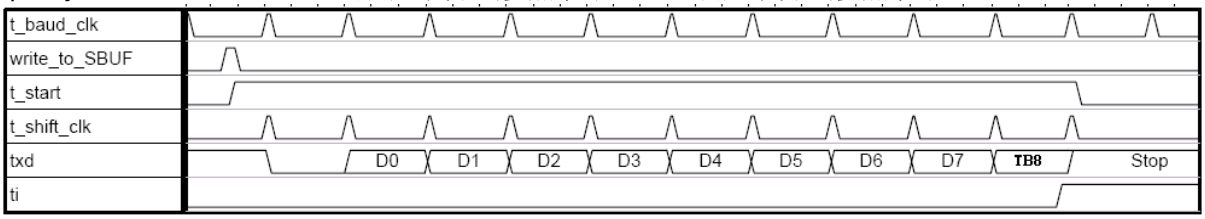


Fig.10-4: Transmit modes 2 and 3

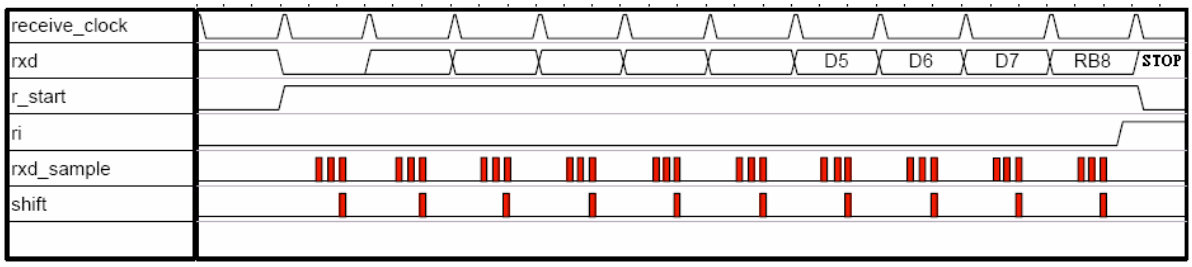


Fig.10-5: Receive modes 2 and 3

9.1.5 Multiprocessor Communication of Serial Interface

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface can be used for multiprocessor communication. In this case, the slave processors have bit SM2 in S0CON set to 1. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear SM2 and receive the rest of the message, while other slaves will leave SM2 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

9.1.6 Peripheral Frequency control register

Mnemonic: PFCON **Address: D9h**

7	6	5	4	3	2	1	0	Reset
-	-			T1PS[1:0]		T0PS[1:0]		00H

T1PS[1:0]: Timer1 Prescaler select

T1PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

9.1.7 Baud rate generator

Serial interface modes 1 and 3

9.1.7.1 When BRGS = 0 (in Special Function Register AUX).

(1) T1PS[1:0] is 00

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{\text{osc}}}{32 \times 12 \times (256 - \text{TH1})}$$

(2) T1PS[1:0] is 01

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{\text{osc}}}{32 \times (256 - \text{TH1})}$$

(3) T1PS[1:0] is 10

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{\text{osc}}}{32 \times 96 \times (256 - \text{TH1})}$$

9.1.7.2 When BRGS = 1 (in Special Function Register AUX).

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times F_{\text{clk}}}{64 \times (2^{10} - \text{S0REL})}$$

9.2 Serial interface 1

Mnemonic: S1CON **Address: 9Bh**

7	6	5	4	3	2	1	0	Reset
S1M	-	S1M2	REN1	TB81	RB81	TI1	RI1	00H

S1M: Serial Port 1 mode selection.

S1M	Mode
0	A
1	B

S1M2: Enables multiprocessor communication feature

REN1: If set, enables serial reception. Cleared by software to disable reception.

TB81: The 9th transmitted data bit in modes A. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB81: In modes A, it is the 9th data bit received. In mode B, if S1M2 is 0, RB81 is the stop bit. Must be cleared by software.

TI1: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI1: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

The Serial Interface 1 can operate in the following 2 modes:

S1M	Mode	Description	Board Rate
0	A	9-bit UART	Variable
1	B	8-bit UART	Variable

9.2.1 Mode A

This mode is similar to Mode 2 and 3 of Serial interface 0, 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB81 in S1CON is outputted as the 9th bit, and at receive, the 9th bit affects RB81 in Special Function Register S1CON.

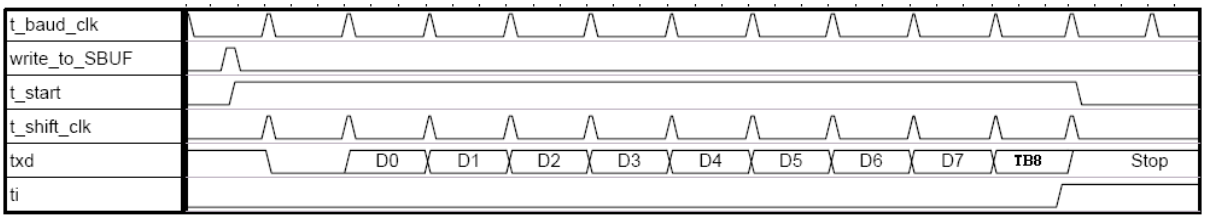


Fig.10-7: Transmit mode A

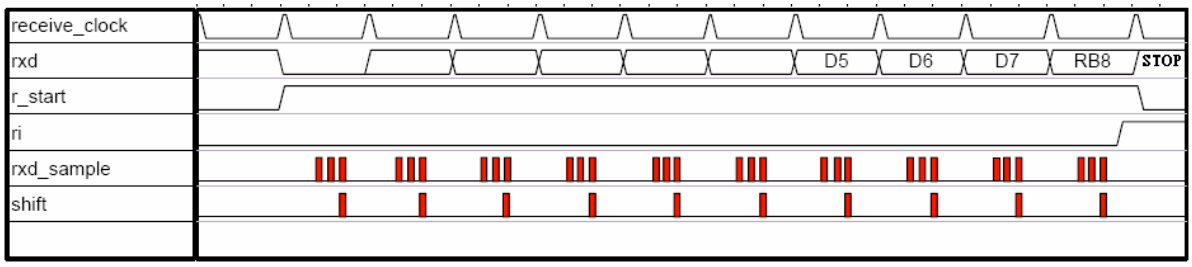


Fig.10-8: Receive mode A

9.2.2 Mode B

This mode is similar to Mode 1 of Serial interface 0. Pin RXD1 serves as input, and TXD1 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S1BUF, and stop bit sets the flag RB81 in the Special Function Register S1CON. In mode B internal baud rate generator is use to specify the baud rate.

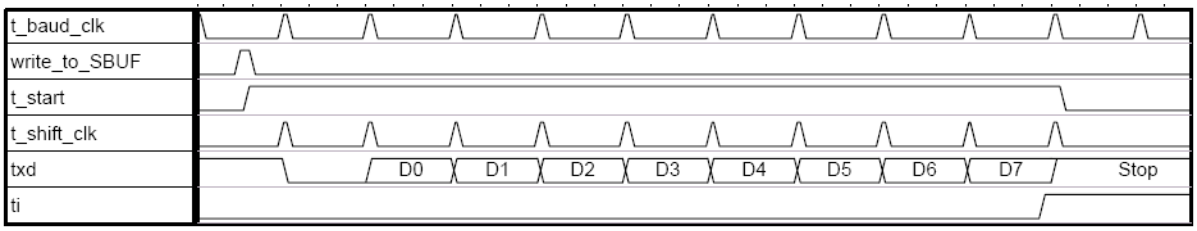


Fig.10-9: Transmit mode B

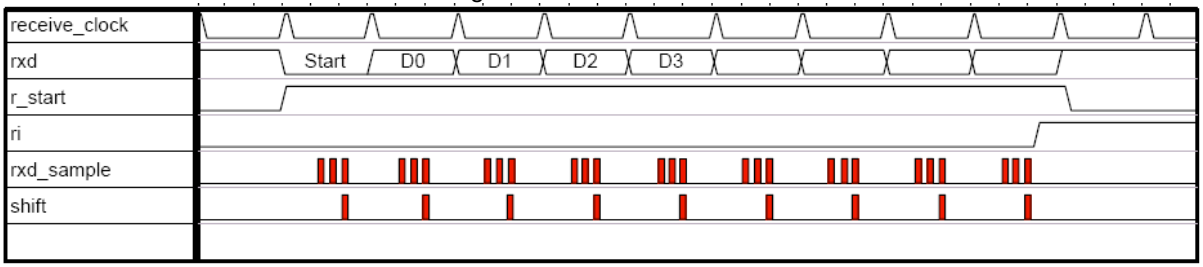


Fig.10-10: Receive mode B

9.2.3 Multiprocessor Communication of Serial Interface

The feature of receiving 9 bits in Mode A of Serial Interface can be used for multiprocessor communication. In this case, the slave processors have bit S1M2 in S1CON set to 1. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear S1M2 and receive the rest of the message, while other slaves will leave S1M2 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

9.2.4 Baud rate generator

Serial interface modes A and B

$$\text{Baud Rate} = \frac{F_{clk}}{32 \times \left(2^{10} - \text{S1REL}\right)}$$

9.3 Serial interface 2

Mnemonic: S2CON **Address: 93h**

7	6	5	4	3	2	1	0	Reset
S2M	-	S2M2	REN2	TB82	RB82	TI2	RI2	00H

S2M: Serial Port 2 mode selection.

S2M	Mode
0	A
1	B

S2M2: Enables multiprocessor communication feature

REN2: If set, enables serial reception. Cleared by software to disable reception.

TB82: The 9th transmitted data bit in modes A. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB82: In modes A, it is the 9th data bit received. In mode B, if S1M2 is 0, RB81 is the stop bit. Must be cleared by software.

TI2: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI2: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

The Serial interface2 can operate in the following 2 modes:

S2M	Mode	Description	Board Rate
0	A	9-bit UART	Variable
1	B	8-bit UART	Variable

9.3.1 Mode A

This mode is similar to Mode 2 and 3 of Serial interface 0, 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB81 in S2CON is outputted as the 9th bit, and at receive, the 9th bit affects RB81 in Special Function Register S2CON.

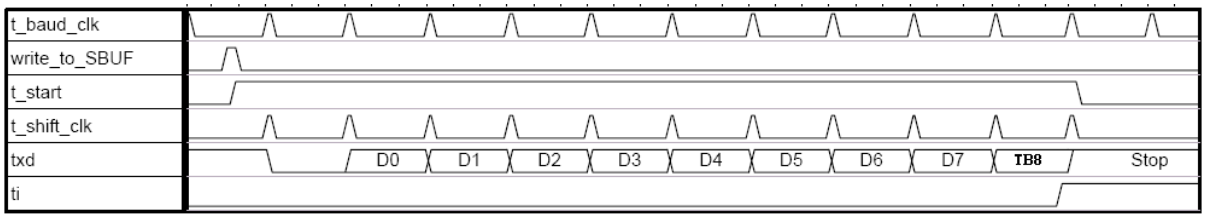


Fig.10-11: Transmit mode A

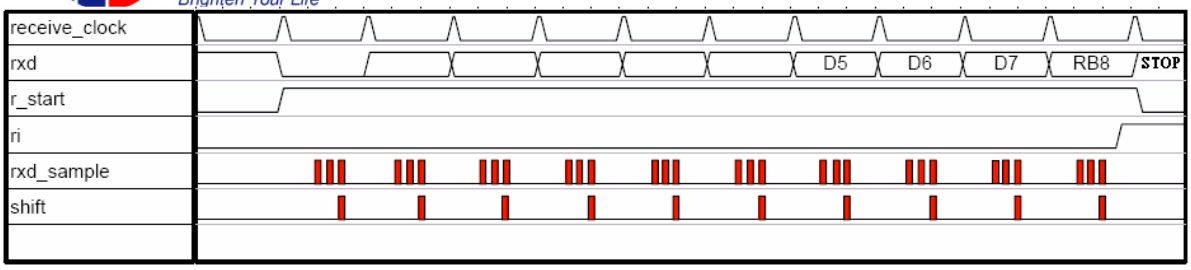


Fig.10-12: Receive mode A

9.3.2 Mode B

This mode is similar to Mode 1 of Serial interface 0. Pin RXD2 serves as input, and TXD2 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S2BUF, and stop bit sets the flag RB82 in the Special Function Register S2CON. In mode B internal baud rate generator is use to specify the baud rate.

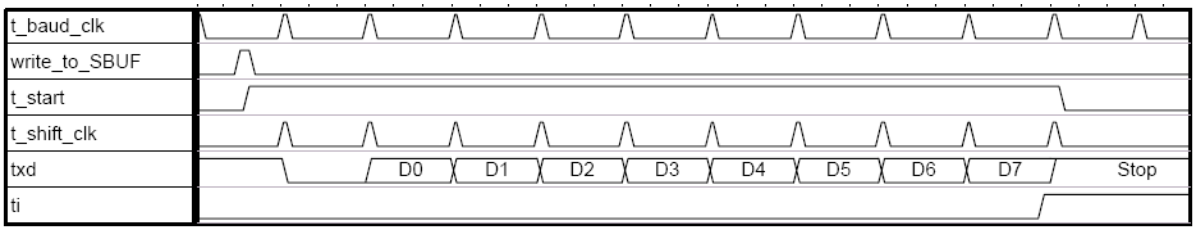


Fig.10-13: Transmit mode B

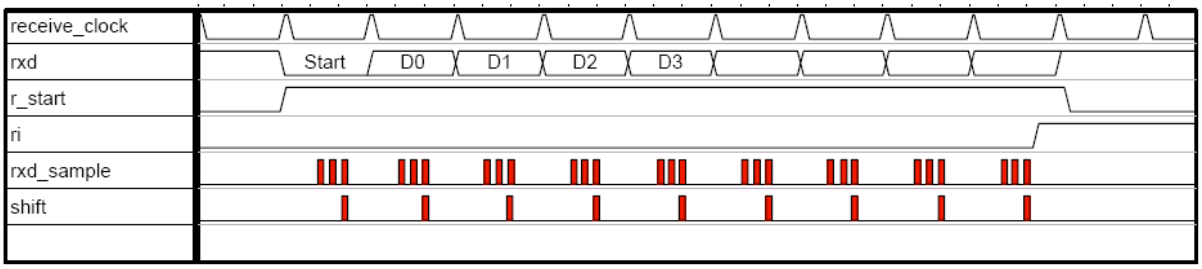


Fig.10-14: Receive mode B

9.3.3 Multiprocessor Communication of Serial Interface

The feature of receiving 9 bits in Mode A of Serial Interface can be used for multiprocessor communication. In this case, the slave processors have bit S2M2 in S2CON set to 1. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear S2M2 and receive the rest of the message, while other slaves will leave S1M2 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

9.3.4 Baud rate generator

Serial interface modes A and B

$$\text{Baud Rate} = \frac{F_{clk}}{32 \times \left(2^{10} - \text{S2REL}\right)}$$

9.4 Serial interface 3

Mnemonic: S3CON **Address: B1h**

7	6	5	4	3	2	1	0	Reset
S3M	-	S3M2	REN3	TB83	RB83	TI3	RI3	00H

S3M: Serial Port 3 mode selection.

S3M	Mode
0	A
1	B

S3M2: Enables multiprocessor communication feature

REN3: If set, enables serial reception. Cleared by software to disable reception.

TB83: The 9th transmitted data bit in modes A. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB83: In modes A, it is the 9th data bit received. In mode B, if S3M2 is 0, RB83 is the stop bit. Must be cleared by software.

TI3: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI3: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

The Serial Interface 3 can operate in the following 2 modes:

S2M	Mode	Description	Board Rate
0	A	9-bit UART	Variable
1	B	8-bit UART	Variable

9.4.1 Mode A

This mode is similar to Mode 2 and 3 of Serial interface 0, 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB83 in S3CON is outputted as the 9th bit, and at receive, the 9th bit affects RB83 in Special Function Register S3CON.

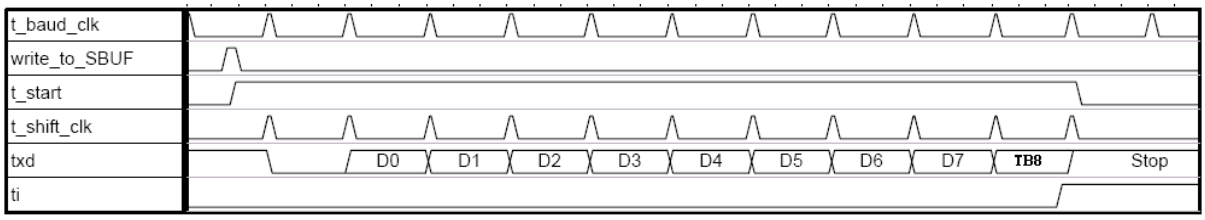


Fig.10-15: Transmit mode A

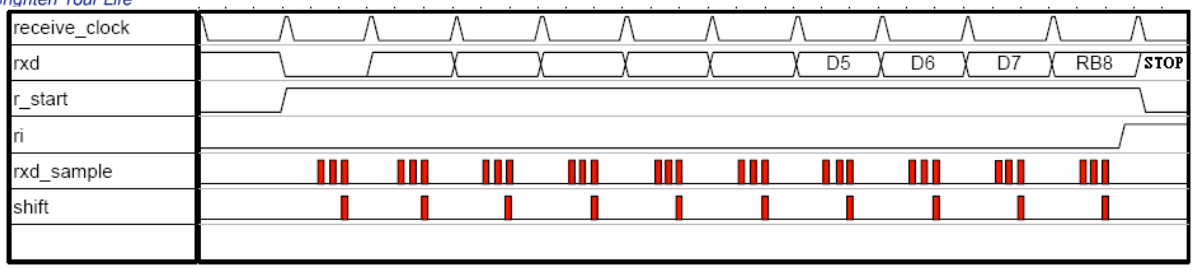


Fig.10-16: Receive mode A

9.4.2 Mode B

This mode is similar to Mode 1 of Serial interface 0. Pin RXD3 serves as input, and TXD3 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S3BUF, and stop bit sets the flag RB83 in the Special Function Register S3CON. In mode B internal baud rate generator is use to specify the baud rate.

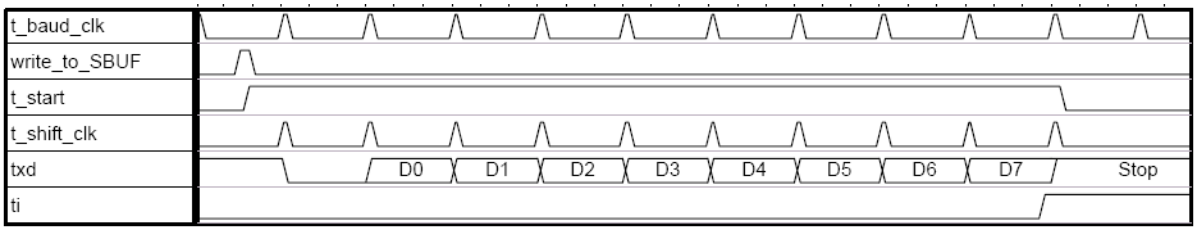


Fig.10-17: Transmit mode B

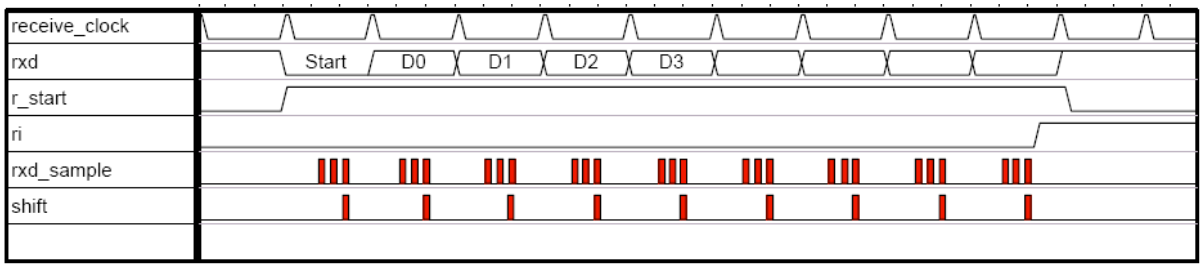


Fig.10-18: Receive mode B

9.4.3 Multiprocessor Communication of Serial Interface

The feature of receiving 9 bits in Mode A of Serial Interface can be used for multiprocessor communication. In this case, the slave processors have bit S3M2 in S3CON set to 1. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear S3M2 and receive the rest of the message, while other slaves will leave S3M2 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

9.4.4 Baud rate generator

Serial interface modes A and B

$$\text{Baud Rate} = \frac{F_{clk}}{32 \times \left(2^{10} - \text{S2REL}\right)}$$

9.5 IR control

IR transmission Period Register (baud rate generator).

Mnemonic: IRTPRL **Address: FF60h**

7	6	5	4	3	2	1	0	Reset
IRTPR.7	IRTPR.6	IRTPR.5	IRTPR.4	IRTPR.3	IRTPR.2	IRTPR.1	IRTPR.0	00H

Mnemonic: IRTPRH **Address: FF61h**

7	6	5	4	3	2	1	0	Reset
IRE3	IRE2	IRE1	IRE0	IRTPR.11	IRTPR.10	IRTPR.9	IRTPR.8	00H

IRE3: Enable IR and combine with UART3 .

IRE3 = 0 – Disable IR transmit when IRE2=IRE1=IRE0=0.

IRE3 = 1 – Enable IR and combine with UART3.

IRE2: Enable IR and combine with UART2 .

IRE2 = 0 – Disable IR transmit when IRE3=IRE1=IRE0=0.

IRE2 = 1 – Enable IR and combine with UART2.

IRE1: Enable IR and combine with UART1 .

IRE1 = 0 – Disable IR transmit when IRE3=IRE2=IRE0=0.

IRE1 = 1 – Enable IR and combine with UART1.

IRE0: Enable IR and combine with UART0 .

IRE0 = 0 – Disable IR transmit when IRE3=IRE2=IRE1=0.

IRE0 = 1 – Enable IR and combine with UART0.

IRTPR.n: IR Transmission Period Register.

n=0~11

IR transmission Duty Register.

Mnemonic: IRTDRL **Address: FF62h**

7	6	5	4	3	2	1	0	Reset
IRTDR.7	IRTDR.6	IRTDR.5	IRTDR.4	IRTDR.3	IRTDR.2	IRTDR.1	IRTDR.0	00H

Mnemonic: IRTDRH **Address: FF63h**

7	6	5	4	3	2	1	0	Reset
IROIDLE0	-	-	-	IRTDR.11	IRTDR.10	IRTDR.9	IRTDR.8	00H

IROIDLE0: IR transmission output idle state.

IROIDLE0 = 0 – IR output 1 when transmission idle.

IROIDLE0 = 1 – IR output 0 when transmission idle.

IRTDR.n: IR Transmission Duty Register.

n=0~11

$$\text{IR Tx period} = \frac{\text{IRTPR} + 1}{\text{system clock}}$$

$$\text{IR Leader pulse} = \frac{\text{IRTDR}}{\text{system clock}}$$

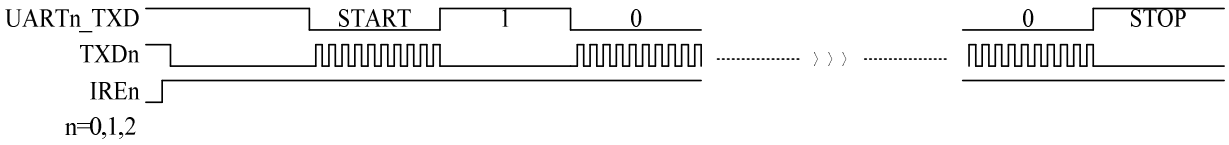


Fig.10-19: IR TXD0/1/2

10. Watchdog timer

The Watch Dog Timer (WDT) is an 8-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDTF bit of WDTC register whenever un-predicted reset happened. After an external reset the watchdog timer is disabled and all registers are set to zeros.

The clock of WDT is from 32768 crystal. The WDT will keep on running even after the system clock has been turned off (for example, in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the MCU to reset. The WDT can be enabled or disabled any time during the normal mode. Please refer the WDTE bit of WDTC register. The default WDT time-out period is approximately 178.0ms (WDTM [3:0] = 0100b).
The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit3 ~ bit0 (WDTM [3:0]) of Watch Dog Timer Control Register (WDTC) should be set accordingly. As shown in **錯誤! 找不到參照來源。**.

$$WDTCLK = \frac{32\text{KHz}}{2^{\text{WDTM}}}$$

$$\text{Watchdog reset time} = \frac{256}{\text{WDTCLK}}$$

Table11-1: WDT time-out period

WDTM [3:0]	Divider	Time period @ 32KHz
0000	1	7.9ms
0001	2	15.8ms
0010	4	31.6ms
0011	8	63.4ms
0100	16	126.8ms
0101	32	253.6ms (default)
0110	64	507.3ms
0111	128	1.0148s
1000	256	2.0296s
1001	512	4.0594s
1010	1024	8.1189s
1011	2048	16.237s
1100	4096	32.476s
1101	8192	64.952s
1110	16384	129.90s
1111	32768	259.81s

When MCU is reset, the MCU will be read WDTEN control bit status. When WDTEN bit is set to 1, the watchdog function will be disabled no matter what the WDTE bit status is. When WDTEN bit is clear to 0, the watchdog function will be enabled if WDTE bit is set to 1 by program. User can to set WDTEN on the writer or ISP.

The program can enable the WDT function by programming 1 to the WDTE bit premise that WDTEN control bit is clear to 0. After WDTE set to 1, the 8 bit-counter starts to count with the selected time base source clock which set by WDTM [3:0]. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when MCU been reset, either hardware reset or WDT reset. As shown in **錯誤! 找不到參照來源。**.

Once the watchdog is started it cannot be stopped. User can refreshed the watchdog timer to zero by writing 0x55 to

Watch Dog Timer refresh Key (WDTK) register. This will clear the content of the 8-bit counter and let the counter re-start to count from the beginning. The watchdog timer must be refreshed regularly to prevent reset request signal from becoming active.

When Watchdog timer is overflow, the WDTF flag will set to one and automatically reset MCU. The WDTF flag can be clear by software or external reset or power on reset.

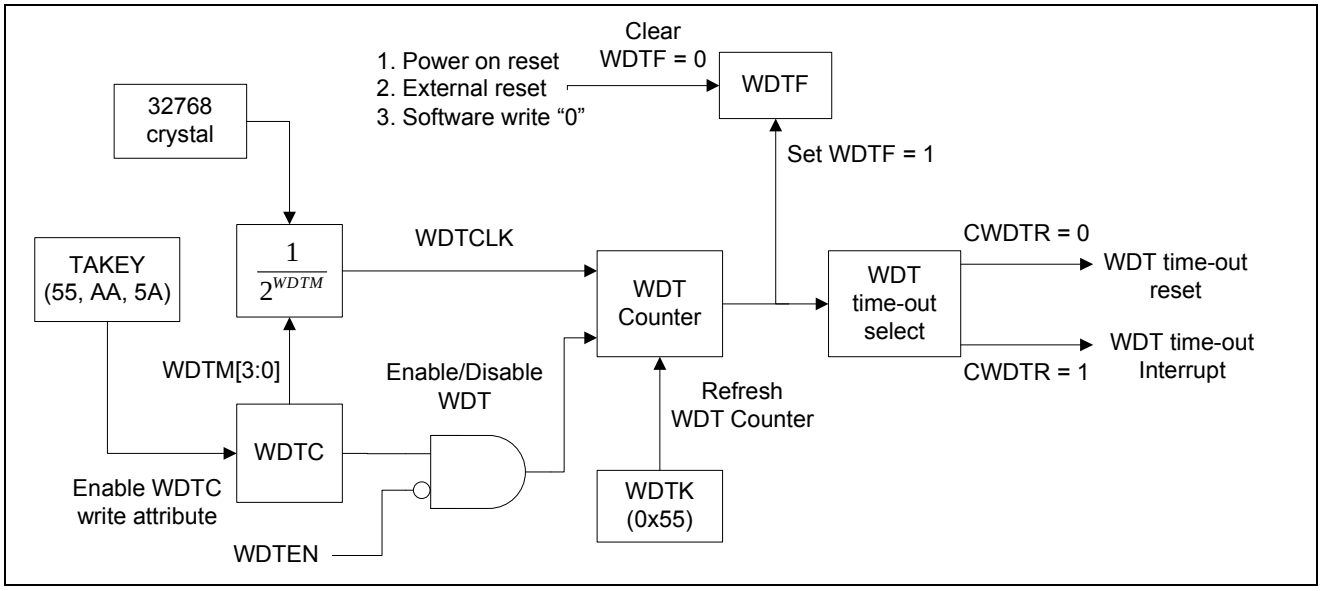


Fig. 9-1: Watchdog timer block diagram

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Watchdog Timer											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
WDTC	Watchdog timer control register	B6h	-	CWDTR	WDTE	-	WDTM [3:0]				04H
WDTK	Watchdog timer refresh key	B7h	WDTK[7:0]								00H
RSTS	Reset status register	A1h	-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00H

Address: F7h

Mnemonic: TAKEY

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Watchdog timer control register (WDTRC & WDTIC)is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the WDTRC write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

.

Mnemonic: WDTC **Address: B6h**

7	6	5	4	3	2	1	0	Reset
-	CWDTR	WDTE	-	WDTM [3:0]				04H

CWDTR: Watch dog states select bit(Support stop mode wakeup)

CWDTR = 0 - Enable watch dog reset.

CWDTR = 1 - Enable watch dog interrupt.

WDTE: Control bit used to enable Watchdog timer.
The WDTE bit can be used only if WDTEN is "0". If the WDTEN bit is "0", then WDT can be disabled / enabled by the WDTE bit.

WDTE = 0 - Disable WDT.

WDTE = 1 - Enable WDT.
The WDTE bit is not used if WDTEN is "1". That is, if the WDTEN bit is "1", WDT is always disabled no matter what the WDTE bit status is. The WDTE bit can be read and written.

WDTM [3:0]: WDT clock source divider bit. As seen in **錯誤! 找不到參照來源。** to reference the WDT time-out period.

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	-	-	PDRF	WDTF	SWRF	LVRF	PORF	00h

WDTF: Watchdog timer reset flag. When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software

Mnemonic: WDTK **Address: B7h**

7	6	5	4	3	2	1	0	Reset
WDTK[7:0]								00h

WDTK: Watchdog timer refresh key.
A programmer must write 0x55 into WDTK register, and then the watchdog timer will be cleared to zero.

For example 1, if enable WDT and select time-out reset period is 2.8493s.

First, programming the information block OP3 bit7 WDTEN to “0”.

Secondly,

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah     ; enable WDTC write attribute.
MOV WDTC, #28h      ; Set WDTM [3:0] = 1000b. Set WDTE =1 to enable WDT function.
.
.
.
MOV WDTK, #55h      ; Clear WDT timer to 0.
```

For example 2, if enable WDT and select time-out Interrupt period is 178.0ms.

First, programming the information block OP3 bit7 WDTEN to “0”.

Secondly,

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah     ; enable WDTC write attribute.
MOV WDTC, #64h      ;Set WDTM [3:0] = 0100b. ;Set WDTE =1 to enable WDT function
                    ; and Set CWDTR =1 to enable period interrupt function
```

11. Interrupt

The OB59A28A1 provides 18 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register. Each interrupt requested by the corresponding flag could individually be enabled or disabled by the enable bits in SFR's IEN0, IEN1, IEN2.

When the interrupt occurs, the engine will vector to the predetermined address as given in **錯誤! 找不到參照來源。**. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction RETI. When an RETI is performed, the processor will return to the instruction that would have been next when interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, and then samples are polled by hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then interrupt request flag is set. On the next instruction cycle the interrupt will be acknowledged by hardware forcing an LCALL to appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of microcontroller when the interrupt occurs. If microcontroller is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles for perform the LCALL.

Table 12-1: Interrupt vectors

	Interrupt Request Flags	Interrupt Vector Address	Keil C Interrupt Number
1	IE0 – External interrupt 0	0003h	0
2	TF0 – Timer 0 interrupt	000Bh	1
3	IE1 – External interrupt 1	0013h	2
4	TF1 – Timer 1 interrupt	001Bh	3
5	RI0/TI 0– Serial channel 0 interrupt	0023h	4
6	TF2/EXF2 – Timer 2 interrupt	002Bh	5
7	RI3/TI3 – Serial channel 3 interrupt	0033h	6
8	ISO7816IF	003Bh	7
9	SPIIF – SPI interrupt	004Bh	9
10	ADCIF – A/D converter interrupt (ADC/SADC)	0053h	10
11	VDCTIF	005Bh	11
12	LVIIF – Low Voltage Interrupt	0063h	12
13	IICIF – IIC interrupt	006Bh	13
14	RTC interrupt	0073h	14
15	RI2/TI2 – Serial channel 2 interrupt	007Bh	15
16	RI1/TI1 – Serial channel 1 interrupt	0083h	16
17	WDT – Watchdog interrupt	008Bh	17
18	Comparator interrupt	009Bh	19

*See Keil C about C51 User's Guide about Interrupt Function description

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Interrupt											
IEN0	Interrupt Enable 0 register	A8H	EA		ET2	ES0	ET1	EX1	ET0	EX0	00H
IEN1	Interrupt Enable 1 register	B8H	EXEN2		IEIIC0	IELVI	IEISO7816	IEADC	IEIIC1		00H
IEN2	Interrupt Enable 2 register	9AH	IESDAC	ES3	EVDCT	ERTC	ES2	ECmpl	EWDT	ES1	00H
IRCON	Interrupt request register	C0H	EXF2	TF2	IICIF0	LVIIF	ISO7816F	ADCIF	IICIF1		00H
IRCON2	Interrupt request register 2	97H	SADCIF	-	VDCTIF	-		CmpIF	WDTIF	-	00H
IP0	Interrupt priority level 0	A9H	-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00H
IP1	Interrupt priority level 1	B9H	-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00H
INTS	Interrupt Input select	E5H	INTS.7	INTS.6	INTS.5	INTS.4	INTS.3	INTS.2	INTS.1	INTS.0	11H
INTLA	Interrupt Input latch	9FH	INTLA.7	INTLA.6	INTLA.5	INTLA.4	INTLA.3	INTLA.2	INTLA.1	INTLA.0	00H

Mnemonic: IEN0 **Address: A8h**

7	6	5	4	3	2	1	0	Reset
EA		ET2	ES	ET1	EX1	ET0	EX0	00h

EA: EA=0 – Disable all interrupt.

EA=1 – Enable all interrupt.

ET3: ET3 = 0 – Disable Timer 3 overflow or external reload interrupt.

ET3 = 1 – Enable Timer 3 overflow or external reload interrupt.

ET2: ET2=0 – Disable Timer 2 overflow or external reload interrupt.

ET2=1 – Enable Timer 2 overflow or external reload interrupt.

ES0: ES0=0 – Disable Serial channel 0 interrupt.

ES0=1 – Enable Serial channel 0 interrupt.

ET1: ET1=0 – Disable Timer 1 overflow interrupt.

ET1=1 – Enable Timer 1 overflow interrupt.

EX1: EX1=0 – Disable external interrupt 1.

EX1=1 – Enable external interrupt 1.

ET0: ET0=0 – Disable Timer 0 overflow interrupt.

ET0=1 – Enable Timer 0 overflow interrupt.

EX0: EX0=0 – Disable external interrupt 0.

EX0=1 – Enable external interrupt 0.

Mnemonic: IEN1 **Address: B8h**

7	6	5	4	3	2	1	0	Reset
EXEN2		IEIIC	IELVI	IEKBI	IEADC	IEIIC1		00H

EXEN2: Timer 2 reload interrupt enable.

EXEN2 = 0 – Disable Timer 2 external reload interrupt.

EXEN2 = 1 – Enable Timer 2 external reload interrupt.

IEIIC0: IIC0 interrupt enable.

IEIIC0 = 0 – Disable IIC0 interrupt.

IEIIC0 = 1 – Enable IIC0 interrupt.

IELVI: LVI interrupt enable.

IELVI = 0 – Disable LVI interrupt.

IELVI = 1 – Enable LVI interrupt.

IEISO7816 ISO7816 interrupt enable

IEISO7816 = – Disable ISO7816 interrupt

IEISO7816 = – Enable ISO7816 interrupt

IEADC: A/D converter interrupt enable(16bit sigma-delta ADC)

IEADC = 0 – Disable ADC interrupt.

IEADC = 1 – Enable ADC interrupt.

IEIIC1: SPI interrupt enable.

IESPI = 0 – Disable SPI interrupt.

IESPI = 1 – Enable SPI interrupt.

Mnemonic: IEN2 **Address: 9Ah**

7	6	5	4	3	2	1	0	Reset
IESADC	ES3	EVDCT	ERTC	ES2	ECmpl	EWDT	ES1	00H

IESADC A/D converter interrupt enable (12bit SAR ADC)

IESADC = 0 – Disable SADC interrupt.

IESADC = 1 – Enable SADC interrupt.

ES3 Enable Serial 3 interrupt.

ES3 = 0 – Disable Serial 3 interrupt.

ES3 = 1 – Enable Serial 3 interrupt.

EVDCT Enable VDCIN voltage toggle interrupt.

EVDCL = 0 – Disable VDCIN voltage toggle interrupt.

EVDCL = 1 – Enable VDCIN voltage toggle interrupt.

ERTC Enable RTC interrupt.

ERTC = 0 – Disable RTC interrupt.

ERTC = 1 – Enable RTC interrupt.

ES2 Enable Serial 2 interrupt.

ES2 = 0 – Disable Serial 2 interrupt.

ES2 = 1 – Enable Serial 2 interrupt.

ECmpI Enable Comparator interrupt (include comparator_0 and comparator_1).

ECmpI = 0 – Disable Comparator interrupt.

ECmpI = 1 – Enable Comparator interrupt.

EWDT Enable Watch dog interrupt.

EWDT = 0 – Disable Watch dog interrupt.

EWDT = 1 – Enable Watch dog interrupt.

ES1: Enable Serial 1 interrupt.

ES1 = 0 – Disable Serial 1 interrupt.

ES1 = 1 – Enable Serial 1 interrupt.

Mnemonic: IRCON **Address: C0h**

7	6	5	4	3	2	1	0	Reset
EXF2	TF2	IICIF	LVIIF	ISO78161F	ADCIF	SPIIF		00H

EXF2: Timer 2 external reload flag. Must be cleared by software.

TF2: Timer 2 overflow flag. Must be cleared by software.

IICIF: IIC interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

LVIIF: LVI interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

ISO7816IF ISO7816 interrut flag..

ADCIF: 16bit sigma-delta ADC end interrupt flag. Must be cleared by software.

SPIIF: SPI interrupt flag.

Mnemonic:IRCON2 **Address: 97h**

7	6	5	4	3	2	1	0	Reset
SADCIF	-	VDCTIF	-		CmpIF	WDTIF	-	00H

SADCIF 12bit SAR ADC end interrupt flag. Must be cleared by software.

VDCTIF VDCIN toggle interrupt flag.

HW will clear this flag automatically when enter interrupt vector.

SW can clear this flag also.

CmpIF Comparator interrupt flag

HW will clear this flag automatically when enter interrupt vector.

SW can clear this flag also.(in case analog comparator INT disable)

WDTIF: Watch dog interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

Mnemonic: INTS **Address: E5h**

7	6	5	4	3	2	1	0	Reset
INTS.7	INTS.6	INTS.5	INTS.4	INTS.3	INTS.2	INTS.1	INTS.0	11h

INTS.7: INTS.7=0 – Disconnect INT1 and P23.

INTS.7=1 – Set P23 to be INT1 input.

INTS.6: INTS.6=0 – Disconnect INT1 and P27.

INTS.6=1 – Set P27 to be INT1 input.

INTS.5: INTS.5=0 – Disconnect INT1 and P13.

INTS.5=1 – Set P13 to be INT1 input.

INTS.4: INTS.4=0 – Disconnect INT1 and P71.

INTS.4=1 – Set P71 to be INT1 input.

INTS.3: INTS.3=0 – Disconnect INT0 and P22.

INTS.3=1 – Set P22 to be INT0 input.

INTS.2: INTS.2=0 – Disconnect INT0 and P26.

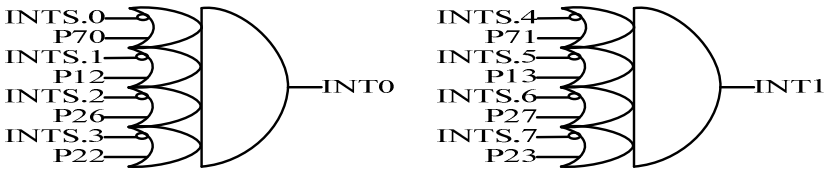
INTS.2=1 – Set P26 to be INT0 input.

INTS.1: INTS.1=0 – Disconnect INT0 and P12.

INTS.1=1 – Set P12 to be INT0 input.

INTS.0: INTS.0=0 – Disconnect INT0 and P70.

INTS.0=1 – Set P70 to be INT0 input.



Mnemonic: INTLA **Address: 9Fh**

7	6	5	4	3	2	1	0	Reset
INTLA.7	INTLA.6	INTLA.5	INTLA.4	INTLA.3	INTLA.2	INTLA.1	INTLA.0	00h

INTLA.7: INTLA.7=0 – No INT1 trigger at P23.

INTLA.7=1 – P23 input trigger latch when INTS.7=1. Clear by SW.

INTLA.6: INTLA.6=0 – No INT1 trigger at P27.

INTLA.6=1 – P27 input trigger latch when INTS.6=1. Clear by SW.

INTLA.5: INTLA.5=0 – No INT1 trigger at P13.

INTLA.5=1 – P13 input trigger latch when INTS.5=1. Clear by SW.

INTLA.4: INTLA.4=0 – No INT1 trigger at P71.

INTLA.4=1 – P71 input trigger latch when INTS.4=1. Clear by SW.

INTLA.3: INTLA.3=0 – No INT0 trigger at P22.

INTLA.3=1 – P22 input trigger latch when INTS.3=1. Clear by SW.

INTLA.2: INTLA.2=0 – No INT0 trigger at P26.

INTLA.2=1 – P26 input trigger latch when INTS.2=1. Clear by SW.

INTLA.1: INTLA.1=0 – No INT0 trigger at P12.

INTLA.1=1 – P12 input trigger latch when INTS.1=1. Clear by SW.

INTLA.0: INTLA.0=0 – No INT0 trigger at P70.

INTLA.0=1 – P70 input trigger latch when INTS.0=1. Clear by SW.

11.1 Priority level structure

All interrupt sources are combined in groups, As given in 錯誤! 找不到參照來源。.

Table 12-2: Priority level groups

Groups		
External interrupt 0	Serial channel 1 interrupt	Serial channel 3 interrupt
Timer 0 interrupt	Watchdog interrupt	SPI interrupt
External interrupt 1	Comparator interrupt	ADC interrupt(ADC/SADC)
Timer 1 interrupt	Serial channel 2 interrupt	ISO7816 interrupt
Serial channel 0 interrupt	RTC interrupt	LVI interrupt
Timer 2 interrupt	VDCT interrupt	IIC interrupt

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level will be received simultaneously, an internal polling sequence determines which request is serviced first. As given in 錯誤! 找不到參照來源。 and 錯誤! 找不到參照來源。 and 錯誤! 找不到參照來源。.

Mnemonic: IP0 **Address: A9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00h

Mnemonic: IP1 **Address: B9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00h

Table 12-3: Priority levels

IP1.x	IP0.x	Priority Level
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

Table 12-4: Groups of priority

Bit	Group		
IP1.0, IP0.0	External interrupt 0	Serial channel 1 interrupt	Serial channel 3 interrupt
IP1.1, IP0.1	Timer 0 interrupt	Watchdog interrupt	SPI interrupt
IP1.2, IP0.2	External interrupt 1	Comparator interrupt	ADC interrupt(ADC/SADC)
IP1.3, IP0.3	Timer 1 interrupt	Serial channel 2 interrupt	ISO7816 interrupt
IP1.4, IP0.4	Serial channel 0 interrupt	RTC interrupt	LVI interrupt
IP1.5, IP0.5	Timer 2 interrupt	VDCT interrupt	IIC interrupt

Table 11-5: Polling sequence

Interrupt source	Sequence
External interrupt 0	
Serial channel 1 interrupt	
Serial channel 3 interrupt	
Timer 0 interrupt	
Watchdog interrupt	
SPI interrupt	
External interrupt 1	
Comparator interrupt	
ADC interrupt(ADC/SADC)	
Timer 1 interrupt	
Serial channel 2 interrupt	
ISO7816 interrupt	
Serial channel 0 interrupt	
RTC interrupt	
LVI interrupt	
Timer 2 interrupt	
VDCT interrupt	
IIC interrupt	

12. Power Management Unit

Power management unit serves two power management modes, IDLE and STOP, for the users to do power saving function.

Mnemonic: PCON **Address: 87h**

7	6	5	4	3	2	1	0	Reset
SMOD	MDUF	-	VDCIS	PDALDO3	PDLDO3	STOP	IDLE	4Ch

VDCIS: VDCIN pin status. Read only.

PDALDO3: Setting this bit will turn off LDO30A, VCC output Hi-Z.

PDLDO3: Setting this bit will turn off LDO30, VLDO3 output Hi-Z.

STOP: Stop mode control bit. Setting this bit turning on the Stop Mode.
Stop bit is always read as 0

IDLE: Idle mode control bit. Setting this bit turning on the Idle Mode.
Idle bit is always read as 0

12.1 Idle mode

Setting the IDLE bit of PCON register invokes the IDLE mode. The IDLE mode leaves internal clocks and peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any interrupts or a reset.

12.2 Stop mode

Setting the STOP bit of PCON register invokes the STOP mode. All internal clocking in this mode is turn off. The CPU will exit this state from a no-clocked interrupt (external INT0/1/2/3, LVI, KBI and Watchdog interrupt) or a reset (WDTR and LVR) condition. Internally generated interrupts (timer, serial port ...) have no effect on stop mode since they require clocking activity.

12.3 LDO control

Setting the PDALDO3 bit of PCON register will turn off LDO30A; VCC output Hi-Z.

Setting the PDLDO3 bit of PCON register will turn off LDO30; VLDO3 output Hi-Z.

User should set PCON[3:2] firstly then set PCON.1, i.e., do not set PCON[3:2] and PCON.1 in the same instruction.

12.4 VDCIN status

VDCIS is the current output status of VDC detector.

13. IIC function

The IIC module uses the SCL (clock) and the SDA (data) line to communicate with external IIC interface. Its speed can be selected to 400Kbps (maximum) by software setting the IICBR [2:0] control bit. The IIC module provided 2 interrupts (RXIF, TXIF). It will generate START, repeated START and STOP signals automatically in master mode and can detects START, repeated START and STOP signals in slave mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

The interrupt vector is 6Bh.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
IIC0 function											
AUX	Auxiliary register	91h	BRGS							DPS	00H
IICCTL	IIC control register	F9h	IICEN	MSS	MAS	AB_EN	BF_EN	IIC0BR[2:0]			04H
IIC0S	IIC status register	F8h	-	MPIF	LAIF	RXIF	TXIF	RXAK	TXAK	RW or BB	00H
IICA1	IIC Address 1 register	FAh	IIC0A1[7:1]							MATCH 1or RW1	A0H
IICA2	IIC Address 2 register	FBh	IIC0A2[7:1]							MATCH 2 or RW2	60H
IICRWD	IIC Read/ Write register	FCh	IIC0RWD[7:0]								00H
IICEBT	IIC Enaable Bus Transaction	FDh	FU_EN		-	-	-	-	-	-	00H

Mnemonic: AUX **Address:91h**

7	6	5	4	3	2	1	0	Reset
BRGS							DSP	00

Mnemonic: IICCTL **Address: F9h**

7	6	5	4	3	2	1	0	Reset
IICEN	MSS	MAS	AB_EN	BF_EN	IICBR[2:0]			04h

IICEN: Enable IIC module

IIC0EN = 1 is Enable

IIC0EN = 0 is Disable.

MSS: Master or slave mode select.

MSS0 = 1 is master mode.

MSS0 = 0 is slave mode.

*The software must set this bit before setting others register.

MAS: Master address select (master mode only)

MAS = 0 is to use IICA1.

MAS = 1 is to use IICA2.

AB_EN: Arbitration lost enable bit. (Master mode only)

If set AB_EN bit, the hardware will check arbitration lost. Once arbitration lost occurred,

hardware will return to IDLE state. If this bit is cleared, hardware will not care arbitration lost condition. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

BF_EN: Bus busy enable bit. (Master mode only)

If set BF0_EN bit, hardware will not generate a start condition to bus until BF=0. Clear this bit will always generate a start condition to bus when MStart is set. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

IIC0BR[2:0]: Baud rate selection (master mode only), where Fosc is the external crystal or oscillator frequency. The default is Fosc/(512+5) for users' convenience.

IIC0BR[2:0]	Baud rate
000	Fosc/(32+5)
001	Fosc/64+5)
010	Fosc/(128+5)
011	Fosc/(256+5)
100	Fosc/(512+5)
101	Fosc/(1024+5)
110	Fosc/(2048+5)
111	Fosc/(4096+5)

Mnemonic: IICS **Address: F8H**

7	6	5	4	3	2	1	0	Reset
-	MPIF	LAIF	RXIF	TXIF	RXAK	TXAK	RW or BB	00H

MPIF: The Stop condition Interrupt Flag

The stop condition occurred and this bit will be set. Software need to clear this bit

LAIF: Arbitration lost bit. (Master mode only)

The Arbitration Interrupt Flag, the bus arbitration lost occurred and this bit will be set. Software need to clear this bit

RXIF: The data Receive Interrupt Flag (RXIF0) is set after the IIC0RWD (IIC0 Read Write Data Buffer) is loaded with a newly receive data.

TXIF: The data Transmit Interrupt Flag (TXIF0) is set when the data of the IIC0RWD (IIC0 Read Write Data Buffer) is downloaded to the shift register.

RXAK: The Acknowledge Status indicate bit. When clear, it means an acknowledge signal has been received after the complete 8 bits data Transmit on the bus.

TXAK: The Acknowledge status Transmit bit. When received complete 8 bits data, this bit will set (NoAck) or clear (Ack) and Transmit to master to indicate the receive status.

RW or BB: Master Mode:

BB : Bus busy bit
If detect SCL=0 or SDA=0 or bus start, this bit will be set. If detect stop,this bit will be cleared. This bit can be cleared by software to return ready state.

Slave Mode:
RW:The slave mode read (received) or wrote (Transmit) on the IIC bus. When this bit is clear, the slave module received data on the IIC bus (SDA).(Slave mode only).

As shown in 錯誤! 找不到參照來源。

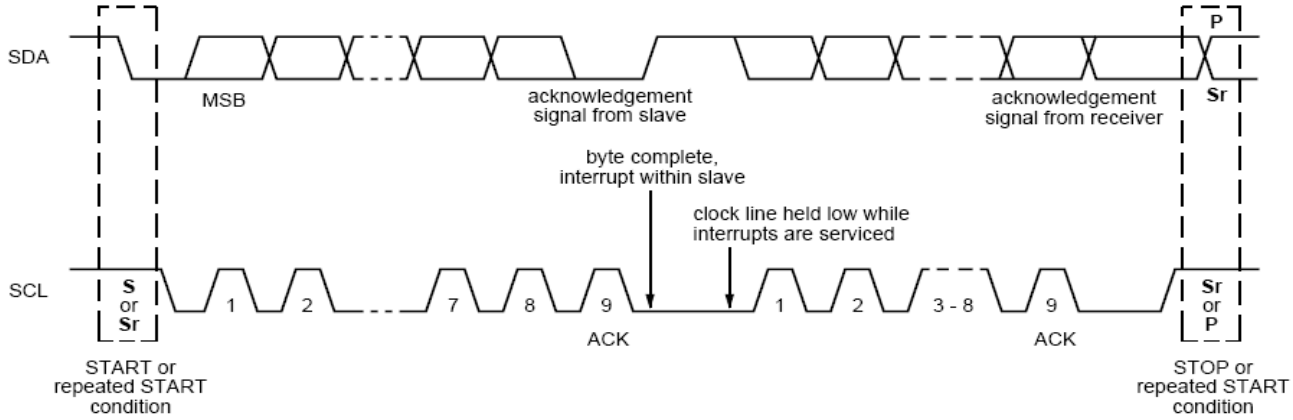


Fig. 12-1: Acknowledgement bit in the 9th bit of a byte transmission

Mnemonic: IICA1 **Address: FAH**

7	6	5	4	3	2	1	0	Reset
IICA1[7:1]							Match1 or RW1	A0H
R/W							R or R/W	

Slave mode:

IIC0A1[7:1]: IIC Address registers

This is the first 7-bit address for this slave module. It will be checked when an address (from master) is received

Match1: When IICA1 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.

Master mode:

IIC0A1[7:1]: IIC Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW1: This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It appears at the 8th bit after the IIC address as below figure. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master Transmit mode. As shown in 錯誤! 找不到參照來源。

RW1=1, master receive mode

RW1=0, master Transmit mode

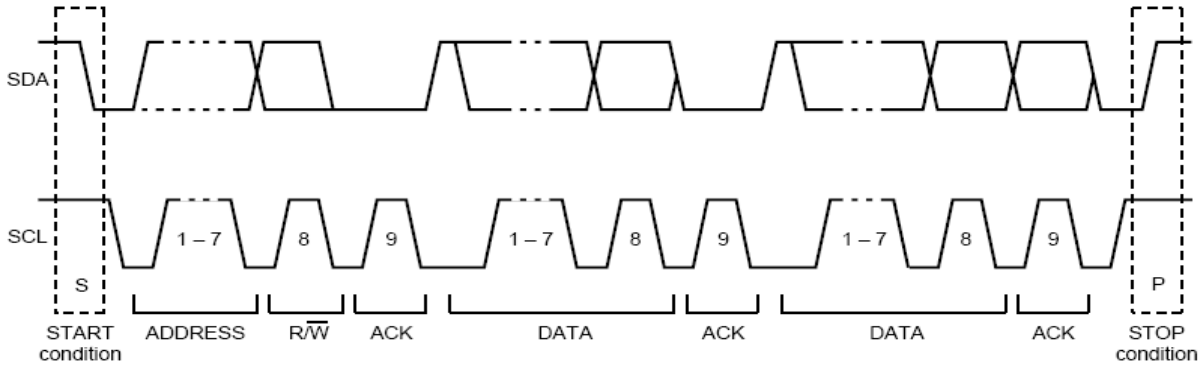


Fig. 12-2: RW bit in the 8th bit after IIC address

Mnemonic: IICA2 **Address: FBH**

7	6	5	4	3	2	1	0	Reset
IICA2[7:1]							Match2 or RW2	60H
R/W							R or R/W	

Slave mode:

IICA2[7:1]: IIC Address registers

This is the second 7-bit address for this slave module.

It will be checked when an address (from master) is received

Match2: When IICA2 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.

Master mode:

IICA2[7:1]: IIC Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW2: This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master Transmit mode.

RW2=1, master receive mode

RW2=0, master Transmit mode

Mnemonic: IICRWD **Address: FCh**

7	6	5	4	3	2	1	0	Reset
IIC0RWD[7:0]								00h

IICRWD[7:0]: IIC read write data buffer.

In receiving (read) mode, the received byte is stored here.

In Transmitting mode, the byte to be shifted out through SDA stays here.

Mnemonic: IICEBT **Address: FDH**

7	6	5	4	3	2	1	0	Reset
FU_EN		-	-	-	-	-	-	00H

Master Mode：

00: reserved

01: IIC bus module will enable read/write data transfer on SDA and SCL.

10: IIC bus module generate a start condition on the SDA/SCL, then send out address which is stored in the IIC0A1/IIC0A2(selected by MAS control bit)

11: IIC bus module generates a stop condition on the SDA/SCL.

FU_EN[7:6] will be auto-clear by hardware, so setting FU_EN[7:6] repeatedly is necessary.

Slave mode:

01: FU_EN[7:6] should be set as 01 only. The other value is inhibited.

Notice:

FU_EN[7:6] should be set as 01 before read/write data transfer for bus release; otherwise, SCL will be locked(pull low).

FU_EN[7:6] should be set as 01 after read/write data transfer for receiving a stop condition from bus master.

In Transmit data mode(slave mode), the output data should be filled into IIC0RWD before setting FU_EN[7:6] as 01.

FU_EN[7:6] will be auto-clear by hardware, so setting FU_EN[7:6] repeatedly is necessary.

14. SPI Function - Serial Peripheral Interface

Serial Peripheral Interface (SPI) is a synchronous protocol that allows a master device to initiate communication with slave devices.

The interrupt vector is 4Bh.

There are 4 signals used in SPI, they are
SPI_MOSI: data output in the master mode, data input in the slave mode,
SPI_MISO: data input in the master mode, data output in the slave mode,
SPI_SCK: clock output from the master, the above data are synchronous to this signal
SPI_SS: input in the slave mode.

This slave device detects this signal to judge if it is selected by the master. As shown in Fig. 15-1

In the master mode, it can select the desired slave device by any IO with value = 0. As below figure is an example showing the relation of the 4 signals between master and slaves.

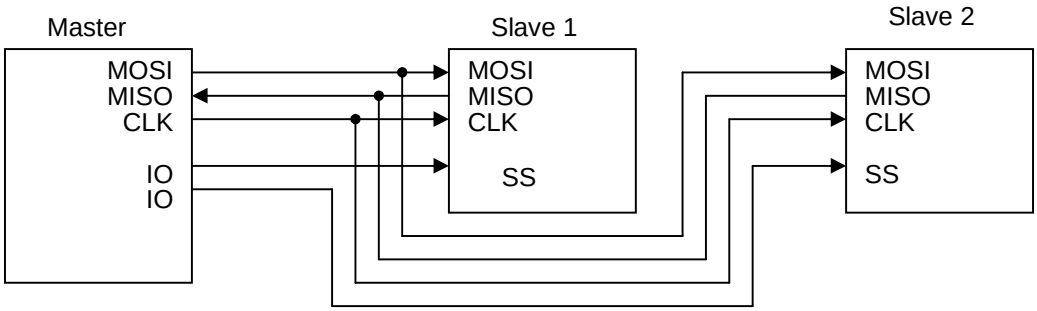


Fig. 15-1: SPI signals between master and slave devices

There is only one channel SPI interface. The SPI SFRs are shown as below:

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
SPI function											
SPIC1	SPI control register 1	F1h	SPIEN	SPIMSS	SPISSP	SPICKP	SPICKE	SPIBR[2:0]			08H
SPIC2	SPI control register 2	F2h	SPIFD	TBC[2:0]			SPIRST	RBC[2:0]			00H
SPIS	SPI status register	F5h	SPIRF	SPIMLS	SPIOV	SPITXIF	SPITDR	SPIRXIF	SPIRDR	SPIRS	40H
SPITXD	SPI Transmit data buffer	F3h	SPITXD[7:0]								00H
SPIRXD	SPI receive data buffer	F4h	SPIRXD[7:0]								00H

Mnemonic:SPIC1 **Address:F1H**

7	6	5	4	3	2	1	0	Reset
SPIEN	SPIMSS	SPISSP	SPICKP	SPICKE	SPIBR[2:0]			08H

SPIEN: Enable SPI module.

SPIEN = 1 - is Enable.

SPIEN = 0 - is Disable.

SPIMSS: Master or Slave mode Select

SPIMSS = 1 - is Master mode.

SPIMSS = 0 - is Slave mode.

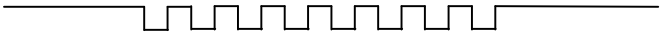
SPISSP: SS or CS active polarity.(Slave mode used only)

SPISSP = 1 - high active.

SPISSP = 0 - low active.

SPICKP: Clock idle polarity select.

SPICKP = 1 - SCK will idle high. Ex :



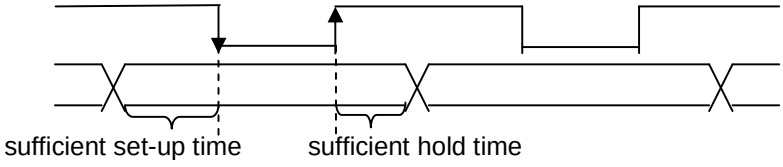
SPICKP = 0 - SCK will idle low. Ex :

SPICKE: Clock sample edge select.

SPICKE = 1 - rising edge latch data.

SPICKE = 0 - falling edge latch data.

* To ensure the data latch stability, OB59A128A1 generate the output data As shown in the following example, the other side can latch the stable data no matter in rising or falling edge.



SPIBR[2:0]: SPI baud rate select. (Master mode used only)

SPIBR[2:0]	Baud rate
0:0:0	Fosc/4
0:0:1	Fosc /8
0:1:0	Fosc /16
0:1:1	Fosc /32
1:0:0	Fosc /64
1:0:1	Fosc /128
1:1:0	Fosc /256
1:1:1	Fosc /512

Mnemonic: SPIC2 **Address: F2H**

7	6	5	4	3	2	1	0	Reset
SPIFD	TBC[2:0]			SPIRST	RBC[2:0]			00H

SPIFD: Full-duplex mode enable.

SPIFD = 1 is enable full-duplex mode.

SPIFD = 0 is disable full-duplex mode.

When it is set, the TBC[2:0] and RBC[2:0] will be reset and keep to zero. When the Master device Transmits data to the Slave device via the MOSI line, the Slave device responds by sending data to the Master device via the MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock. As shown in Fig. 15-2

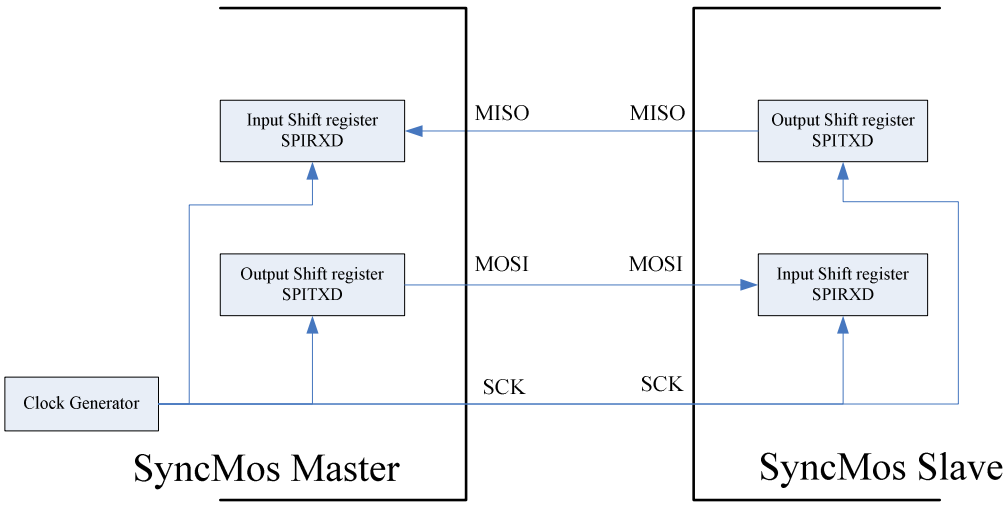


Fig. 15-2: SPI Master and slave transfer method

SPIRST: SPI Re-start (Slave mode used only)

SPIRST = 0 - Re-start function disable.SPI Transmit/receive data when SS active.

In SPITXD/SPIRXD buffer, data got from previous SS active period will not be removed (i.e. it's valid).

SPIRST = 1 - Re-start function enable.SPI Transmit/receive new data when SS re-active;

In SPITXD/SPIRXD buffer, data got from previous SS active period will be removed (i.e. It's invalid).

TBC[2:0]: SPI Transmitter bit counter.

TBC[2:0]	Bit counter
0:0:0	8 bits output
0:0:1	1 bit output
0:1:0	2 bits output
0:1:1	3 bits output
1:0:0	4 bits output
1:0:1	5 bits output
1:1:0	6 bits output
1:1:1	7 bits output

RBC[2:0]: SPI receiver bit counter.

RBC[2:0]	Bit counter
0:0:0	8 bits input
0:0:1	1 bit input
0:1:0	2 bits input
0:1:1	3 bits input
1:0:0	4 bits input
1:0:1	5 bits input
1:1:0	6 bits input
1:1:1	7 bits input

Mnemonic: SPIS **Address:F5H**

7	6	5	4	3	2	1	0	Reset
SPIRF	SPIMLS	SPIOV	SPITXIF	SPITDR	SPIRXIF	SPIRDR	SPIRS	40H

SPIRF: SPI SS pin Release Flag.

This bit is set when SS pin release & SPIRST as '1'.

SPIMLS: MSB or LSB first output /input Select.

SPIMLS = 1 is MSB first output/input.

SPIMLS = 0 is LSB first output/input.

SPIOV: Overflow flag.

When SPIRDR is set and next data already into shift register, this flag will be set.

It is clear by hardware, when SPIRDR is cleared.

SPITXIF: Transmit Interrupt Flag.

This bit is set when the data of the SPITXD register is downloaded to the shift register.

SPITDR: Transmit Data Ready.

When MCU finish writing data to SPITXD register, the MCU needs to set this bit to '1' to inform the SPI module to send the data. After SPI module finishes sending the data from SPITXD, this bit will be cleared automatically.

SPIRXIF: Receive Interrupt Flag.

This bit is set after the SPIRXD is loaded with a newly receive data.

SPIRDR: Receive Data Ready.

The MCU must clear this bit after it gets the data from SPIRXD register. The SPI module is able to write new data into SPIRXD only when this bit is cleared.

SPIRS: Receive Start.

This bit set to “1” to inform the SPI module to receive the data into SPIRXD register.

Mnemonic: SPITXD **Address: F3H**

7	6	5	4	3	2	1	0	Reset
SPITXD[7:0]								00H

SPITXD[7:0]: Transmit data buffer.

Mnemonic: SPIRXD **Address: F4H**

7	6	5	4	3	2	1	0	Reset
SPIRXD[7:0]								00H

SPIRXD[7:0]: Receive data buffer.

P.S. MISO pin must be float when SS or CS no-active in slave mode.

15. LVI & LVR – Low Voltage Interrupt and Low Voltage Reset

The interrupt vector 63h

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
LVR											
RSTS	Reset status register	A1h	CFRF	PRRF	LVRLPF	PDRF	WDTF	SWRF	LVRF	PORF	00H
LVC	Low voltage control register	E6h	LVI_EN	LVRLPE	LVRE	LVIF	CFRE	PRRE	LVIS[1:0]		60H

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
CFRF	PRRF	LVRLPF	PDRF	WDTF	SWRF	LVRF	PORF	00H

CFRF Clock failure reset flag.

When clock failure reset event occur, CFRF is set to 1. This flag can be cleared by software.

PRRF Power recovery reset flag.

When VDCIN rising (Vil ≒ 1.0V, Vih ≒ 1.1V), PRRF is set to 1. This flag can be cleared by software.

LVRLPF "External" Low voltage reset flag.

When MCU is reset by LVR(External Low Power), LVRLPF flag will be set to one by hardware. This flag clear by software.

PDRF: Pad reset flag.

When MCU is reset by reset pad, PDRF flag will be set to one by hardware. This flag clear by software.

WDTF: WDT reset flag.

When MCU is reset by WDT overflow, WDTF flag will be set to one by hardware. This flag clear by software.

SWRF: SoftWare reset flag.

When MCU is reset by software, SWRF flag will be set to one. This flag clear by software.

LVRF: Low voltage reset flag.

When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.

PORF: Power on reset flag.

When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

Mnemonic: LVC **Address: E6h**

7	6	5	4	3	2	1	0	Reset
LVI_EN	LVRLPE	LVRE	LVIF	CFRE	PRRE	LVIS[1:0]		60H

LVI_EN: Low voltage interrupt function enable bit.

LVI_EN = 0 - disable low voltage detect function.

LVI_EN = 1 - enable low voltage detect function.

LVRLPE External low voltage reset function (Low Power)enable bit. (detect external voltage)

LVRLPE = 0 - disable external low voltage reset(Low Power) function.

LVRLPE = 1 - enable external low voltage reset(Low Power) function.

Note: LVRLP = 1.14 V

LVRE: External low voltage reset function enable bit. (detect external voltage)

LVRXE = 0 - disable external low voltage reset function.

LVRXE = 1 - enable external low voltage reset function.

Note: LVR = 1.50 V

LVIF: Low Voltage interrupt Flag(i.e., Low Voltage Interrupt Status Flag)

CFRE Clock failure(32KHz Xtal) reset function enable bit.

RTCRE = 0 - disable clock failure(32KHz Xtal) reset function.

RTCRE = 1 - enable clock failure(32KHz Xtal) reset function.

PRRE: Power Recovery reset function enable bit.

PRRE = 0 - disable Power Recovery reset function.

PRRE = 1 - enable Power Recovery reset function.

LVIS[1:0] LVI level select:

00: 1.65V

01: 2.60V

10: 3.20V

11: 4.00V

16. 16-bit ADC(Sigma-Delta ADC)

The OB59A128A1 provides 8 channels 16-bit ADC. The Digital output DATA [15:0] were put into ADCD [15:0]. The ADC the block diagram show in Fig. 17-1

The ADC interrupt vector is 53H.

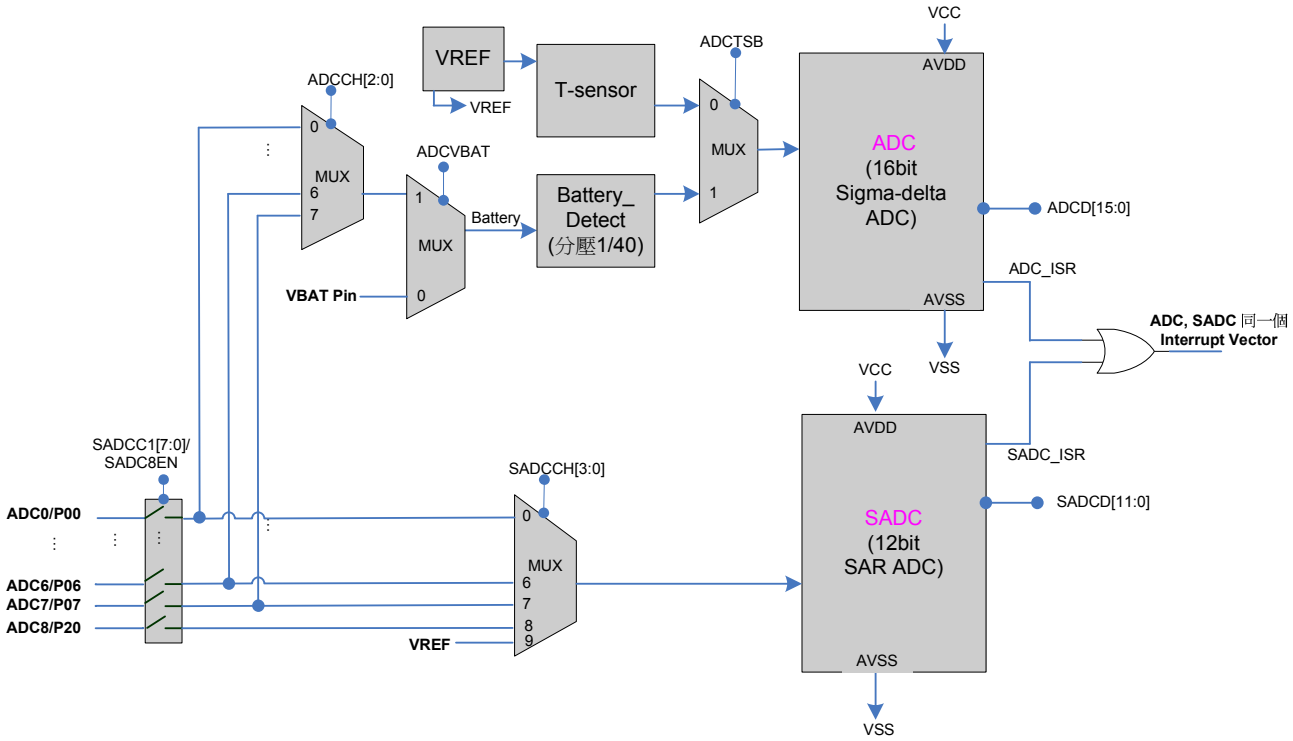


Fig. 17-1: ADC Analog to Digital converter operation set

The ADC SFR show as below:

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
ADC											
SADCC1	SADC Control register 1	FFF0h	SADC7EN	SADC6EN	SADC5EN	SADC4EN	SADC3EN	SADC2EN	SADC1EN	SADC0EN	00H
ADCC2	ADC Control register 2	FFE8h	Start	-	FFS	ADCVBAT	ADCMODE	ADCCH[2:0]			00H
ADCDH	ADC data high byte	FFE9h	ADCDH [7:0]								00H
ADCDL	ADC data low byte	FFEAh	ADCDL [7:0]								00H

Mnemonic: SADCC1 **Address: FFF0H**

7	6	5	4	3	2	1	0	Reset
SADC7EN	SADC6EN	SADC5EN	SADC4EN	SADC3EN	SADC2EN	SADC1EN	SADC0EN	00H

SADC7EN: SADC channel 7 enable.

0: Disable SADC channel 7

1: Enable SADC channel 7

SADC6EN: SADC channel 6 enable.
0: Disable SADC channel 6
1: Enable SADC channel 6
SADC5EN: SADC channel 5 enable.
0: Disable SADC channel 5
1: Enable SADC channel 5
SADC4EN: SADC channel 4 enable.
0: Disable SADC channel 4
1: Enable SADC channel 4
SADC3EN: SADC channel 3 enable.
0: Disable SADC channel 3
1: Enable SADC channel 3
SADC2EN: SADC channel 2 enable.
0: Disable SADC channel 2
1: Enable SADC channel 2
SADC1EN: SADC channel 1 enable.
0: Disable SADC channel 1
1: Enable SADC channel 1
SADC0EN: SADC channel 0 enable.
0: Disable SADC channel 0
1: Enable SADC channel 0

Mnemonic: ADCC2 **Address: FFE8h**

7	6	5	4	3	2	1	0	Reset
START	FFS[1:0]		ADCVBAT	ADCMODE	ADCCH[2:0]			00H

START When this bit is set, the ADC will be start conversion.
(SW trigger conversion)
FFS[1:0] Frequency of FS
00: FS = 1MHz.
01: FS = 1.67MHz.
11: FS = 2.5MHz.
ADCVBAT MUX select
ADCVBAT = 0 - (default value)
MUX select VBAT(external Pin)
ADCVBAT = 1- MUX select ADC[7:0](external Pin)
ADCMODE Connect to T-sensor one_shot_en
0 = continuous mode(Normal mode)
1 = single-shot mode(one-shot mode)

ADCCH[2:0] ADC channel select.

ADCCH [2:0]	Channel
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Mnemonic: ADCDH **Address: FFE9h**

7	6	5	4	3	2	1	0	Reset
ADCD[15]	ADCD[14]	ADCD[13]	ADCD[12]	ADCD[11]	ADCD[10]	ADCD[9]	ADCD[8]	00H

Mnemonic: ADCDL **Address: FFEAh**

7	6	5	4	3	2	1	0	Reset
ADCD[7]	ADCD[6]	ADCD[5]	ADCD[4]	ADCD[3]	ADCD[2]	ADCD[1]	ADCD[0]	00H

ADCD[15:0]: ADC data register.

17. 12 bit SADC(SAR ADC)

The OB59A128A1 provides ten channels 12-bit ADC. The Digital output DATA [11:0] were put into SADCD[11:0]. The ADC SFR show as below:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
SADC											
SADCC1	SADC Control 1	FFF0H	SADC7EN	SADC6EN	SADC5EN	SADC4EN	SADC3EN	SADC2EN	SADC1EN	SADC0EN	00H
SADCC2	SADC Control 2	FFF1H	SSTART	SADJUST	SASHM	SASHC	SADCCH[3:0]				00H
SADCDH	SADC Data High	FFF2H	SADCDH [7:0]								00H
SADCDL	SADC Data Low	FFF3H	SADCDL [7:0]								00H
SADCCS	SADC Clock Select	FFF4H	TSBVREFEN	SADC8EN	-	SADCCS[4:0]					00H
SADCSH	SADC Sample and Hold Time	FFF5H	SADCSH[7:0]								00H

SADC for Calibration:

Mnemonic	Description	Indirect	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
SADCCAL	SADC Calibration	FFFFH	-	-	-	-	-	-	SCALEN	SCALST	00H
SADCOVS	SADC Overflow Status	FFFEH	SRUN_OV	SCAL_OV	SOVF						00H
SADCCT0	SADC Calibration Tolerance 0	FFF8H	SADCCT0 [7:0]								00H
SADCCT1	SADC Calibration Tolerance 1	FFF9H	SADCCT1 [7:0]								00H
SADCCT2	SADC Calibration Tolerance 2	FFFAH	SADCCT2 [7:0]								00H
SADCCT3	SADC Calibration Tolerance 3	FFFBH	SADCCT3 [7:0]								00H
SADCCT4	SADC Calibration Tolerance 4	FFFCH	SADCCT4 [7:0]								00H
SADCCT5	SADC Calibration Tolerance 5	FFFDH	SADCCT5 [7:0]								00H

Mnemonic: SADCC1 **Address: FFF0H**

7	6	5	4	3	2	1	0	Reset
SADC7EN	SADC6EN	SADC5EN	SADC4EN	SADC3EN	SADC2EN	SADC1EN	SADC0EN	00H

SADC7EN: SADC channel 7 enable.
0: Disable SADC channel 7
1: Enable SADC channel 7

SADC6EN: SADC channel 6 enable.
0: Disable SADC channel 6
1: Enable SADC channel 6

SADC5EN: SADC channel 5 enable.
0: Disable SADC channel 5
1: Enable SADC channel 5

SADC4EN: SADC channel 4 enable.
0: Disable SADC channel 4
1: Enable SADC channel 4

SADC3EN: SADC channel 3 enable.

0: Disable SADC channel 3

1: Enable SADC channel 3

SADC2EN: SADC channel 2 enable.

0: Disable SADC channel 2

1: Enable SADC channel 2

SADC1EN: SADC channel 1 enable.

0: Disable SADC channel 1

1: Enable SADC channel 1

SADC0EN: SADC channel 0 enable.

0: Disable SADC channel 0

1: Enable SADC channel 0

Mnemonic: SADCC2 **Address: FFF1H**

7	6	5	4	3	2	1	0	Reset
SSTART	SADJUST	SASHM	SASHC	SADCCH[3:0]				00H

SSTART: When this bit is set, the SADC will be start conversion.

SADJUST: Adjust the format of SADC conversion DATA.

0: (default value)

SADC data high byte ADCDH [7:0] = ADCD [11:4].

SADC data low byte ADCDL [3:0] = ADCD [3:0

1: SADC data high byte ADCDH [3:0] = ADCD [11:8].

SADC data low byte ADCDL [7:0] = ADCD [7:0].

SASHM: SADC sample and hold mode :

SASHM=0: SADC sampling time is controlled by hardware.

SASHM=1: SADC sampling time is controlled by firmware.

SASHC: SADC sample and hold control bit. This control bit for SASHM=1.

SASHC=0: Disable SADC sampling.

SASHC=1: Enable SADC sampling.

SADCCH[3:0]: SADC channel select.

SADCCH [3:0]	Channel	
0000	0	ADC0/P00
0001	1	ADC1/P01
0010	2	ADC2/P02
0011	3	ADC3/P03
0100	4	ADC4/P04
0101	5	ADC5/P05
0110	6	ADC6/P06

0111	7	ADC7/P07
1000	8	ADC8/P20
1001	9	VREF
others	--	--

SADJUST = 0:

Mnemonic: SADCDH **Address: FFF2H**

7	6	5	4	3	2	1	0	Reset
SADCD.11	SADCD.10	SADCD.9	SADCD.8	SADCD.7	SADCD.6	SADCD.5.	SADCD.4	00H

Mnemonic: SADCDL **Address: FFF3H**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	SADCD.3	SADCD.2	SADCD.1	SADCD.0	00H

SADJUST = 1:

Mnemonic: SADCDH **Address: FFF2H**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	SADCD.11	SADCD.10	SADCD.9	SADCD.8	00H

Mnemonic: SADCDL **Address: FFF3H**

7	6	5	4	3	2	1	0	Reset
SADCD.7	SADCD.6	SADCD.5	SADCD.4	SADCD.3	SADCD.2	SADCD.1	SADCD.0	00H

SADCD[11:0]: SADC data register.

Mnemonic: SADCSH **Address: FFF5H**

7	6	5	4	3	2	1	0	Reset
SADCSH[7:0]								00H

SADCSH[7:0]: SADC sample and hold time register. This register for SASHM=0.

Mnemonic: SADCCS **Address: FFF4H**

7	6	5	4	3	2	1	0	Reset
TSBVREFEN	SADC8EN	-	SADCCS[4:0]					00H

TSBVREFEN: TSB VREF voltage enable

0: Disable

1: Enable

SADC8EN: SADC channel 8 enable.

0: Disable SADC channel 8

1: Enable SADC channel 8

SADCCS[4:0]: SADC clock select.

$$SADC\_Clock = \frac{\text{Fclk}}{6 \times (SADCCS[4:0] + 1)}$$

SASHM=0 , SADCSH=0x00:

$$SADC\_Conversion\_Rate = \frac{\text{SADC\_Clock}}{16}$$

SASHM=0 , SADCSH≠0x00:

$$SADC\_Conversion\_Rate = \frac{\text{SADC\_Clock}}{19 + SADCSH[7:0]}$$

※Sample and hold time by hardware control decisions.

SASHM=1:

$$SADC\_Conversion\_Rate = \frac{\text{SADC\_Clock}}{16} + F/W\_Sampling\_Time$$

※Sample and hold time by firmware control decisions.

Mnemonic: SADCCAL **Indirect Address: FFFFH**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	SCALEN	SCALST	00H

SCALEN: SADC calibration enable

0: Disable

1: Enable

※ If SCALEN and SADCxEN both set to “1”, SADC execute conversion according to the calibrated parameter. It will cost some conversion time to complete SADC conversion.

SCALST: SADC calibration start
0: Calibration complete (Hardware will clear this bit automatically to indicate the calibration has been finished)
1: Start calibration (Software set this bit to start calibration)

Mnemonic: SADCOVS **Indirect Address: FFFEH**

7	6	5	4	3	2	1	0	Reset
SRUN_OV	SCAL_OV	SOVF						00H

SRUN_OV: SRUN_OV Flag (Read only by default)
SCAL_OV: SCAL_OV Flag (Read only by default)
SOVF: SOverflow Flag (Read only by default)

Mnemonic: SADCCT0 **Indirect Address: FFF8H**

7	6	5	4	3	2	1	0	Reset
SADCCT0[7:0]								00H

SADCCT0[7:0]: SADC Calibration Data0 (Read only by defaul)

Mnemonic: SADCCT1 **Indirect Address: FFF9H**

7	6	5	4	3	2	1	0	Reset
SADCCT1[7:0]								00H

SADCCT1[7:0]: SADC Calibration Data1 (Read only by defaul)

Mnemonic: SADCCT2 **Indirect Address: FFFAH**

7	6	5	4	3	2	1	0	Reset
SADCCT2[7:0]								00H

SADCCT2[7:0]: SADC Calibration Data2 (Read only by defaul)

Mnemonic: SADCCT3 **Indirect Address: FFFBH**

7	6	5	4	3	2	1	0	Reset
SADCCT3[7:0]								00H

SADCCT3[7:0]: SADC Calibration Data3 (Read only by defaul)

Mnemonic: SADCCT4 **Indirect Address: FFFCH**

7	6	5	4	3	2	1	0	Reset
SADCCT4[7:0]								00H

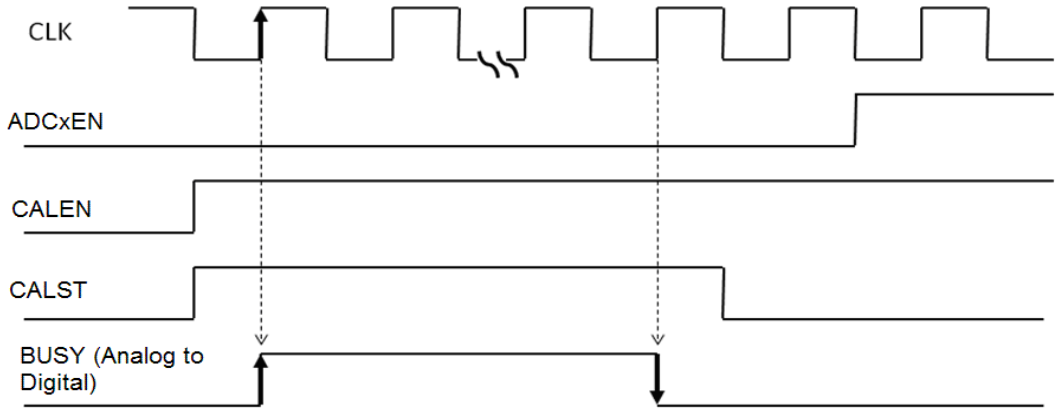
SADCCT4[7:0]: SADC Calibration Data4 (Read only by defaul)

Mnemonic: SADCCT5 **Indirect Address: FFFDH**

7	6	5	4	3	2	1	0	Reset
SADCCT5[7:0]								00H

SADCCT5[7:0]: SADC Calibration Data5 (Read only by defaul)

SADC Calibration Timing Chart



18. In-System Programming (Internal ISP)

The OB59A128A1 can generate flash control signal by internal hardware circuit. Users utilize flash control register, flash address register and flash data register to perform the ISP function without removing the OB59A128A1 from the system.

The OB59A128A1 provides internal flash control signals which can do flash program/chip erase/page erase/protect functions. User need to design and use any kind of interface which OB59A128A1 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

18.1 ISP service program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the OB59A128A1 for the ISP purpose.

The ISP service programs were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between OB59A128A1 and host device which output data to the OB59A128A1. For example, if user utilize UART interface to receive/Transmit data between OB59A128A1 and host device, the ISP service program should include baud rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.

The ISP service program can be initiated under OB59A128A1 active or idle mode. It can not be initiated under power down mode.

18.2 Lock Bit (N)

The Lock Bit N has two functions: one is for service program size configuration and the other is to lock the ISP service program space from flash erase function.

The ISP service program space address range $E000 to $FFFF. It can be divided as blocks of N*1K byte. (N=0 to 8). When N=0 means no ISP function, all of 64K byte flash memory can be used as program memory. When N=1 means ISP service program occupies 1K byte while the rest of 63K byte flash memory can be used as program memory. The maximum ISP service program allowed is 8K byte when N=8. Under such configuration, the usable program memory space is 64K byte.

After N determined, OB59A128A1 will reserve the ISP service program space downward from the top of the program address $FFFF. The start address of the ISP service program located at $Ex00 while x is depending on the lock bit N. Please see section 3.1 program memory diagram for this ISP service program space structure.

The lock bit N function is different from the flash protect function. The flash erase function can erase all of the flash memory except for the locked ISP service program space. If the flash not has been protected, the content of ISP service program still can be read. If the flash has been protected, the overall content of flash program memory space including ISP service program space can not be read. As given in Table 19-1.

Table 19-1 ISP code area

N	ISP service program address
0	No ISP service program
1	1.0 K bytes ($1_F800h ~ $1_FBFFh)
2	2.0 K bytes ($1_F400h ~ $1_FBFFh)
3	3.0 K bytes ($1_F000h ~ $1_FBFFh)
4	4.0 K bytes ($1_EC00h ~ $1_FBFFh)
5	5.0 K bytes ($1_E800h ~ $1_FBFFh)
6	6.0 K bytes ($1_E400h ~ $1_FBFFh)
7	7.0 K bytes ($1_E000h ~ $1_FBFFh)
8	8.0 K bytes ($1_DC00h ~ $1_FBFFh)

ISP service program configurable in N*1K byte (N= 0 ~ 8)

18.3 Program the ISP Service Program

After Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If user needs to erase the locked ISP service program, he can do it by writer only. User can not change ISP service program when OB59A128A1 was in system.

18.4 Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are four ways to do so:

(1) Blank reset. Power on reset with first flash address blank ($0000=#FFH) will load the PC with start address of ISP service program.

(2) Execute jump instruction can load the start address of the ISP service program to PC.

(3) Enter's ISP service program by hardware setting. User can force OB59A128A1 enter ISP service program by setting P14, P15 "active low" or P11 " active low" during power on reset period. In application system design, user should take care of the setting of P14,P15 or P11 at reset period to prevent OB59A128A1 from entering ISP service program.

(4) Enter's ISP service program by hardware setting, the P25(RXD) will be detected the two clock signals during power on reset period. The hardware reset includes power on reset and external pad reset. The hardware will issue to detect 2 clock signals after hardware reset.

During the strobe window, the hardware will detect the status of P14, P15, P11 and P25. If they meet one of above conditions, chip will switch to ISP mode automatically. After ISP service program executed, user need to reset the OB59A128A1, either by hardware reset or by WDT, or jump to the address $0000 to re-start the firmware program.

There are 6 kinds of entry mechanisms for user different applications. This entry method will select on the writer or ISP.

(1) First Address Blank. i.e. $0000 = 0xFF. And triggered by Power on reset signal.
(2) First Address Blank. i.e. $0000 = 0xFF. And triggered by PAD reset signal.
(3) P14,P15 (or P11) = 0. And triggered by Internal reset signal.
(4) P14,P15 (or P11) = 0. And triggered by Internal reset signal.
(5) P25 input 2 clocks. And triggered by Internal reset signal.
(6) P25 input 2 clocks. And triggered by Internal reset signal.

18.5 ISP register – TAKEY, IFCON, ISPFAH, ISPFAL, ISPFD and ISPFC

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
ISP function											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
IFCON	Interface Control register	8Fh	-	CDPR	-	-	Flag1A	Flag0B-	Flag0A-	ISPE	00H
ISPFAH	ISP Flash Address – High register	E1h	ISPFAH [7:0]								FFH
ISPFAL	ISP Flash Address - Low register	E2h	ISPFAL [7:0]								FFH
ISPFD	ISP Flash Data register	E3h	ISPFD [7:0]								FFH
ISPFC	ISP Flash Control register	E4h	EMF1	EMF2	EMF3	EMF4	ISPF.3	ISPF.2	ISPF.1	ISPF.0	00H
PSBS	PS Bank Select	B5h			COBK1	COBK0			IFBK.1	IFBK.0	
ISPBS	ISP Bank Select	ADh							ISPBS.1	ISPBS.0	01H

Mnemonic: TAKEY **Address: F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

ISP enable bit (ISPE) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the ISPE bit write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

Mnemonic: IFCON **Address: 8FH**

7	6	5	4	3	2	1	0	Reset
-	CDPR	-	-	Flag1A	Flag0B	Flag0A	ISPE	00H

The bit 0 (ISPE) of IFCON is ISP enable bit. User can enable overall OB59A128A1 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0. The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally. ISP registers ISPFAH, ISPFAL, ISPFD and ISPFC are read-only by default. Software must be set ISPE bit to 1 to enable these 4 registers write attribute.

Mnemonic: ISPFAH **Address: E1H**

7	6	5	4	3	2	1	0	Reset
ISPFAH[7:0]								FFH

ISPFAH [7:0]: Flash address-high for ISP function

Mnemonic: ISPFAL **Address: E2H**

7	6	5	4	3	2	1	0	Reset
ISPFAL[7:0]								FFH

ISPFAL [7:0]: Flash address-Low for ISP function

The ISPFAH & ISPFAL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

Mnemonic: ISPFD **Address: E3H**

7	6	5	4	3	2	1	0	Reset
ISPFD[7:0]								FFH

ISPFD [7:0]: Flash data for ISP function.

The ISPFD provide the 8-bit data register for ISP function.

Mnemonic: ISPFC **Address: E4H**

7	6	5	4	3	2	1	0	Reset
EMF1	EMF2	EMF3	EMF4	ISPF[3]	ISPF[2]	ISPF[1]	ISPF[0]	00H

EMF1: Entry mechanism (1) flag, clear by reset. (Read only)

EMF2: Entry mechanism (2) flag, clear by reset. (Read only)

EMF3: Entry mechanism (3) flag, clear by reset. (Read only)

EMF4: Entry mechanism (4) flag, clear by reset. (Read only)

ISPF [2:0]: ISP function select bit.

ISPF[3:0]	ISP function
0000	Byte program
0001	Chip protect
0010	Page erase
0011	Chip erase
0100	Write option
0101	Read option
0110	Erase option
0111	Finish flag (Write flag0b)
1000	Read main

One page of flash memory is 1K byte

18.5.1.1 Program Space Bank Select (PSBS)

Mnemonic: PSBS **Address: B5H**

7	6	5	4	3	2	1	0	Reset
		COBK[1]	COBK[0]			IFBK[1]	IFBK[0]	11H: normal run 33H: ISP entry

COBK[1:0]: Constant Operation Bank select

There bits select the upper 32KB bank for Constant Operation.

00: reserved. (logical addr[15]=0, HW select common bank)

01: bank0 (logical addr[15]=1)

10: bank1 (logical addr[15]=1)

11: bank2 (logical addr[15]=1)

IFBK[1:0]: Instruction Fetch Bank Select

There bits select the upper 32KB bank for instruction execution bank.

00: reserved. (logical addr[15]=0, HW select common bank)

01: bank0 (logical addr[15]=1)

10: bank1 (logical addr[15]=1)

11: bank2 (logical addr[15]=1)

18.5.1.2 ISP Bank Select (ISPBS)

Mnemonic: ISPBS **Address: ADH**

7	6	5	4	3	2	1	0	Reset
						ISPBS[1]	ISPBS[0]	01H

ISPBS [1:0]: ISP function Bank select

There bits select the upper 32KB bank for ISP flash write/read.

00: reserved. (logical addr[15]=0, HW select common bank)

01: bank0 (logical addr[15]=1)

10: bank1 (logical addr[15]=1)

11: bank2 (logical addr[15]=1)

The choice ISP function will start to execute once the software write data to ISPFC register.

To perform byte program/page erases ISP function, user need to specify flash address at first. When performing page erase function, OB59A128A1 will erase entire page which flash address indicated by ISPFAH & ISPFAL registers located within the page.

e.g. flash address: $ X000

page erase function will erase from $X000 to $X4FF

To perform the chip erase ISP function, OB59A128A1 will erase all the flash program memory except the ISP service program space. To perform chip protect ISP function, the OB59A128A1 flash memory content will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah    ; enable ISPE write attribute
ORL IFCON, #01H    ; enable OB59A128A1 ISP function
MOV ISPBS, #03H    ; select bank#2
MOV ISPFAH, #10H   ; set flash address-high, 10H
MOV ISPFAL, #05H   ; set flash address-low, 05H
MOV ISPFD, #22H    ; set flash data to be programmed, data = 22H
MOV ISPFC, #00H    ; start to program #22H to the flash address $1005H
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah    ; enable ISPE write attribute
ANL IFCON, #0FEH   ; disable OB59A128A1 ISP function
```

19. Comparator

OB59A128A1 had integrated Comparator in chip. When use it as comparator, the comparator output is logical one when positive input greater than negative input, otherwise the output is a zero. Following is the work of a block diagram of the comparator, as Fig. 20-1 shown. The user can set the operation mode with reference to the block diagram.

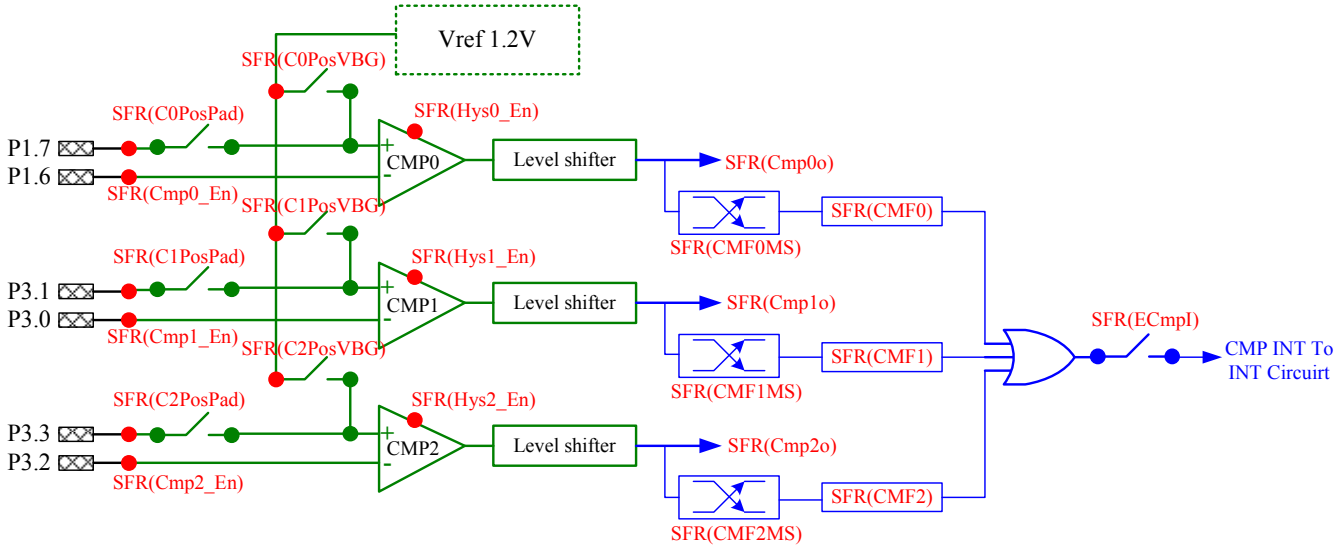


Fig. 20-1: Operation of Comparator Mode

Mnemonic	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Comparator											
OpPin	OpCmp Pin Select	F6h	-	Cmp0_En	C0PosVBG	C0PosPAD	-	Cmp1_En	C1PosVBG	C1PosPAD	~OP11
OpPin2	OpCmp Pin Select 2	CEh	-	Cmp2_En	C2PosVBG	C2PosPAD	-	-	-	-	~OP16
Cmp0CON	Comparator_0 control	FEh	Hys0En	Cmp0o	CMF0MS1	CMF0MS0	CMF0	-	-	-	00h
Cmp1CON	Comparator_1 control	FFh	Hys1En	Cmp1o	CMF1MS1	CMF1MS0	CMF1	-	-	-	00h
Cmp2CON	Comparator_2 control	CFh	Hys2En	Cmp2o	CMF2MS1	CMF2MS0	CMF2	-	-	-	00h

*OP11 and OP16 by writer programming set.

Mnemonic: OpPin **Address: F6h**

7	6	5	4	3	2	1	0	Reset
-	Cmp0_En	C0PosVBG	C0PosPad	-	Cmp1_En	C1PosVBG	C1PosPad	~OP11

Cmp0_En : Cmp0 enable.

Cmp0_En = 1 - Comparator_0 circuit enables and switch to corresponding signal in multi-function pin by HW automatically.

C0PosVBG : Select Comparator_0 positive input source

Cmp0_En = 1 - set positive input source as internal reference voltage (1.2V±10%)

C0PosPad: Select Comparator_0 positive input source

C0PosPad = 1 - set positive input source as external pin

Cmp1_En : Cmp1 enable.

Cmp1_En =1 - Comparator_1 circuit enables and switch to corresponding signal in multi-function pin by HW automatically.

C1PosVBG: Select Comparator_1 positive input source

C1PosVBG =1 - set positive input source as internal reference voltage (1.2V±10%)

C1PosPad: Select Comparator_1 positive input source

C1PosPad =1 - set positive input source as external pin

CmpxOut、Cmpx_En、CxPosVBG 及 CxPosPad setting table：

Cmpx_En	**CxPosVBG**	**CxPosPad**	**CmpxOut_En**	**Comparator**	
				CmpxPIn	**CmpxNIn**
0	X	X	X	IO	IO
1	0	1	0	IO	CMP
1	0	1	1	IO	IO
1	1	0	0	CMP	CMP
1	1	0	1	CMP	CMP

Mnemonic: OpPin2 **Address:CEh**

7	6	5	4	3	2	1	0	Reset
-	Cmp2_En	C2PosVBG	C2PosPad	-	-	-	-	~OP16

Cmp2_En : Cmp2 enable.

Cmp2_En= 1 - Comparator_2 circuit enable and switch to corresponding signal in multi-function pin by HW automatically.

C2PosVBG: Select Comparator_2 positive input source

C2PosVBG = 1- set positive input source as bandgap reference voltage

C2PosPad: Select Comparator_2 positive input source

C2PosPad =1 - set positive input source as external pin

Mnemonic: Cmp0CON **Address:FEh**

7	6	5	4	3	2	1	0	Reset
Hys0En	Cmp0o	CMF0MS1	CMF0MS0	CMF0	-	-	-	00h

Hys0En: Hysteresis function enable

Hys0En = 0 - disable Hysteresis at comparator_0 input

Hys0En = 1 - enable

Cmp0o: Comparator_0 output (read only)

Cmp0o = 0 - The positive input source was lower than negative input source

Cmp0o = 1 - The positive input source was higher than negative input source

CMF0MS[1:0] : CMF0(Comparator_0 Flag) setting mode select

CMF0MS[1:0] = 00 - CMF0 will be set when comprator_0 output toggle

CMF0MS[1:0] = 01 - CMF0 will be set when comprator_0 output rising

CMF0MS[1:0] = 10 - CMF0 will be set when comprator_0 output falling

11: reserved

CMF0: Comparator_0 Flag

This bit is setting by hardware according to meet CMF0MS [1:0] select condition.

This bit must clear by software.

Mnemonic: Cmp1CON **Address:FFh**

7	6	5	4	3	2	1	0	Reset
Hys1En	Cmp1o	CMF1MS1	CMF1MS0	CMF1	-	-	-	00h

Hys1En: Hysteresis function enable

Hys1En = 0 - disable Hysteresis at comparator_1 input

Hys1En =1 - enable

Cmp1o: Comparator_1 output (read only)

Cmp1o = 0 - The positive input source was lower than negative input source

Cmp1o = 1 - The positive input source was higher than negative input source

CMF1MS[1:0] : CMF1(Comparator_1 Flag) setting mode select

CMF1MS[1:0] = 00 - CMF1 will be set when comprator_1 output toggle

CMF1MS[1:0] = 01 - CMF1 will be set when comprator_1 output rising

CMF1MS[1:0] = 10 - CMF1 will be set when comprator_1 output falling

CMF1MS[1:0] = 11 - reserved

CMF1: Comparator_1 Flag

This bit is setting by hardware according to meet CMF1MS [1:0] select condition.

This bit must clear by software.

Mnemonic: Cmp2CON **Address:CFh**

7	6	5	4	3	2	1	0	Reset
Hys2En	Cmp2o	CMF2MS1	CMF2MS0	CMF2	-	-	-	00h

Hys2En: Hysteresis function enable

Hys2En = 0 - disable Hysteresis at comparator_2 input

Hys2En = 1 - enable

Cmp2o: Comparator_1 output (read only)

Cmp2o = 0 - The positive input source was lower than negative input source

Cmp2o = 1 -The positive input source was higher than negative input source

CMF2MS[1:0] : CMF1(Comparator_2 Flag) setting mode select

CMF2MS[1:0] = 00 – CMF2 will be set when comprator_2 output toggle

CMF2MS[1:0] = 01 – CMF2 will be set when comprator_2 output rising

CMF2MS[1:0] = 10 – CMF2 will be set when comprator_2 output falling

CMF2MS[1:0] = 11 - reserved

CMF2: Comparator_2 Flag

This bit is setting by hardware according to meet CMF2MS [1:0] select condition.

This bit must clear by software.

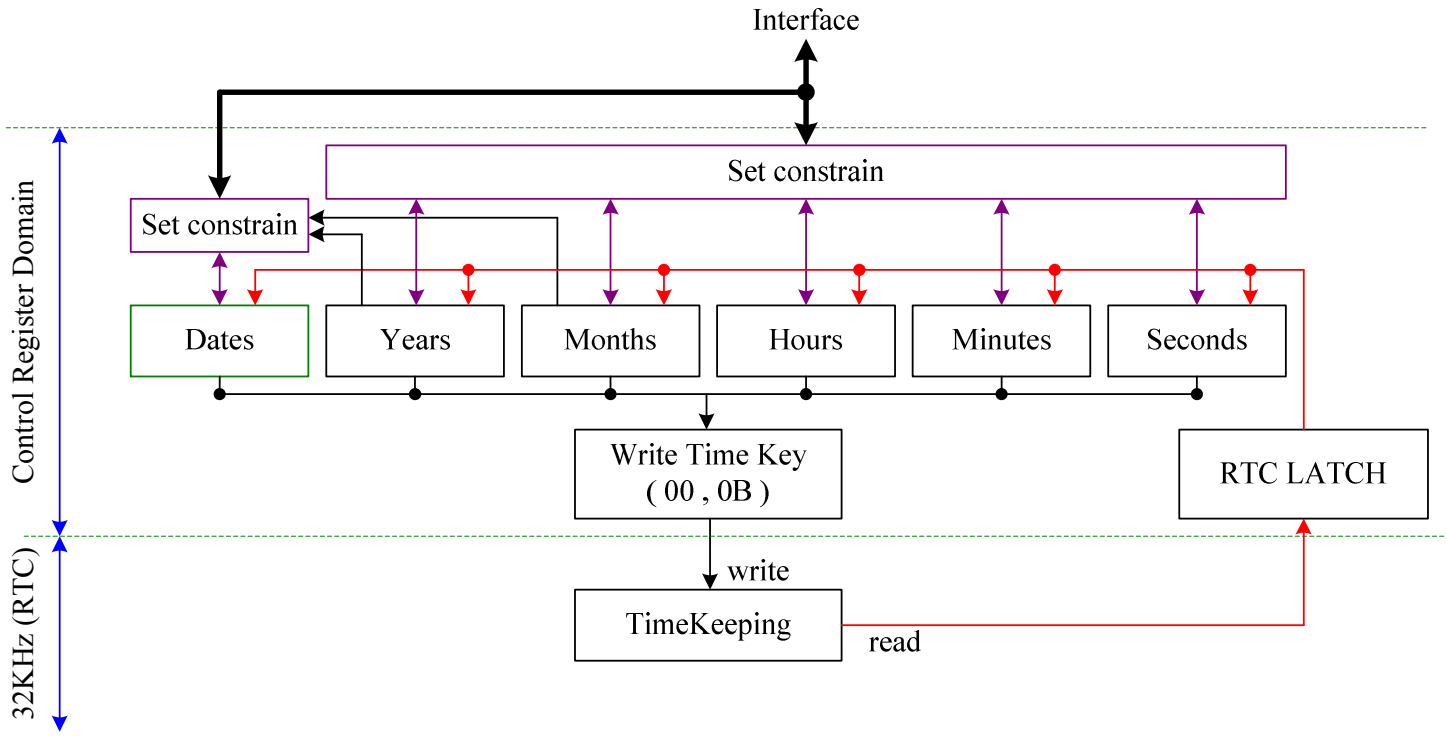
20. RTC

The On-Bright RTC low-current RTCs are timekeeping devices that consume an extremely low timekeeping current, which permits longer life from a power supply. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year through 2099.
The On-Bright RTC use an external 32.768kHz crystal. The devices support a high-ESR crystal, which broadens the pool of usable crystals for the device.
The RTC counter is always driven with the signal derived from the crystal oscillator.

RTC Register Map

Mnemonic	Description	Indirect	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
CLKCTR	Clock Control	FF00h	BTRY CTRL	BTRY RPT						RTCCG	00H
WTKEY	Write Time Key	FF01h	WTKEY[7:0]								00H
SECONDS	Seconds	FF02h		SECONDS[6:0]							00H
MINUTES	Minutes	FF03h		MINUTES[6:0]							00H
HOURS	Hours	FF04h			HOURS[5:0]						00H
DATES	Dates	FF05h			DATES[5:0]						01H
DAYS	Days	FF06h						DAYS[2:0]			00H
MONTHS	Months	FF07h				MONTHS[4:0]					01H
YEARS	Years	FF08h	YEARS[7:0]								00H
RTCLATCH	RTL Latch	FF09h	RTLLATCH[7:0]								00H
ADJUSTL	Adjust (Calibration)	FF0Ah	ADJUST[7:0]								00H
ADJUSTM	Adjust (Calibration)	FF0Bh	ADJUST[15:8]								00H
INTENABLE	Interrupt Enable	FF0Ch				ALMIE	DIE	HIE	MIE	SIE	00H
INTFLAG	Interrupt Flag	FF0Dh				ALMIF	DIF	HIF	MIF	SIF	00H
ALMS	Alarm Seconds	FF0Eh		ALMS[6:0]							00H
ALMM	Alarm Minutes	FF0Fh		ALMM[6:0]							00H
ALMH	Alarm Hours	FF10h			ALMH[4:0]						00H
Test Mode	Test Mode	FF1Eh					XTM	TESTSEL[2:0]			04H
CTRSTA	Control Status	FF1Fh	XPD	OSR	OSFDET	OSF				XAMP	00H
RCCH	Calibration Counter[23:16]	FF20h	RCC[23]	RCC[22]	RCC[21]	RCC[20]	RCC[19]	RCC[18]	RCC[17]	RCC[16]	00H
RCCM	Calibration Counter[15:8]	FF21h	RCC[15]	RCC[14]	RCC[13]	RCC[12]	RCC[11]	RCC[10]	RCC[9]	RCC[8]	00H
RCCL	Calibration Counter[7:0]	FF22h	RCC[7]	RCC[6]	RCC[5]	RCC[4]	RCC[3]	RCC[2]	RCC[1]	RCC[0]	00H
RCCS	Calibration Control/Status	FF23h	RCCE	O1HZE	CALSEL[1:0]		CLKDIV			RCCOV	00H

Time Register Block



Case 1 : Software modify All-Time value. Suggest to set from years to second. Because Data is relationship about Years and Months. For example, if year is leap year, the maximum dates of February is written 29.

Step :

(A) Write data 0x01 for clock control, **enable** clock (address : 00h).

(B) Write time information for control register (address : 02h ~ 08h).

(C) Write data 0x00 for write time key (address : 01h).

(D) Write data 0x0B for write time key (address : 01h).

(E) Write data 0x00 for clock control, **disable** clock (address : 00h).

Case 2 : Software modify Partial-Time value. Suggest to read from Timekeeping.

Step :

(A) Write data 0x01 for clock control, **enable** clock (address : 00h).

(B) Read RTCLATCH control register (address : 09h).

(C) Write time information for control register (address : 02h ~ 08h).

(D) Write data 0x00 for write time key (address : 01h).

(E) Write data 0x0B for write time key (address : 01h).

(F) Write data 0x00 for clock control, **disable** clock (address : 00h).

Case 3 : Software read Time value. At first read RTCLATCT control register. Hardware keep time

information from TimeKeeping to control register.

(A) Write data 0x01 for clock control, **enable** clock (address : 00h).

(B) Read RTCLATCH control register (address : 09h).

(C) Read time information for control register (address : 02h ~ 08h).

(D) Write data 0x00 for clock control, **disable** clock (address : 00h).

Time Register

Mnemonic: Clock Control **Address: FF00H**

7	6	5	4	3	2	1	0	Reset
BTRYCTRL	BTRYRPT						RTCCG	C0H

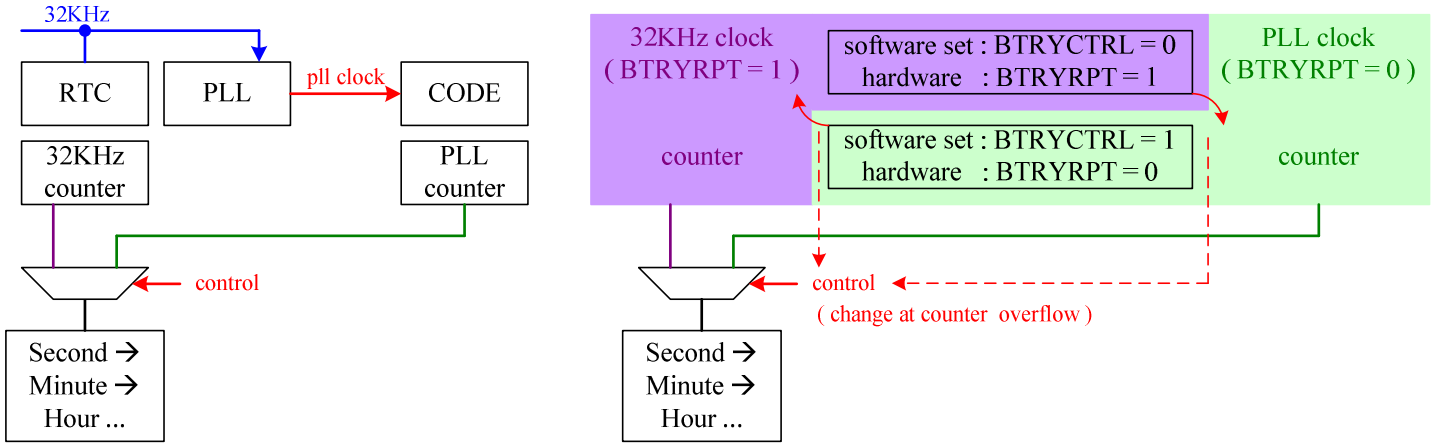
BTRYCTRL: Battery control

1 : power come from battery

BTRYRPT: Battery report

1 : RTC function change battery

BTRYCTRL & BTRYRPT relationship



RTCCG : RTC clock gate
Default MCU can't write/read RTC control register. Set RTCCG enable sfr bus clock.

Mnemonic: Write Time Key **Address: FF00H**

7	6	5	4	3	2	1	0	Reset
WTKEY.7	WTKEY.6	WTKEY.5	WTKEY.4	WTKEY.3	WTKEY.2	WTKEY.1	WTKEY.0	00H

Write key data flow: 0x00 & 0x0B

Mnemonic: Seconds **Address: FF02H**

7	6	5	4	3	2	1	0	Reset
	SECONDS.6	SECONDS.5	SECONDS.4	SECONDS.3	SECONDS.2	SECONDS.1	SECONDS.0	00H

Contains the BCD value of seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0~59.

Mnemonic: Minutes **Address: FF03H**

7	6	5	4	3	2	1	0	Reset
	MINUTES.6	MINUTES.5	MINUTES.4	MINUTES.3	MINUTES.2	MINUTES.1	MINUTES.0	00H

Contains the BCD value of minutes. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0~59.

Mnemonic: Hours **Address: FF04H**

7	6	5	4	3	2	1	0	Reset
		HOURS.5	HOURS.4	HOURS.3	HOURS.2	HOURS.1	HOURS.0	00H

Contains the BCD value of hours in 24-hour format. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0~23.

Mnemonic: Dates **Address: FF05H**

7	6	5	4	3	2	1	0	Reset
		DATES.5	DATES.4	DATES.3	DATES.2	DATES.1	DATES.0	00H

Contains the BCD value for the date of the month . Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 3. The range for the register is 1~31.

.

Mnemonic: Days **Address: FF06H**

7	6	5	4	3	2	1	0	Reset
					DAYS.2	DAYS.1	DAYS.0	00H

Lower nibble contains a value that correlate to day of the week. Day of the week is a ring counter that counts from 0 to 6 then returns to 0. The user must assign meaning to the day value, as the day is not integrated with the date.

Mnemonic: Months **Address: FF07H**

7	6	5	4	3	2	1	0	Reset
			MONTHS.4	MONTHS.3	MONTHS.2	MONTHS.1	MONTHS.0	00H

Contains the BCD digits for the months. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1~12.

.

Mnemonic: Years **Address: FF08H**

7	6	5	4	3	2	1	0	Reset
YEARS.7	YEARS.6	YEARS.5	YEARS.4	YEARS.3	YEARS.2	YEARS.1	YEARS.0	00H

Contains the lower two BCD digits of the years. Lower nibble contains the value for years; upper nibble contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0-99.

Adjust (Calibration)

Mnemonic: **Address: FF0AH**

7	6	5	4	3	2	1	0	Reset
ADJUST.7	ADJUST.6	ADJUST.5	ADJUST.4	ADJUST.3	ADJUST.2	ADJUST.1	ADJUST.0	00H

Mnemonic: **Address: FF0BH**

7	6	5	4	3	2	1	0	Reset
ADJUST. 15	ADJUST. 14	ADJUST. 13	ADJUST. 12	ADJUST. 11	ADJUST. 10	ADJUST.9	ADJUST.8	00H

ADJUST : Calibration value. (2's complement)

other reserve (SIGN except)

calibra_duration[1:0] : RTC compensation duration

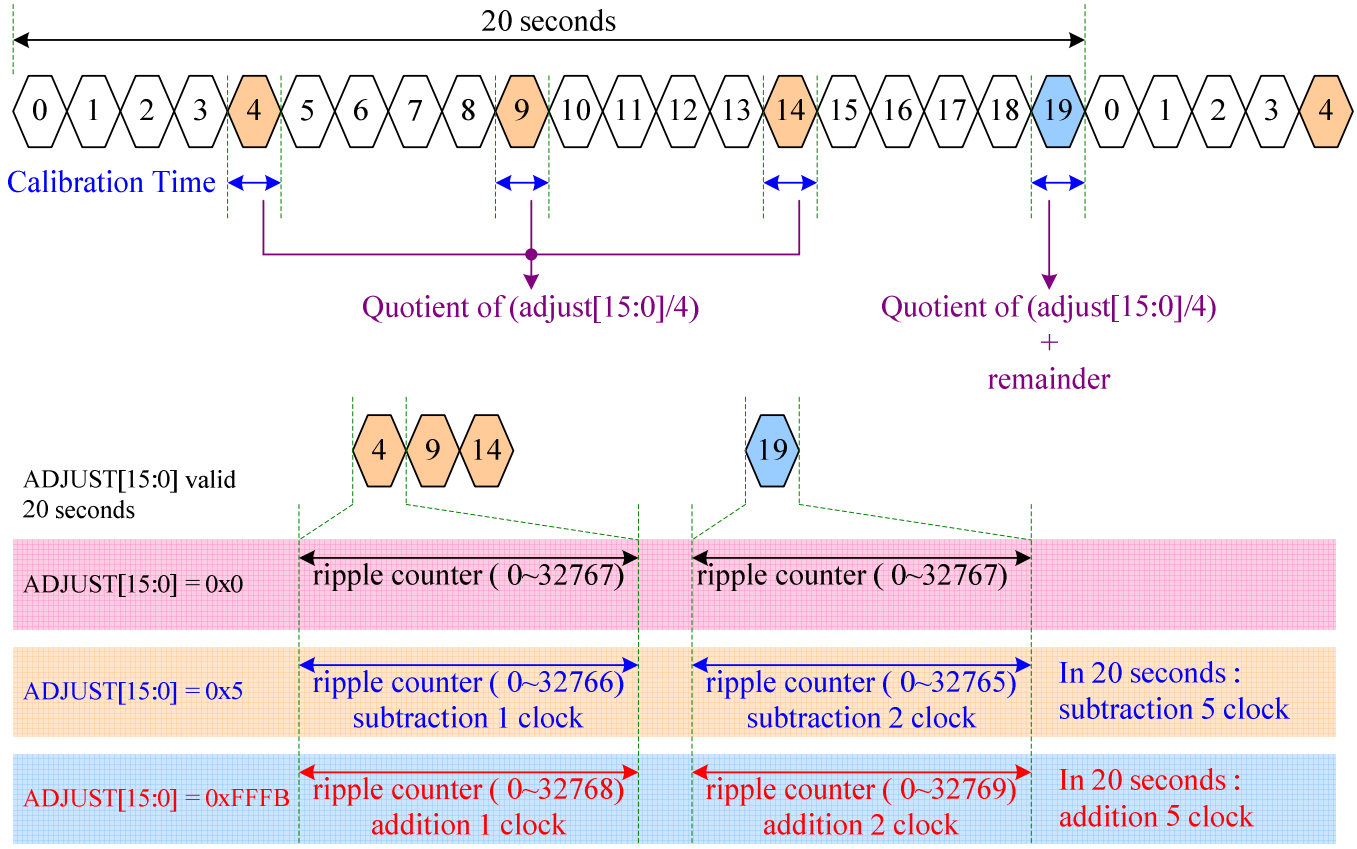
00 : 20s ADJUST[15:0] valid

01 : 30s ADJUST[15:0] valid

10 : 60s ADJUST[15:0] valid

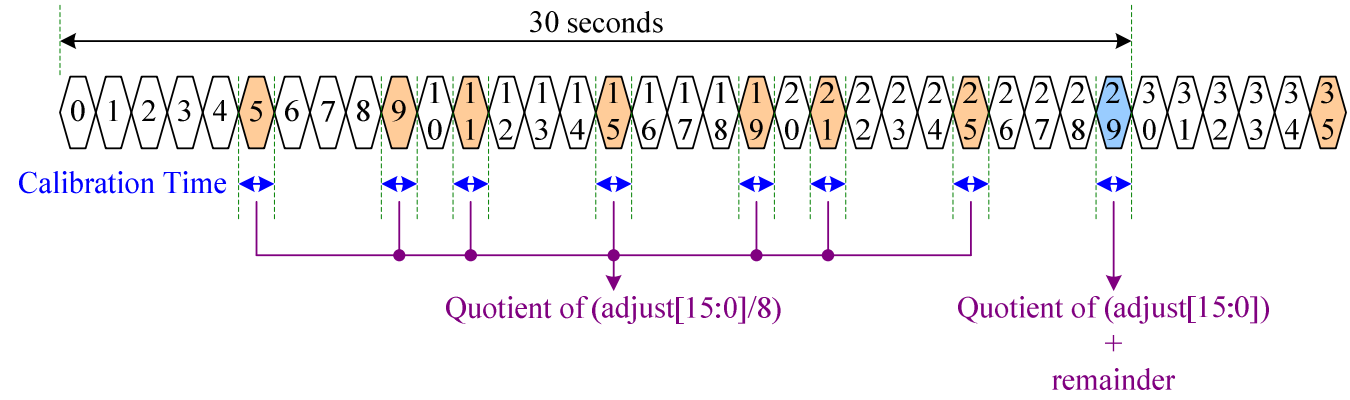
11 : 120s ADJUST[15:0] valid

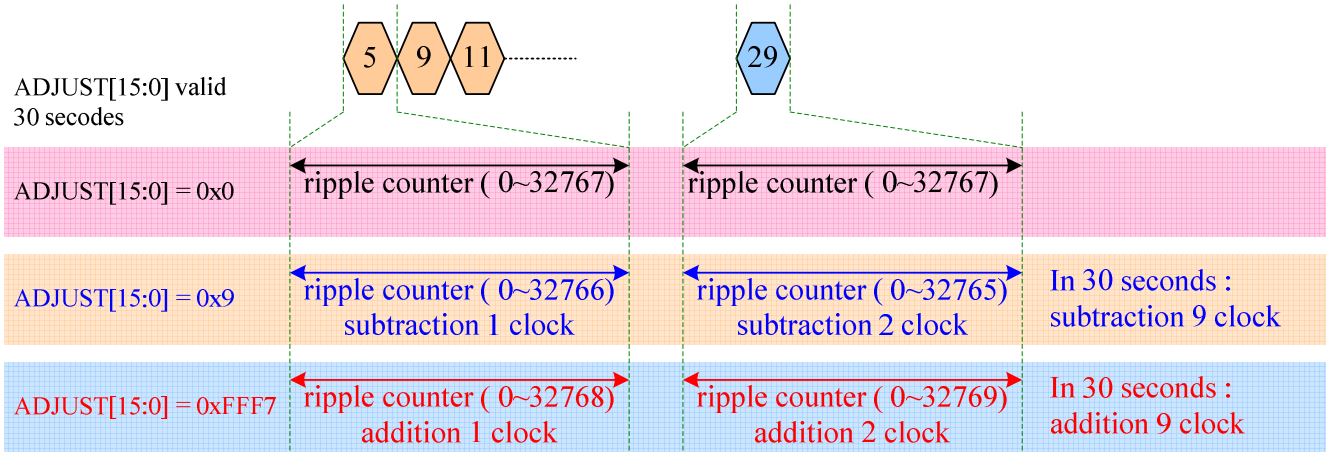
20 Second Calibration Timing



Register Set Condition	second counter (32KHz)		
	04, 09, 14 second 24, 29, 34 second 44, 49, 54 second	19 second 39 second 59 second	Other
ADJUST[15:0] = 0x0000	32768 clock	32768 clock	32768 clock
ADJUST[15:0] = 0x0001	32768 clock	32767 clock	
ADJUST[15:0] = 0x0FFF	31745 clock	31742 clock	
ADJUST[15:0] = 0xFFFF	32768 clock	32769 clock	
ADJUST[15:0] = 0xF001	33791 clock	33794 clock	

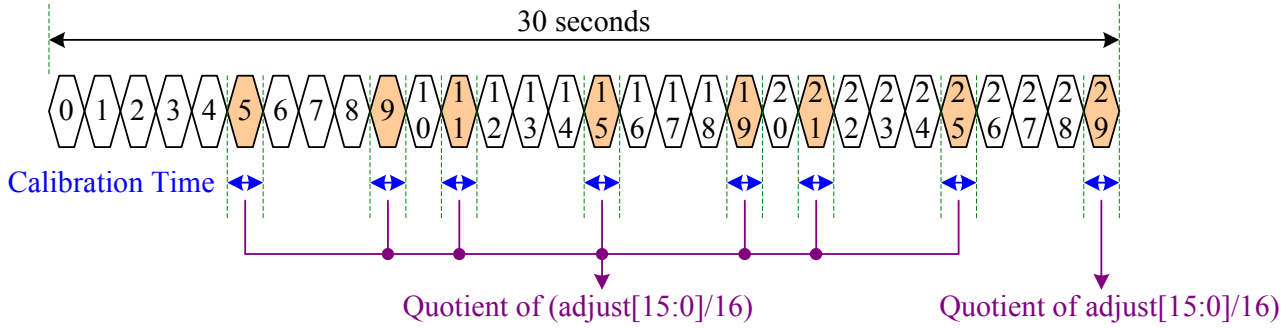
30 Second Calibration Timing

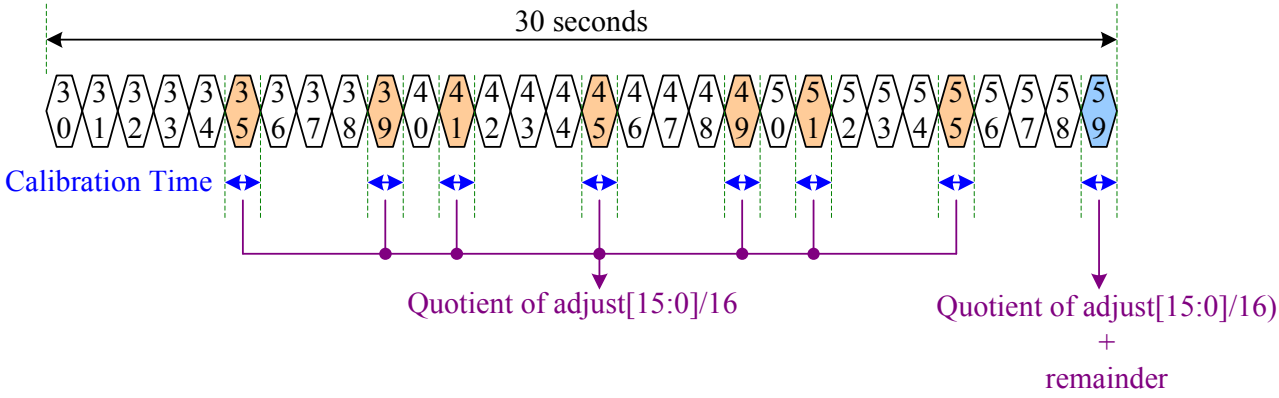


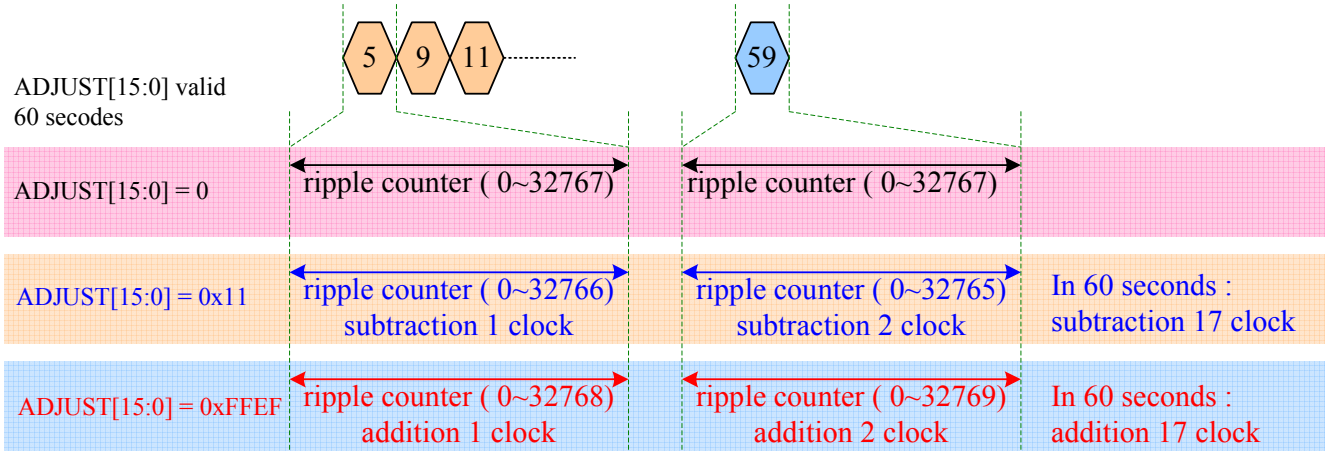


Register Set Condition	second counter (32KHz)		
	05, 09, 11, 15, 19, 21, 25 second 35, 39, 41, 45, 49, 51, 55 second	29 second 59 second	Other
ADJUST[15:0] = 0x0000	32768 clock	32768 clock	32768 clock
ADJUST[15:0] = 0x0001	32768 clock	32767 clock	
ADJUST[15:0] = 0x1FFF	31745 clock	31738 clock	
ADJUST[15:0] = 0xFFFF	32768 clock	32769 clock	
ADJUST[15:0] = 0xE001	33791 clock	33798 clock	

60 Second Calibration Timing

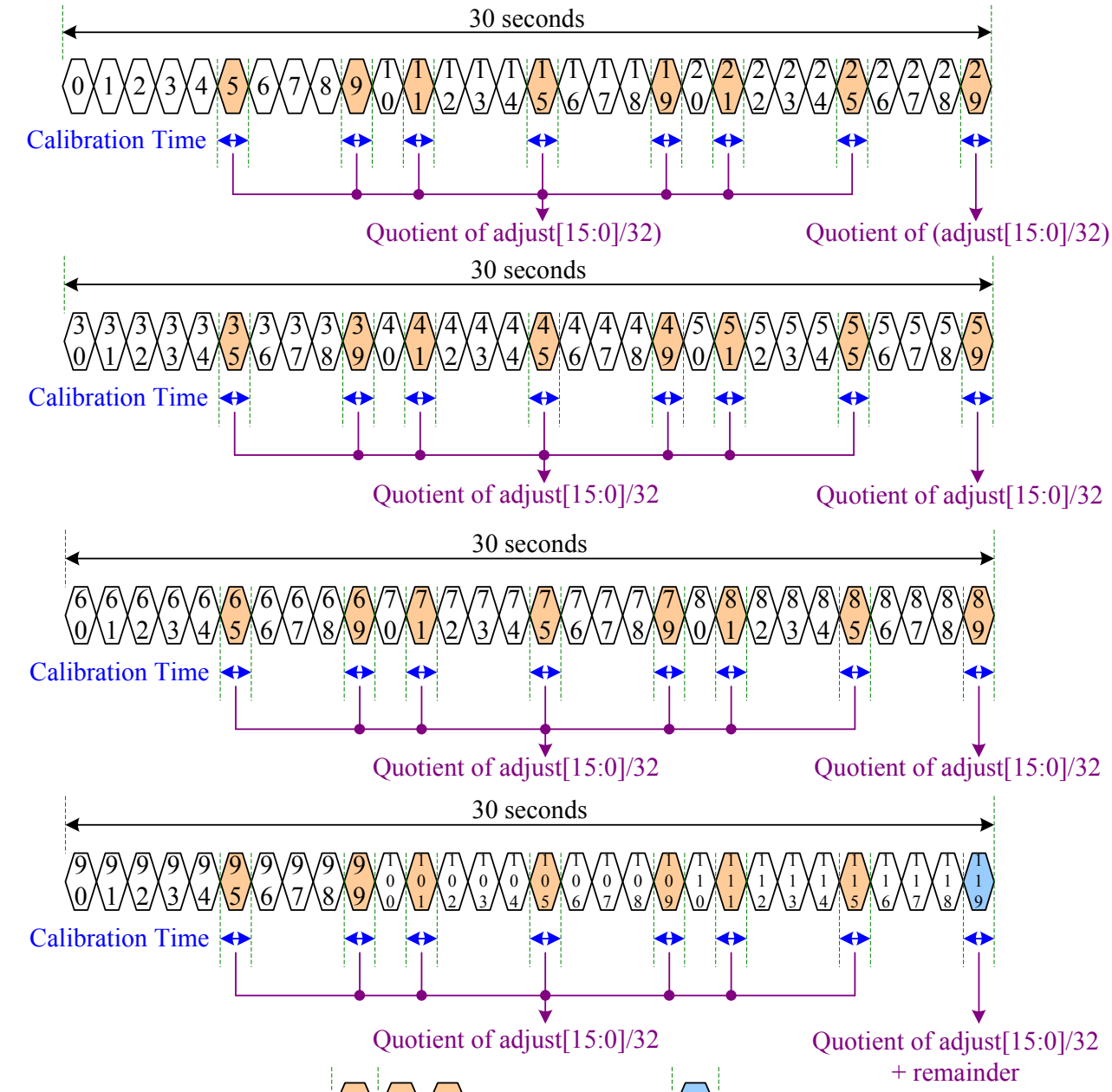


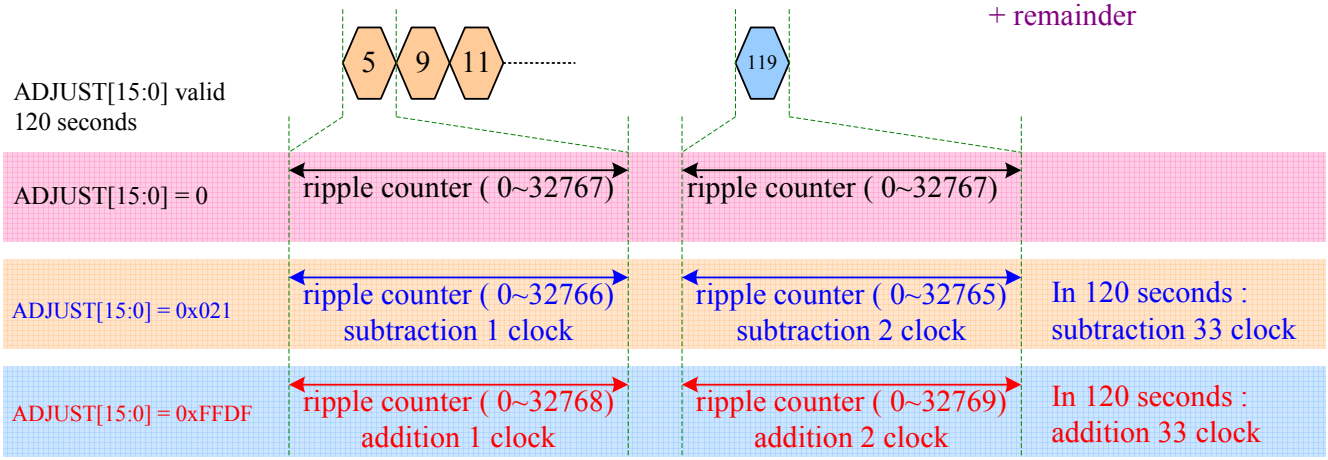




Register Set Condition	second counter (32KHz)		
	05, 09, 11, 15, 19, 21, 25, 29 second 35, 39, 41, 45, 49, 51, 55 second	59 second	Other
ADJUST[15:0] = 0x0000	32768 clock	32768 clock	32768 clock
ADJUST[15:0] = 0x0001	32768 clock	32767 clock	
ADJUST[15:0] = 0x1FFF	32257 clock	32242 clock	
ADJUST[15:0] = 0xFFFF	32768 clock	32769 clock	
ADJUST[15:0] = 0xE001	33279 clock	33294 clock	

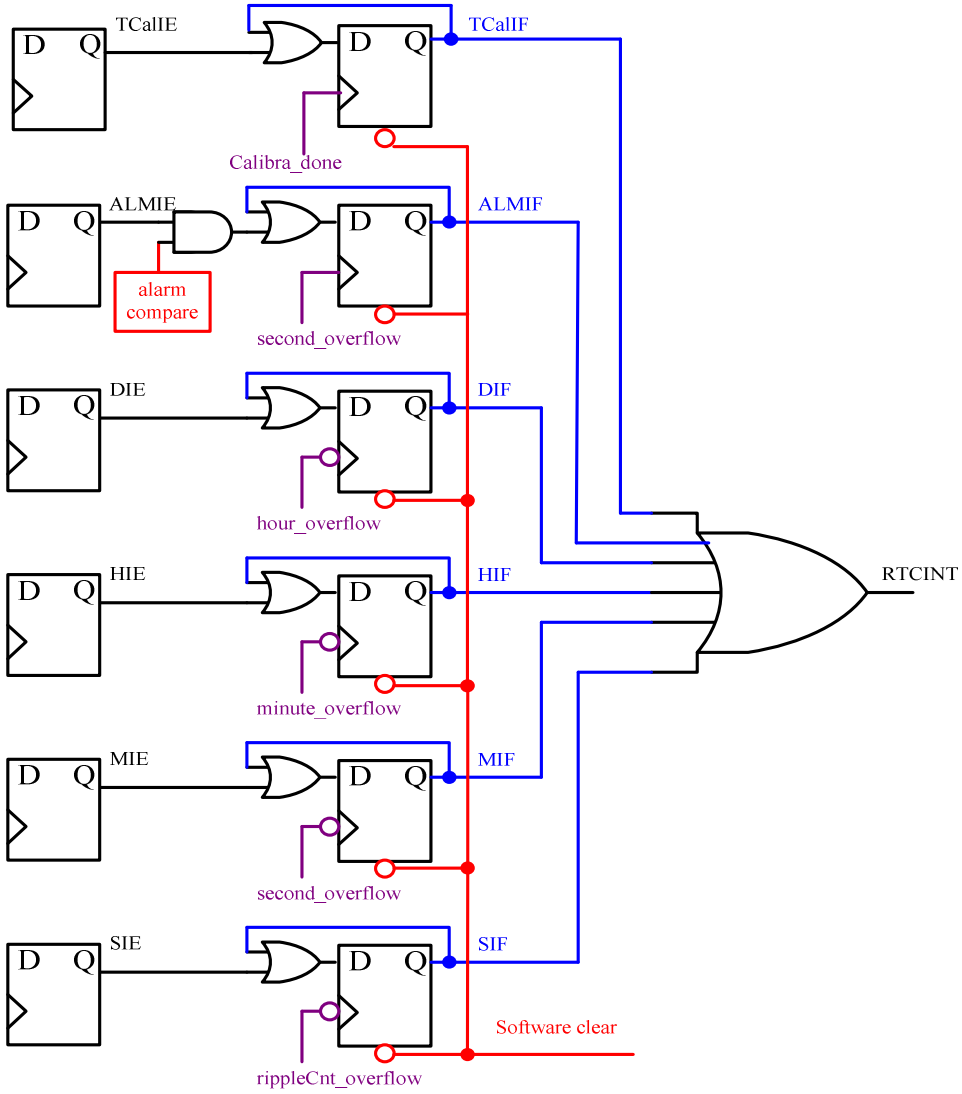
120 Second Calibration Timing





Register Set Condition	second counter (32KHz)		
	05, 09, 11, 15, 19, 21, 25, 29 second 35, 39, 41, 45, 49, 51, 55, 59 second 65, 69, 71, 75, 79, 81, 85, 89 second 95, 99, 101, 105, 109, 111, 115 second	119 second	Other
ADJUST[15:0] = 0x0000	32768 clock	32768 clock	32768 clock
ADJUST[15:0] = 0x0001	32768 clock	32767 clock	
ADJUST[15:0] = 0x1FFF	32513 clock	32482 clock	
ADJUST[15:0] = 0xFFFF	32768 clock	32769 clock	
ADJUST[15:0] = 0xE001	33023 clock	33054 clock	

Interrupt and Alarm Function Block



Mnemonic: Interrupt Enable **Address:FF0Ch**

7	6	5	4	3	2	1	0	Reset
		TCalIE	ALMIE	DIE	HIE	MIE	SIE	00h

Function interrupt Enable; write 1 enable interrupt, write 0 disable interrupt.

TCallIE: RTC Temperature Calibrate Interrupt Enable

ALMIE: Alarm Interrupt Enable.

DIE: Dates Interrupt Enable

HIE: Hours Interrupt Enable.

MIE: Minutes Interrupt Enable

SIE: Seconds Interrupt Enable.

Mnemonic: Interrupt Flag **Address:FF0Dh**

7	6	5	4	3	2	1	0	Reset
		TCalIF	ALMIF	DIF	HIF	MIF	SIF	00h

Function interrupt flag: Software write 0 clear flag, write 1 no function work. Interrupt enable and flag are independent. For example, if SIF (seconds flag) status is 1. Software clear SIE (seconds interrupt enable). SIE status always keep 1.

TCalIF: RTC Temperature Calibrate Interrupt flag

ALMIF: Alarm Interrupt flag.
If ALMIE (alarm interrupt enable) is written to logic 1, the ALMIF is the result of a match with seconds, minutes and hours.

DIF: Date Interrupt Flag
If DIF (dates interrupt enable) is written to logic 1. Hours change from 23 to 0, hardware set DIF flag from 0 to 1

HIF: Hours Interrupt Flag
If HIE (hours interrupt enable) is written to logic 1. Minute change from 59 to 0, hardware set HIF flag from 0 to 1

MIF: Minutes Interrupt Flag
If MIE (minutes interrupt enable) is written to logic 1. Second change from 59 to 0, hardware set MIF flag from 0 to 1.

SIF: Seconds Interrupt Flag
If SIE (seconds interrupt enable) is written to logic 1. Ripple count from 32767 to 0, hardware set SIF flag from 0 to 1

Mnemonic: Alarm Seconds **Address: FF0EH**

7	6	5	4	3	2	1	0	Reset
	ALMS.6	ALMS.5	ALMS.4	ALMS.3	ALMS.2	ALMS.1	ALMS.0	00H

Contains the alarm value for the seconds. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0~59.

Mnemonic: Alarm Minutes **Address: FF0FH**

7	6	5	4	3	2	1	0	Reset
	ALMM.6	ALMM.5	ALMM.4	ALMM.3	ALMM.2	ALMM.1	ALMM.0	00H

Contains the alarm value for the minutes.Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 5. The range for the register is 0~59.

Mnemonic: Alarm Hours **Address: FF10H**

7	6	5	4	3	2	1	0	Reset
		ALMH.5	ALMH.4	ALMH.3	ALMH.2	ALMH.1	ALMH.0	00H

Contains the alarm value for the hours. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0~23.

Mnemonic: Control / Status **Address: FF1FH**

7	6	5	4	3	2	1	0	Reset
XPD	OSR	OSFDET	OSF				XAMP	10H

XPD : Power down enable signal of crystal osc from RTC controller.
[0= Not PD **(def)** / 1= PD]

OSR : Output signal of Osc ready detection to RTC controller.
[1=ready / 0=unready]

OSFDET : Crystal osc failure detector enable signal from RTC controller.
[1=enable**(def)** / 0=disable]

OSF : Output signal of Osc failure detection to RTC controller.
[1=failure / 0=normal]

XAMP : Crystal osc amplifier SFR option from RTC controller
[1=enable / 0=disable**(def)**]

RTC Calibration

Mnemonic: Counter High Byte **Address: FF20H**

7	6	5	4	3	2	1	0	Reset
RCC[23]	RCC[22]	RCC[21]	RCC[20]	RCC[19]	RCC[18]	RCC[17]	RCC[16]	00H

Calibration counter for accurate 1HZ input.

.

Mnemonic: Counter Middle Byte **Address: FF21H**

7	6	5	4	3	2	1	0	Reset
RCC[15]	RCC[14]	RCC[13]	RCC[12]	RCC[11]	RCC[10]	RCC[9]	RCC[8]	00H

Calibration counter for accurate 1HZ input.

Mnemonic: Counter Low Byte **Address: FF22H**

7	6	5	4	3	2	1	0	Reset
RCC[7]	RCC[6]	RCC[5]	RCC[4]	RCC[3]	RCC[2]	RCC[1]	RCC[0]	00H

Calibration counter for accurate 1HZ input.

RTC Calibration Control/Status Register

Mnemonic: **Address: FF23H**

7	6	5	4	3	2	1	0	Reset
RCCE	O1HZE	CALSEL.1	CALSEL.0	CLKDIV			RCCOV	18H

RCCE : RTC Calibration Enable. (Sample 1Hz counter).

Software set “HIGH” for enable RTC calibration function. Function finish, hardware clear “LOW” for disable RTC calibration function

O1HZE : RTC 1HZ output enable.

1: enable RTC 1HZ output to pin IO1HZ

0: disable pin IO1HZ output function.

CALSEL : Calculate select.

00: 1 second

01: 2 second

10: 3 second

11: 4 second

CLKDIV : Clock divide.

1: divide 5

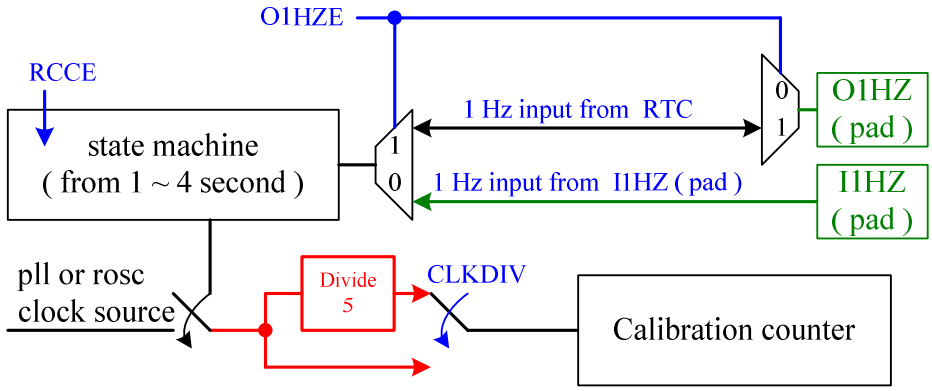
0: divide 1

RCCOV : Overflow flag of RTC calibration counter.

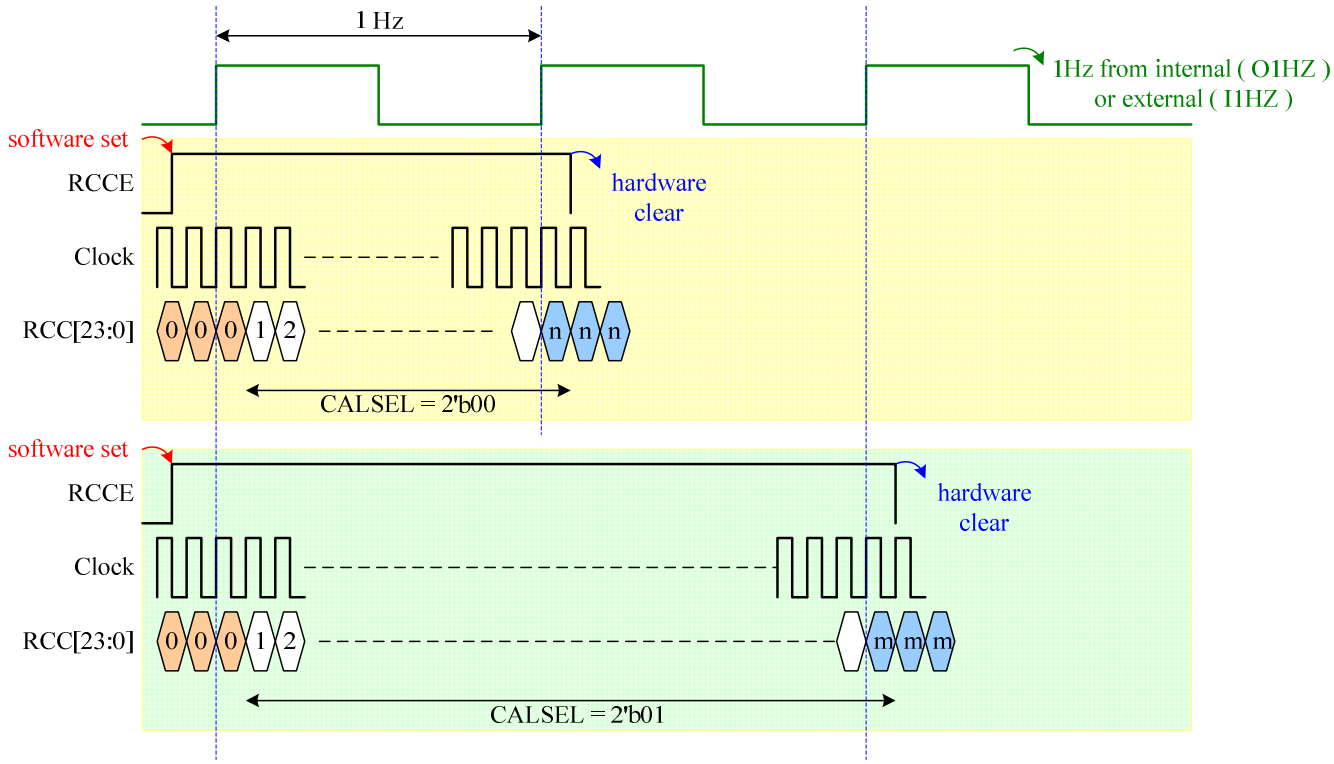
1: RCC overflow, set by HW.

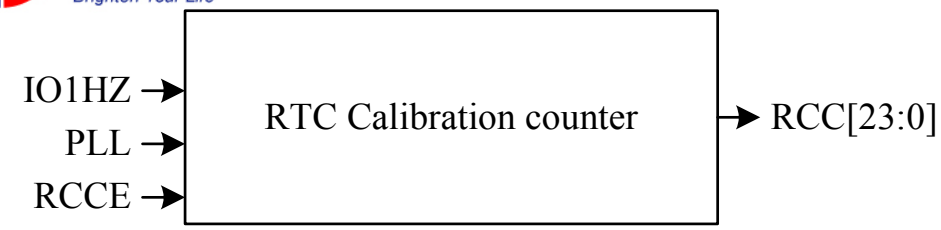
0: RCC not overflow, clear by SW.

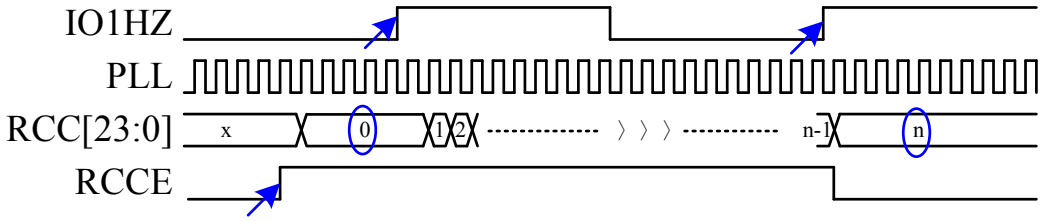
Calibration Function Diagram



Calibration Timing Waveform







Internal Analog Signal Monitor (IASM)

Mnemonic: **Address: FF30H**

7	6	5	4	3	2	1	0	Reset
				EN_VMON	CH_SEL[2]	CH_SEL[1]	CH_SEL[0]	07H

EN_VMON : 0: Disable internal signal monitor.
1: Enable internal signal monitor, the monitor signal is sent to VDCIN pad.

CH_SEL[2:0] : 0: RTCXT32K.VL
1: RTCXT32K.VH
2: PORLVD.VBG0P6
3: PORLVD.VBG1P2
4: VDET.VREF11
5: reserved
6: reserved
7: reserved

21. ISO7816

21.1 Feature

2 path IO TD-multiplex using one RTX-block, controlled by register

4 types 7816 clock output within 1~5MHz

Multi ETU period setup

Support Block Guard Time, Extra Guard Time setup

Auto RTX-repeat mode with error detector, 0~3 repeat times

3 kinds of ACK width, 1ETU, 1.5ETU, 2ETU

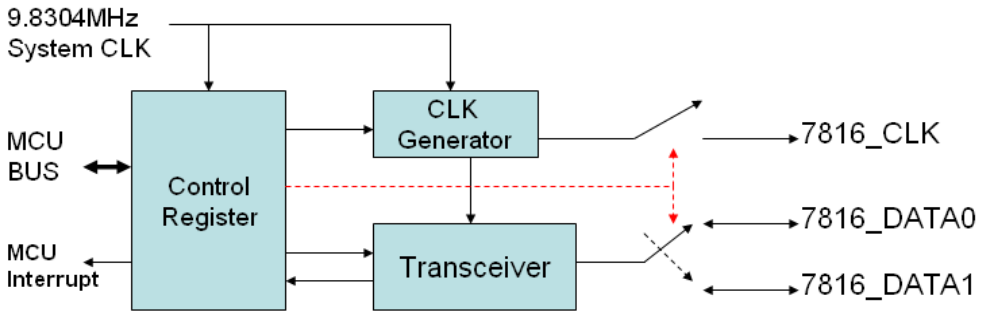
Low power mode by turning off output clock and control block

21.2 General Descriptions

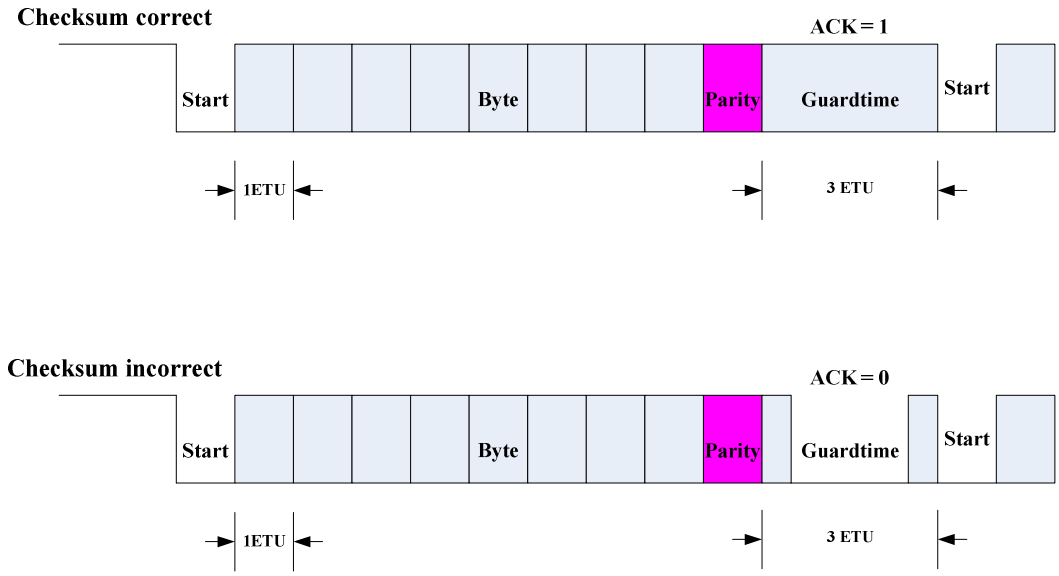
This module consist of a PHY-block based on ISO7816-3protocol.

21.3 Basic Structure and Operation

Module function

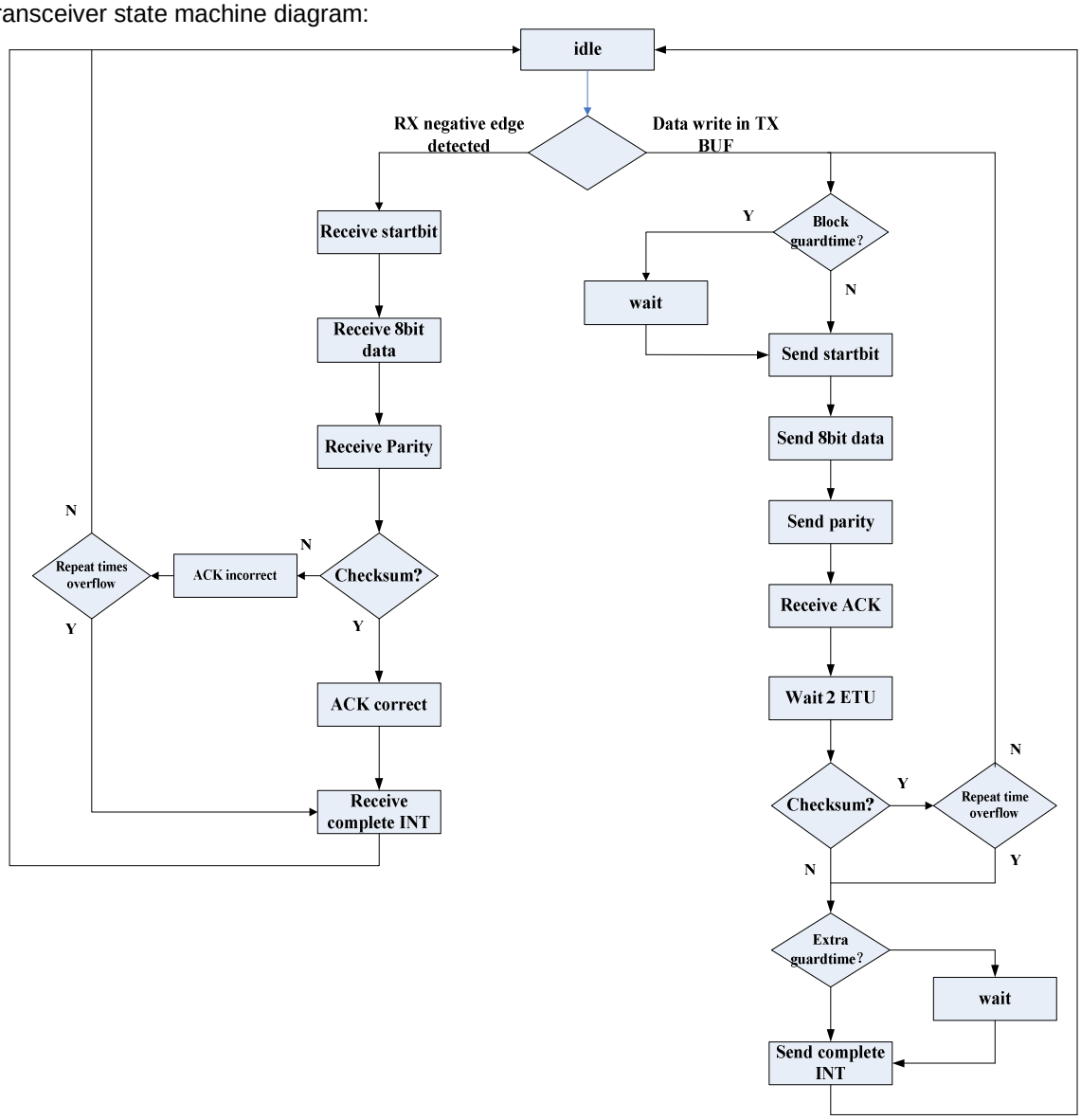


7816 protocol standard timing



It's defined that ETU (Elementary Time Unit) as time needed for send or receive 1 bit. A RTX frame consist of a start bit ,8 data bit ,1 parity bit and guard time. Once parity bit is received, the TX-ACK set high if checksum correct, otherwise TX-ACK set low if checksum incorrect. The length of ACK is about 1~2 ETU. Once the transmitter received ACK, based on the setting register the transmitter can re-send the last data frame or just ignore ACK to continue sending the next data frame.

Transceiver state machine diagram:



21.4 7816 Control Register

Mnemonic: CTL **Address:FE01H**

7	6	5	4	3	2	1	0	Reset
MOD_EN	CLK_EN	TXEN	RXEN	DSEL				00H

MOD_EN: 7816 function block enable control.

1 = 7816 function block enable

0 = 7816 function block disable'.

CLK_EN: 7816 clock output control

1 = 7816 clock output enable.

0 = 7816 clock output disable.

TXEN: Transmiter control.

1 = enable transmit data

0 = disable transmit data.

RXEN: Receiver control.

1 = enable receive data

0 = disable receive data.

DSEL: Data channel selection.

1 = select channel 1

0 = select channel 0.

Mnemonic: FRAME_CTL_1 **Address:FE02H**

7	6 5	4	3	2	1	0	Reset
PAR	REP_T[1:0]	TX_AREP_EN	RX_AREP_EN	CONV	BGTEN	-	38H

PAR: Parity mode selection in TX-state.

1 = even parity, when the numbers of '1' in 8bit transmit data are even, the 9th bit set '1', otherwise set '0'

0 = odd parity, when the numbers of '1' in 8bit transmit data are odd, the 9th bit set '0', otherwise set '1''.

REP_T[1:0]: When RX-ACK is '0' at TX mode, auto resend times selection from 0-3.

TX_AREP_EN: Auto resend enable in TX mode l.

1 = active when RX-ACK is '0'.resend times controlled by REP_T[1:0],from 0-3, 0 means not active. When resend completed, TX_ERR will be set according to the last ACK, and TX-INT set '1'

0 = disable.

RX_AREP_EN: Auto repeat-receive enable in RX mode.

1 = Once parity checksum error, ACK low will be send, RX_INT will not be active, RX state will be start again. Repeat times controlled by REP_T[1:0], from 0-3, 0 means don't repeat

receive. Once done, ACK will be sent according the last parity, RX_ERR will be set, RX_INT set '1'

0 = Once checksum error, send high ACK, RX_ERR set '1'，RX_INT set '1'.

CONV: Transmit coding selection.

1 = MSB first, parity bit reverse logic

0 = LSB first, parity bit normal logic.

BGTEN: BGT（Block Guard Time）control.

BGT is defined as the least time from RX mode to TX mode = 22ETU.

1 = BGT enable

0 = BGT disable.

Mnemonic: FRAME_CTL_2 **Address:FE03H**

7	6	5	4	3	2	1	0	Reset
						ERWD[1:0]		01H

ERWD[1:0]: When RX mode, ACK signal width

00 = 1 ETU

01 = 1.5 ETU

10 = 2 ETU

11 = 2 ETU

Default : 01 = 1.5 ETU

Mnemonic: CCLK **Address:FE04H**

7	6	5	4	3	2	1	0	Reset
						CCLK[1:0]		02H

CCLK[1:0] ： 7816 output clock frequency division

00 = 1/8 1.2288 MHz

01 = 1/2 4.9152 MHz

10 = 1/4 2.4576 MHz

11 = 1/6 1.6384 MHz

Mnemonic: ETUCLK **Address:FE05H**

7	6	5	4	3	2	1	0	Reset
DIV_M	PDIV[6:0]							0BH

DIV_M: Second division selection.

1 = div is 16， ETU_CLK = (fcclk/(PDIV+1)X16)'.

0 = div is 31， ETU_CLK = (fcclk/(PDIV+1)X31)

PDIV[6:0]: First division selection.

PS: 7816 protocol require F/D=372， so this register should be set as 0x0BH（DIV_M=0，. PDIV=11）before working.

Mnemonic: CEGT **Address:FE06H**

7	6	5	4	3	2	1	0	Reset
TXEGT[7:0]								00H

TXEGT[7:0] ： extra guard time after TX frame is sent，unit ETU

Mnemonic: DATA_BUF **Address:FE07H**

7	6	5	4	3	2	1	0	Reset
DATA_BUF[7:0]								00H

DATA_BUF[7:0] :

1. Data write in this register will active one send event.
2. After receive complete, data will be put in this register. Receive overflow INT will be set once new data arrive and old data still not be read.

Mnemonic: INT **Address:FE08H**

7	6	5	4	3	2	1	0	Reset
					TXIE	RXIE	OVIE	00H

TXIE: TX INT control.

1 = enable

0 = disable.

RXIE: RX INT control.

1 = enable

0 = disable.

OVIE: Receive overflow INT control.

1 = enable

0 = disable.

Mnemonic: INFO **Address:FE09H**

7	6	5	4	3	2	1	0	Reset
TX_BUSY	RX_BUSY		TX_ERR	RX_ERR	TXIF	RXIF	OVIF	00H

TX_BUSY: TX data busy flag, auto clear after transmit complete (read only).

1 = busy

0 = idle.

RX_BUSY: RX data busy flag, auto clear after receive complete (read only).

1 = busy

0 = idle.

TX_ERR: TX data parity checksum error flag.

1 = checksum error（write ’0’ to clear the flag, this bit will be updated after transmit done）

0 = checksum correct.

RX_ERR: RX data parity checksum error flag.

1 = checksum error（write ’0’ to clear the flag, this bit will be updated after receive done）

0 = checksum correct.

TXIF: TX INT flag, write ‘0’ to clear.

This flag will be set ’1’ after TX complete

RXIF: RX INT flag, write ‘0’ to clear.

OVIF: RX overflow flag, write ‘0’ to clear.

22. Temperature Sensor and Temperature Compensation

22.1 General Descriptions

The chip integrated with high precision temperature sensor and temperature compensation circuit . The measurement accuracy of the sensor is +-1℃ between -30℃ and 80℃. The frequency of external crystal will change with temperature variation and this will affect the accuracy of RTC inside. The compensation circuit is just used to eliminate the influence and the accuracy will be controlled below 10ppm after calibration（-30℃~80℃）

22.2 Register Descriptions

Mnemonic: TSBCTL **Address: FFE0h**

7	6	5	4	3	2	1	0	Reset
-	CHOP_EN	-	ADCTSB	SpeedEN[1:0]		-	PD	40H

CHOP_EN: 0 –

1 – Chopper enable(default value)

ADCTSB: MUX select

ADCTSB = 0 - (default value)

MUX select TSB(Temp Sensor)

ADCTSB = 1-

MUX select Battery_detect(or ADC[7:0] external Pin)

SpeedEN[1:0] ADC data output rate

(16K clock can be changed from SFR (16K/32K/64K) to speed up T-sensor testing)

00: output rate 8Hz

01: output rate 16Hz

10: output rate 32Hz

11: output rate 64Hz

PD: Power down TSB IP .

0 –Power down TSB.

1 – Enable TSB.

Mnemonic: TSB_VREF_V **Address: FFE1h**

7	6	5	4	3	2	1	0	Reset
-					VREF_V[2:0]			00H

VREF_V<2:0> Trimming VREF initial precision

Mnemonic: TSB_VREF_T **Address: FFE2h**

7	6	5	4	3	2	1	0	Reset
-				VREF_T[3:0]				00H

VREF_V<3:0> Trimming VREF temperature coefficient

Mnemonic: Calibra_en **Address: FF40h**

7	6	5	4	3	2	1	0	Reset
-							Calibra_en	00H

Calibra_en = 1 : RTC temperature compensation enable
= 0 : RTC RTC temperature compensation disable

Mnemonic: ref_h **Address: FF41h**

7	6	5	4	3	2	1	0	Reset
Ref_h[7:0]								00H

Ref_h[7:0] : REF magnitude translation value-high 8 bit

Mnemonic: ref_l **Address: FF42h**

7	6	5	4	3	2	1	0	Reset
Ref_l[7:0]								00H

Ref_l[7:0] : REF magnitude translation value-low 8 bit

Mnemonic: t_turn_flag **Address: FF43h**

7	6	5	4	3	2	1	0	Reset
-							t_turn_flag	00H

t_turn_flag : flag of turn temperature

Mnemonic: t_turn **Address: FF44h**

7	6	5	4	3	2	1	0	Reset
t_turn[7:0]								00H

t_turn[7:0] : turn temperature

Mnemonic: offset_turn **Address: FF45h**

7	6	5	4	3	2	1	0	Reset
offset_turn[7:0]								00H

offset_turn[7:0] : offset compensation at turn temperature

Mnemonic: cofe_a **Address: FF46h**

7	6	5	4	3	2	1	0	Reset
Cofe_a[15:8]								00H

Mnemonic: cofe_a **Address: FF47h**

7	6	5	4	3	2	1	0	Reset
Cofe_a[7:0]								00H

Cofe_a[15:0] : compensation coefficient -a

Mnemonic: cofe_b **Address: FF48h**

7	6	5	4	3	2	1	0	Reset
Cofe_b[15:8]								00H

Mnemonic: cofe_b **Address: FF49h**

7	6	5	4	3	2	1	0	Reset
Cofe_b[7:0]								00H

Cofe_b[15:0] : compensation coefficient -b

Mnemonic: cofe_c **Address: FF4Ah**

7	6	5	4	3	2	1	0	Reset
Cofe_c[15:8]								00H

Mnemonic: cofe_c **Address: FF4Bh**

7	6	5	4	3	2	1	0	Reset
Cofe_c[7:0]								00H

Cofe_c[15:0] : compensation coefficient -c

Mnemonic: fix_dis_a **Address: FF4Ch**

7	6	5	4	3	2	1	0	Reset
Fix_dis_a[7:0]								00H

Fix_dis_a[7:0] : temperature sensor fix value-a

Mnemonic: fix_dis_b **Address: FF4Dh**

7	6	5	4	3	2	1	0	Reset
Fix_dis_b[7:0]								00H

Fix_dis_b[7:0] : temperature sensor fix value-b

Mnemonic: fix_dis_c **Address: FF4Eh**

7	6	5	4	3	2	1	0	Reset
Fix_dis_c[7:0]								00H

Fix_dis_c[7:0] : temperature sensor fix value-c

Mnemonic: i_data_cvt_spc **Address: FF4Fh**

7	6	5	4	3	2	1	0	Reset
i_data_cvt_spc[7:0]								00H

i_data_cvt_spc : special temperature value input

Mnemonic: o_data_cvt_spc **Address: FF50h**

7	6	5	4	3	2	1	0	Reset
o_data_cvt_spc[7:0]								00H

o_data_cvt_spc : special temperature value output

Mnemonic: cvt_spc_avl **Address: FF51h**

7	6	5	4	3	2	1	0	Reset
-							cvt_spc_avl	00H

cvt_spc_avl : special temperature value output available

Mnemonic: t_data_cvt **Address: FF52h**

7	6	5	4	3	2	1	0	Reset
t_data_cvt [7:0]								00H

t_data_cvt : actual temperature value (sign number)

Mnemonic: data_calibra **Address: FF53h**

7	6	5	4	3	2	1	0	Reset
Data_calibra [15:8]								00H

Mnemonic: data_calibra **Address: FF54h**

7	6	5	4	3	2	1	0	Reset
Data_calibra [7:0]								00H

Data_calibra [15:0] : RTC calibration number

Mnemonic: calibra_done **Address: FF55h**

7	6	5	4	3	2	1	0	Reset
-							calibra_done	00H

calibra_done : flag of RTC calibration done

Mnemonic: calibra_ duration **Address: FF56h**

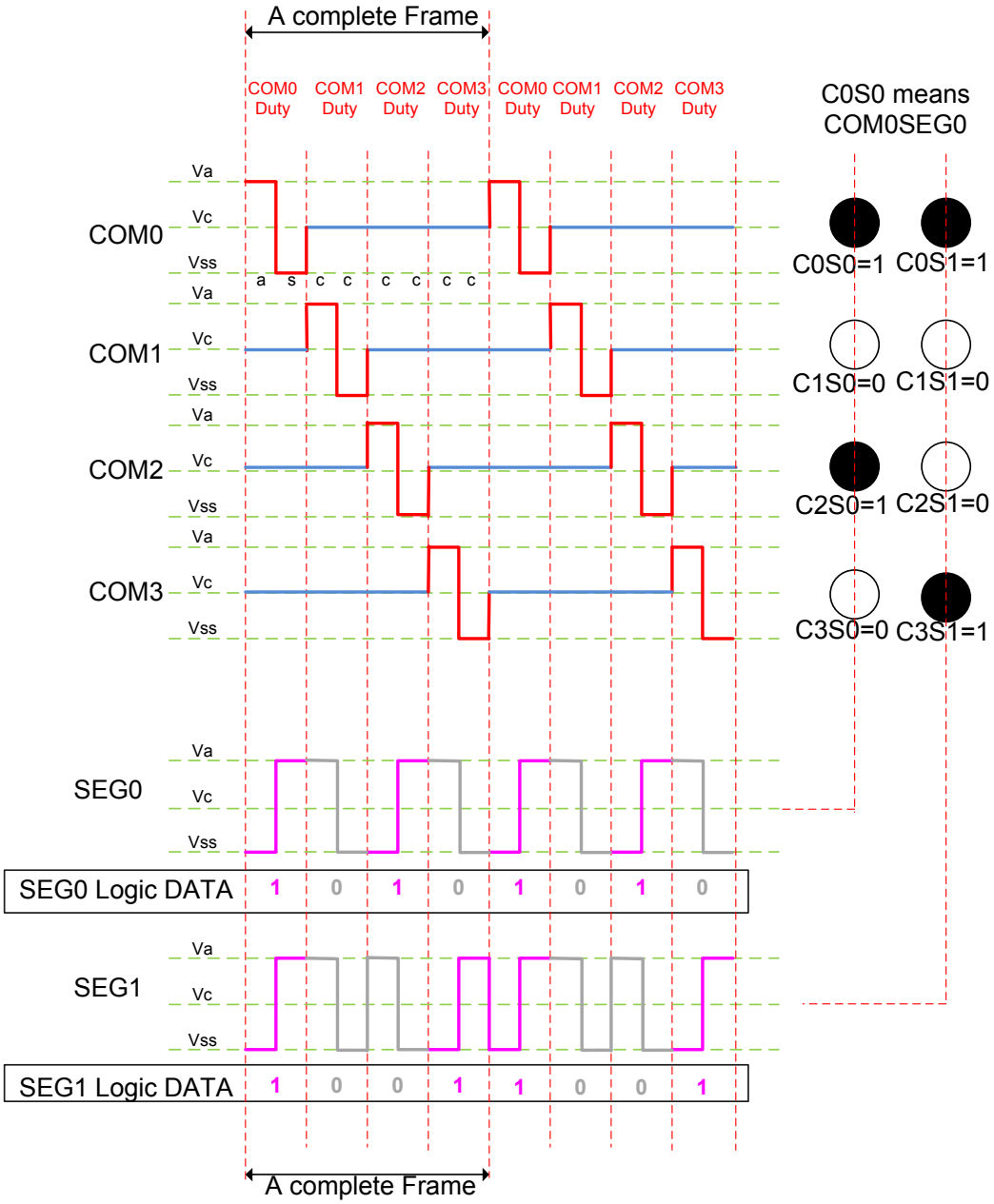
7	6	5	4	3	2	1	0	Reset
-						calibra_duration[1:0]		00H

calibra_duration[1:0] : RTC calibration duration
00 : 20 seconds(default)
01 : 30 seconds
10 : 60 seconds
11 : 120 seconds

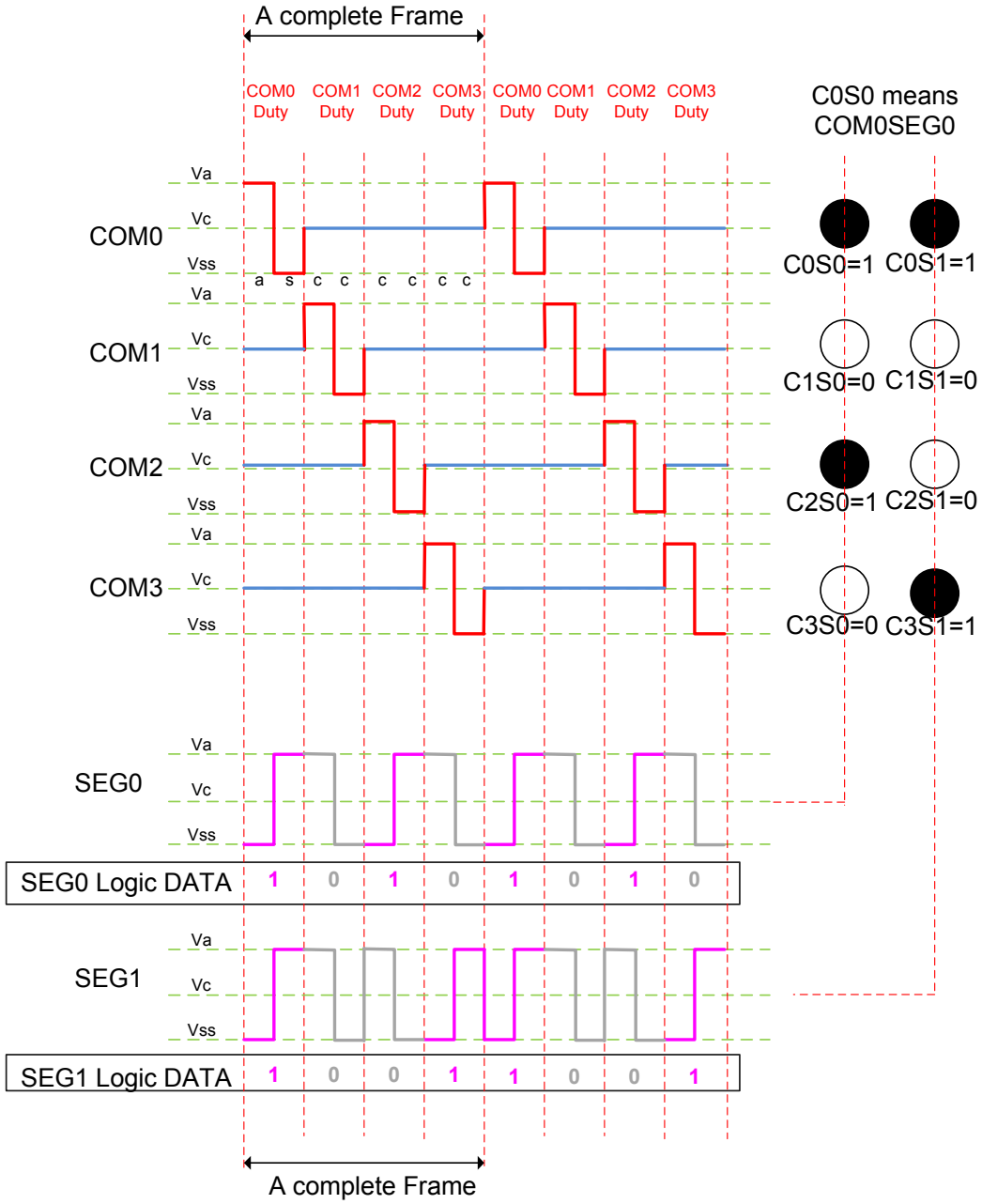
23. LCD

LCD selectable duty : 1/8, 1/6, 1/4 , 1/3 , 1/2 or full-duty
LCD selectable 1/4, 1/3, 1/2 bias
LCD maximum SEG-driver 36 pins, COM-driver 8 pin
Support Type A, Type B waveform

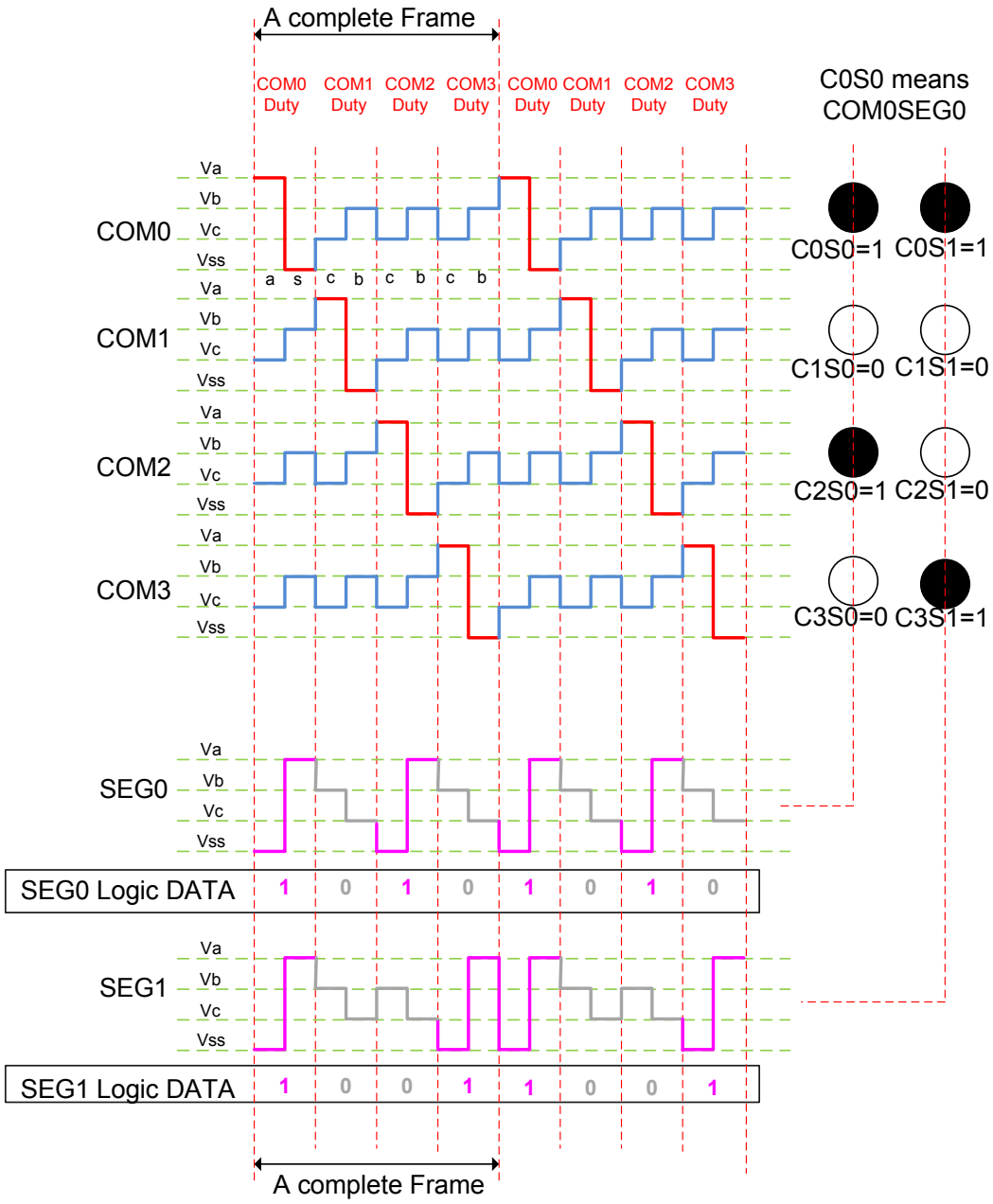
23.1 LCD drive waveform



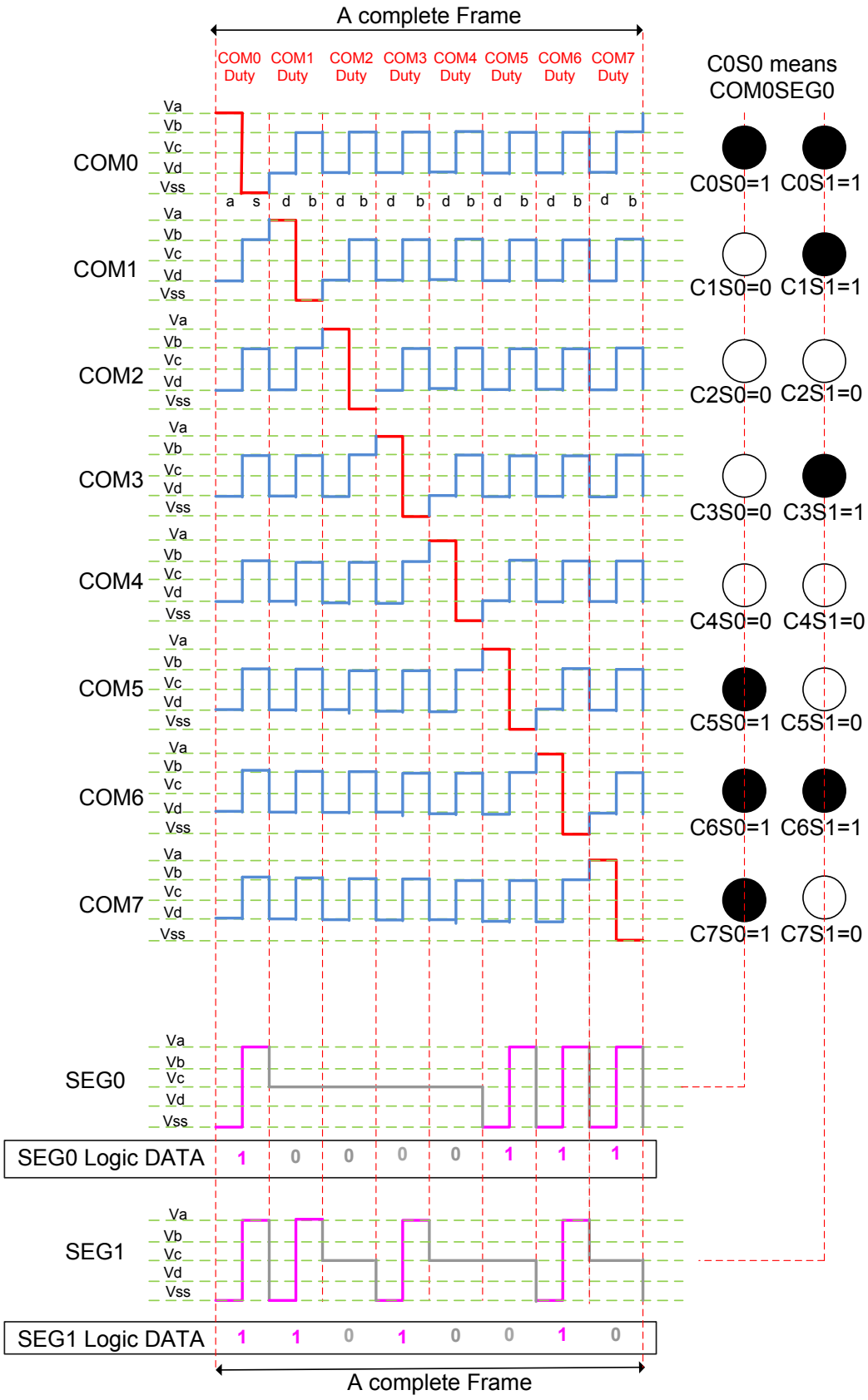
1/2 bias, 1/4 duty LCD waveform Type A



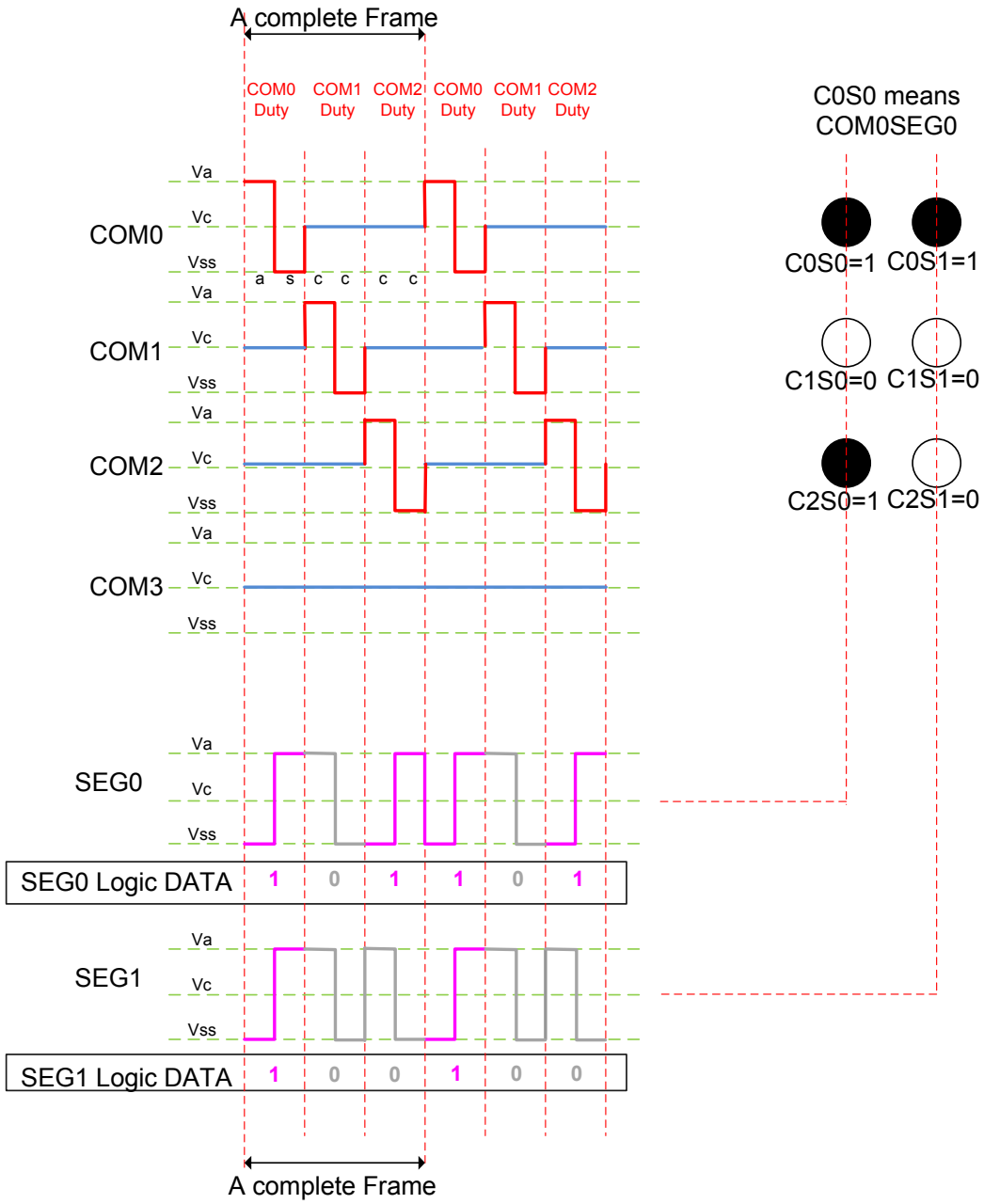
1/2 bias, 1/4 duty LCD waveform Type A



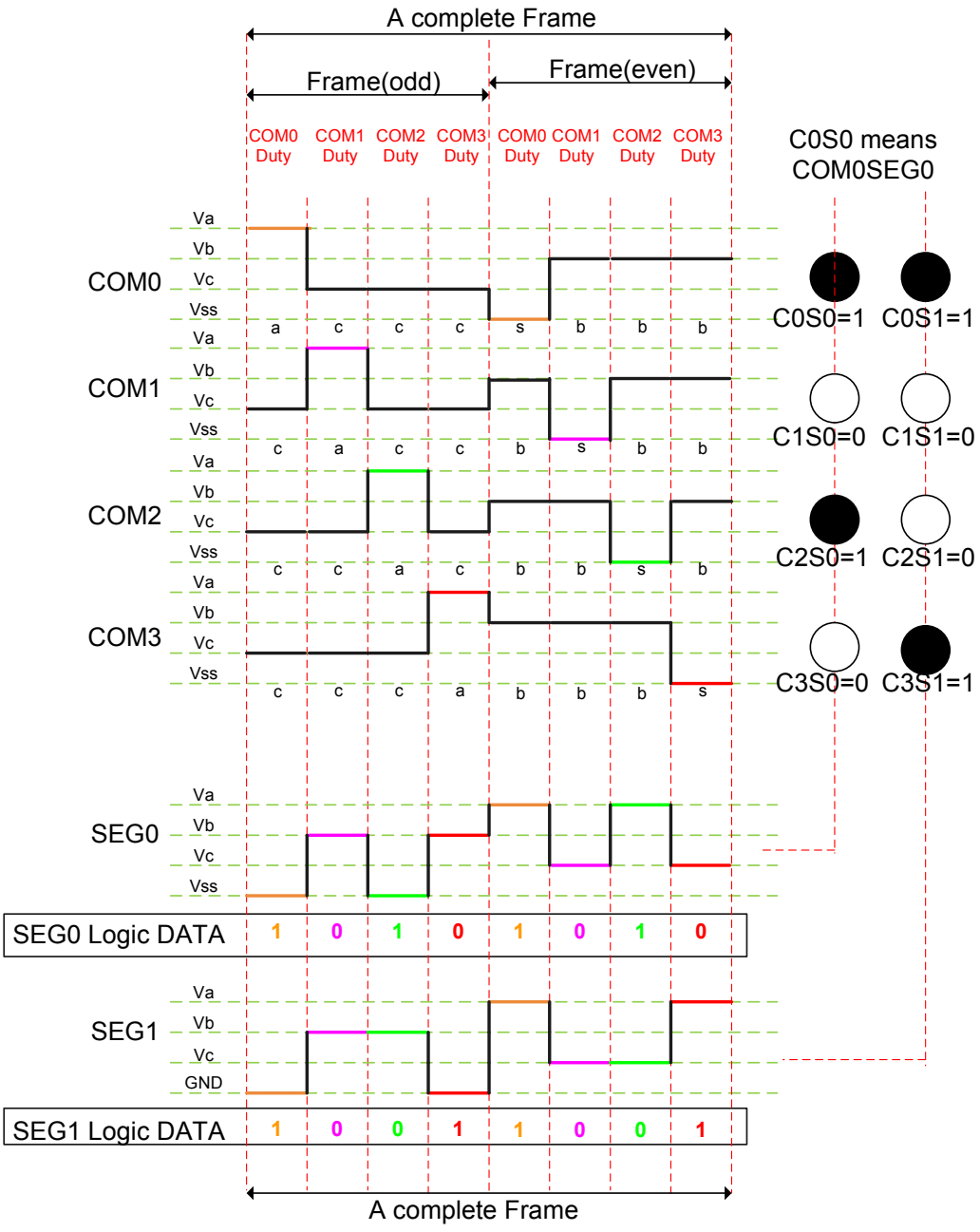
1/3 bias, 1/4 duty LCD waveform Type A



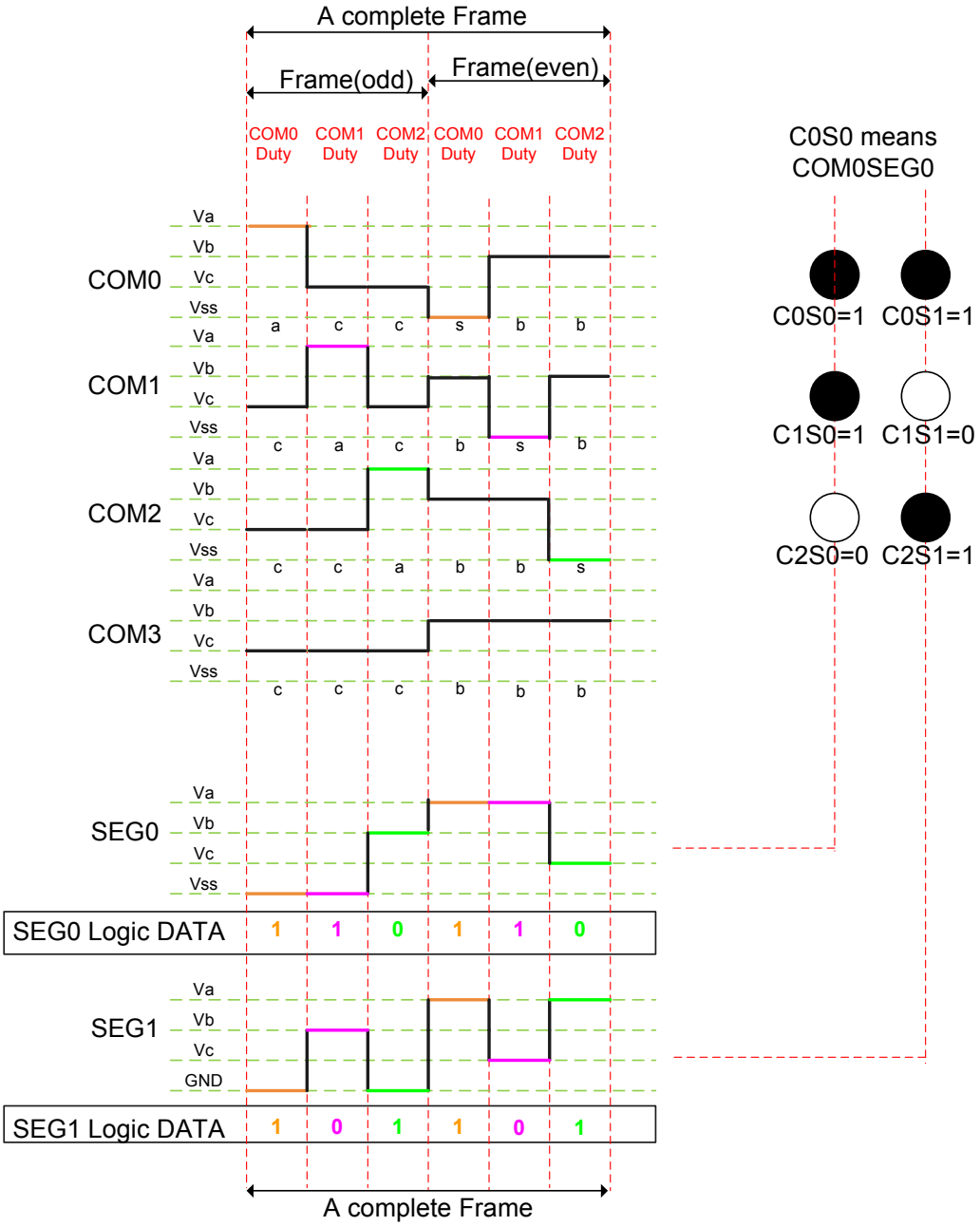
1/4 bias, 1/8 duty LCD waveform Type A



1/2 bias, 1/3 duty LCD waveform Type A



1/3 bias, 1/4 duty LCD waveform Type B



1/3 bias, 1/3 duty LCD waveform Type B

23.2 LCD Display Memory – RAM Structure

The display RAM is a static 36x4 bits RAM which stores the LCD data. A logic “1” state in the RAM bit cell indicates the “ON” state of the corresponding LCD segment. A logic “0” state indicates the “OFF” state.

Table:24-1 4COM/3COM/2COM/1COM

Mnemonic	Description	Indirect	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
		4x24 (4x36)	COM3	COM2	COM1	COM0	COM3	COM2	COM1	COM0	
		FFA0	SEG1	SEG1	SEG1	SEG1	SEG0	SEG0	SEG0	SEG0	
		FFA1	SEG3	SEG3	SEG3	SEG3	SEG2	SEG2	SEG2	SEG2	
		FFA2	SEG5	SEG5	SEG5	SEG5	SEG4	SEG4	SEG4	SEG4	
		FFA3	SEG7	SEG7	SEG7	SEG7	SEG6	SEG6	SEG6	SEG6	
		FFA4	SEG9	SEG9	SEG9	SEG9	SEG8	SEG8	SEG8	SEG8	
		FFA5	SEG11	SEG11	SEG11	SEG11	SEG10	SEG10	SEG10	SEG10	
		FFA6	SEG13	SEG13	SEG13	SEG13	SEG12	SEG12	SEG12	SEG12	
		FFA7	SEG15	SEG15	SEG15	SEG15	SEG14	SEG14	SEG14	SEG14	
		FFA8	SEG17	SEG17	SEG17	SEG17	SEG16	SEG16	SEG16	SEG16	
		FFA9	SEG19	SEG19	SEG19	SEG19	SEG18	SEG18	SEG18	SEG18	
		FFAA	SEG21	SEG21	SEG21	SEG21	SEG20	SEG20	SEG20	SEG20	
		FFAB	SEG23	SEG23	SEG23	SEG23	SEG22	SEG22	SEG22	SEG22	
		FFAC	SEG25	SEG25	SEG25	SEG25	SEG24	SEG24	SEG24	SEG24	
		FFAD	SEG27	SEG27	SEG27	SEG27	SEG26	SEG26	SEG26	SEG26	
		FFAE	SEG29	SEG29	SEG29	SEG29	SEG28	SEG28	SEG28	SEG28	
		FFAF	SEG31	SEG31	SEG31	SEG31	SEG30	SEG30	SEG30	SEG30	
		FFB0	SEG33	SEG33	SEG33	SEG33	SEG32	SEG32	SEG32	SEG32	
		FFB1	SEG35	SEG35	SEG35	SEG35	SEG34	SEG34	SEG34	SEG34	
		FFB2									
		FFB3									
		FFB4									
		FFB5									
		FFB6									
		FFB7									
		FFB8									
		FFB9									
		FFBA									
		FFBB									
		FFBC									
		FFBD									
		FFBE									
		FFBF									
		FFC0									
		FFC1									

Table:24-2 8COM

Mnemonic	Description	Indirect	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
		8x17 (8x32)	COM7	COM6	COM5	COM4	COM3	COM2	COM1	COM0	
		FFA0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	
		FFA1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	
		FFA2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	
		FFA3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	
		FFA4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	
		FFA5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	
		FFA6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	
		FFA7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	
		FFA8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	
		FFA9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	
		FFAA	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	
		FFAB	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	

		FFAC	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	
		FFAD	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	
		FFAE	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	
		FFAF	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	
		FFB0	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	
		FFB1	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	
		FFB2	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	
		FFB3	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	
		FFB4	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	
		FFB5	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	
		FFB6	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	
		FFB7	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	
		FFB8	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	
		FFB9	SEG25	SEG25	SEG25	SEG25	SEG25	SEG25	SEG25	SEG25	
		FFBA	SEG26	SEG26	SEG26	SEG26	SEG26	SEG26	SEG26	SEG26	
		FFBB	SEG27	SEG27	SEG27	SEG27	SEG27	SEG27	SEG27	SEG27	
		FFBC	SEG28	SEG28	SEG28	SEG28	SEG28	SEG28	SEG28	SEG28	
		FFBD	SEG29	SEG29	SEG29	SEG29	SEG29	SEG29	SEG29	SEG29	
		FFBE	SEG30	SEG30	SEG30	SEG30	SEG30	SEG30	SEG30	SEG30	
		FFBF	SEG31	SEG31	SEG31	SEG31	SEG31	SEG31	SEG31	SEG31	
		FFC0									
		FFC1									

Table:24-3 6COM

Mnemonic	Description	Indirect	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
		6x22 (6x34)			COM5	COM4	COM3	COM2	COM1	COM0	
		FFA0			SEG0	SEG0	SEG0	SEG0	SEG0	SEG0	
		FFA1			SEG1	SEG1	SEG1	SEG1	SEG1	SEG1	
		FFA2			SEG2	SEG2	SEG2	SEG2	SEG2	SEG2	
		FFA3			SEG3	SEG3	SEG3	SEG3	SEG3	SEG3	
		FFA4			SEG4	SEG4	SEG4	SEG4	SEG4	SEG4	
		FFA5			SEG5	SEG5	SEG5	SEG5	SEG5	SEG5	
		FFA6			SEG6	SEG6	SEG6	SEG6	SEG6	SEG6	
		FFA7			SEG7	SEG7	SEG7	SEG7	SEG7	SEG7	
		FFA8			SEG8	SEG8	SEG8	SEG8	SEG8	SEG8	
		FFA9			SEG9	SEG9	SEG9	SEG9	SEG9	SEG9	
		FFAA			SEG10	SEG10	SEG10	SEG10	SEG10	SEG10	
		FFAB			SEG11	SEG11	SEG11	SEG11	SEG11	SEG11	
		FFAC			SEG12	SEG12	SEG12	SEG12	SEG12	SEG12	
		FFAD			SEG13	SEG13	SEG13	SEG13	SEG13	SEG13	
		FFAE			SEG14	SEG14	SEG14	SEG14	SEG14	SEG14	
		FFAF			SEG15	SEG15	SEG15	SEG15	SEG15	SEG15	
		FFB0			SEG16	SEG16	SEG16	SEG16	SEG16	SEG16	
		FFB1			SEG17	SEG17	SEG17	SEG17	SEG17	SEG17	
		FFB2			SEG18	SEG18	SEG18	SEG18	SEG18	SEG18	
		FFB3			SEG19	SEG19	SEG19	SEG19	SEG19	SEG19	
		FFB4			SEG20	SEG20	SEG20	SEG20	SEG20	SEG20	
		FFB5			SEG21	SEG21	SEG21	SEG21	SEG21	SEG21	
		FFB6			SEG22	SEG22	SEG22	SEG22	SEG22	SEG22	
		FFB7			SEG23	SEG23	SEG23	SEG23	SEG23	SEG23	
		FFB8			SEG24	SEG24	SEG24	SEG24	SEG24	SEG24	
		FFB9			SEG25	SEG25	SEG25	SEG25	SEG25	SEG25	
		FFBA			SEG26	SEG26	SEG26	SEG26	SEG26	SEG26	
		FFBB			SEG27	SEG27	SEG27	SEG27	SEG27	SEG27	
		FFBC			SEG28	SEG28	SEG28	SEG28	SEG28	SEG28	
		FFBD			SEG29	SEG29	SEG29	SEG29	SEG29	SEG29	
		FFBE			SEG30	SEG30	SEG30	SEG30	SEG30	SEG30	
		FFBF			SEG31	SEG31	SEG31	SEG31	SEG31	SEG31	

		FFC0			SEG32	SEG32	SEG32	SEG32	SEG32	SEG32	
		FFC1			SEG33	SEG33	SEG33	SEG33	SEG33	SEG33	

23.3 LCD Register

Mnemonic	Description	Indirect	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
SYC	System Control Register	0xFF80							LBE	SYE	0x00
FRC	Frame-Rate Control Register	0xFF81	BK[1]	BK[0]	TYPE	DT[2]	DT[1]	DT[0]		IVA	0x08
LCDCLKDIV	LCD Clock Divide Register	0xFF82	CLKDIV[7]	CLKDIV[6]	CLKDIV[5]	CLKDIV[4]	CLKDIV[3]	CLKDIV[2]	CLKDIV[1]	CLKDIV[0]	0x3F
VLC	LCD Voltage Control Register	0xFF83	BSS[1]	BSS[0]	OPIB[1]	OPIB[0]	VRS[3]	VRS[2]	VRS[1]	VRS[0]	0x40
LCDC0	LCD/GPIO Configuration-0	0xFF84	SEGC[7:0]								0xFF
LCDC1	LCD/GPIO Configuration-1	0xFF85	SEGC[15:8]								0xFF
LCDC2	LCD/GPIO Configuration-2	0xFF86	SEGC[23:16]								0xFF
LCDC3	LCD/GPIO Configuration-3	0xFF87	SEGC31	SEGC30	SEGC29/COM4	SEGC28/COM5	SEGC27/COM6	SEGC26/COM7	SEGC25	SEGC24	0xC3
LCDC4	LCD/GPIO Configuration-4	0xFF88					SEGC[35:32]				0xFF
LCDTEST	LCD test register	0xFF89							LTEST[1:0]		0x00

SYC : System Control Register

Mnemonic: **Address:FF80H**

7	6	5	4	3	2	1	0	Reset
						LBE	SYE	00H

LBE : LCD Bias Enable. 0 is LCD bias “OFF”, 1 is ON.

SYE : Global control for LCD function and power control.

0 : Enable LCD ‘s power down mode.

1 : LBE bit get control of LCD bias and LCD function.

FRC : Frame-Rate Control Register

Mnemonic: **Address:FF81H**

7	6	5	4	3	2	1	0	Reset
BK[1]	BK[0]	TYPE	DT[2]	DT[1]	DT[0]	--	IVA	08H

BK[1:0] : Define the blinking frequency of LCD display.

00 : No blinking function.

01 : Blinking rate 2Hz

10 : Blinking rate 1Hz

11 : Blinking rate 0.5Hz

TYPE: LCD drive waveform type.

0 : Type A

1 : Type B

DT[2:0] : Define COM duty cycle (See note-1)

000 : 1/8 duty (COM0~7; RAM use: Table:1-2)

001 : 1/6 duty (COM0~5; RAM use: Table:1-3)

010 : 1/4 duty (COM0~3; RAM use: Table:1-1) (default)

011 : 1/3 duty (COM0~2; RAM use: Table:1-1)

100 : 1/2 duty (COM0~1; RAM use: Table:1-1)

101 : full duty (COM0 ; RAM use: Table:1-1)

Other: reserved

Note-1 :

(a) If DT[2:0] is configured as 2'b011 (1/3 duty), COM3 always signals out OFF waveform.
COM0 ~ COM2 is recursively active while in 1/3 duty mode.

(b) If DT[2:0] is configured as 2'b100 (1/2 duty), COM2 and COM3 always signal out OFF waveform.
COM0 ~ COM1 is recursively active while in 1/2 duty mode.

(c) If DT[2:0] is configured as 2'b101 (full duty), COM1 ~ COM3 always signal out OFF waveform
COM0 is always active while in full-duty mode.

IVA : Program VLCD is coming from V5V(external Pin) or from VCC(3V LDO output)

0 : LCD Seg/Com power come from V5V (and the full-scale voltage level is determined by VRS[3:0])

1 : LCD Seg/Com power come from VLDO3 (and the full-scale voltage level is determined by VRS[3:0])

LCDCLKDIV : LCD Clock Divide Register

Mnemonic: **Address:FF82H**

7	6	5	4	3	2	1	0	Reset
CLKDIV[7]	CLKDIV[6]	CLKDIV[5]	CLKDIV[4]	CLKDIV[3]	CLKDIV[2]	CLKDIV[1]	CLKDIV[0]	3FH

LCD FRQ: 32.768KHz;

LCD_CLK=32.768KHz/(2*(CLKDIV+1))

Ex: If CLKDIV[7:0]=0x3F DT[2:0]=2 (1/4 duty)

→ LCD_CLK = 32768/(2*(63+1)) = 256

→ 256/4 = 64, Frame Rate is 64Hz

Frame Rate

CLKDIV[7:0]	full duty	1/2 duty	1/3 duty	1/4 duty	1/6 duty	1/8 duty
0xFF	64 Hz	32 Hz	21.3 Hz	16 Hz	10.7 Hz	8 Hz
0x7F	128 Hz	64 Hz	42.7 Hz	32 Hz	21.3 Hz	16 Hz
0x54	192.8 Hz	96.4 Hz	64.3 Hz	48.2 Hz	32.1 Hz	24.1 Hz
0x3F	256 Hz	128 Hz	85.3 Hz	64 Hz	42.7 Hz	32 Hz
0x2A	381.3 Hz	190.5 Hz	127 Hz	95.3 Hz	63.5 Hz	47.6 Hz
0x1F	512 Hz	256 Hz	170.7 Hz	128 Hz	85.3 Hz	64 Hz

VLC : VLCD voltage control

Mnemonic: **Address:FF83H**

7	6	5	4	3	2	1	0	Reset
BSS[1]	BSS[0]	OPIB[1]	OPIB[0]	VRS[3]	VRS[2]	VRS[1]	VRS[0]	40H

BSS[1:0] : Define LCD bias voltage.

00 : 1/4 Bias

01 : 1/3 Bias (default)

10 : 1/2 Bias

OPIB[1:0] : Define LCD OP current bias.

00 : 1.3uA (default)

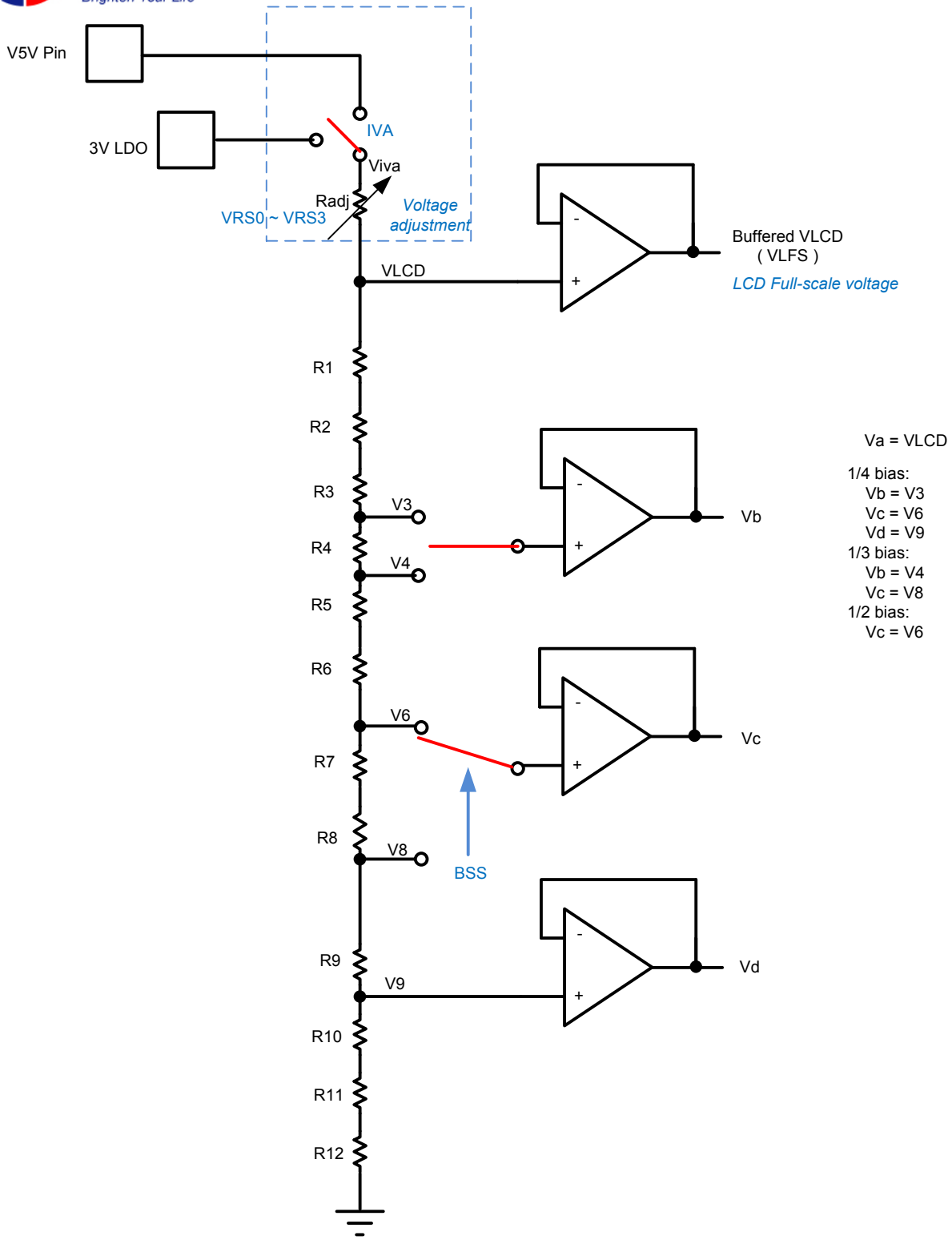
01 : 1.8uA

10 : 2.3uA

11 : 2.8uA

VRS[3:0] : Define full-scale voltage level

VRS[3:0]	VLCD voltage level	Note
0000	Viva	Default
0001	0.938 x Viva	
0010	0.882 x Viva	
0011	0.833 x Viva	
0100	0.789 x Viva	
0101	0.750 x Viva	
0110	0.714 x Viva	
0111	0.682 x Viva	
1000	0.652 x Viva	
1001	0.625 x Viva	
1010	0.600 x Viva	
1011	0.577 x Viva	
1100	0.556 x Viva	
1101	0.536 x Viva	
1110	0.517 x Viva	
1111	0.500 x Viva	



LCD Bias Voltage Generator and Adjustment

LCDC : LCD/GPIO Configuration

Mnemonic: LCDC0 **Address:FF84H**

7	6	5	4	3	2	1	0	Reset
SEGC7	SEGC6	SEGC5	SEGC4	SEGC3	SEGC2	SEGC1	SEGC0	FFH

Mnemonic: LCDC1 **Address:FF85H**

7	6	5	4	3	2	1	0	Reset
SEGC15	SEGC14	SEGC13	SEGC12	SEGC11	SEGC10	SEGC9	SEGC8	FFH

Mnemonic: LCDC2 **Address:FF86H**

7	6	5	4	3	2	1	0	Reset
SEGC23	SEGC22	SEGC21	SEGC20	SEGC19	SEGC18	SEGC17	SEGC16	FFH

Mnemonic: LCDC3 **Address:FF87H**

7	6	5	4	3	2	1	0	Reset
SEGC31	SEGC30	SEGC29 /COM4	SEGC28 /COM5	SEGC27 /COM6	SEGC26 /COM7	SEGC25	SEGC24	FFH

Mnemonic: LCDC4 **Address:FF88H**

7	6	5	4	3	2	1	0	Reset
				SEGC35	SEGC34	SEGC33	SEGC32	FFH

SEG[35:0]

0 : The corresponding SEG pin is LCD SEG/COM function.

1 : The corresponding SEG pin is MCU-expanded IO.

LCDC3[5:2] must be 0(SEG or COM choose by duty cycle)

SEGx=1 (default), is GPIO, and weakly pull-up.

Each SEG I/O pin is able to be configured as LCD driver or MCU-expanded IO through the SEG configuration bit.

If the configuration bit is 0, the pin has LCD function otherwise it is MCU-expanded IO.

If SYE=0 and SEGx=0, then the corresponding SEGx stays at VDD weakly pull-up state.

If SEGx=1, SYE will have no any effect on the corresponding SEG pin.

Remember to off the leakage path of input buffer on SEG pin while it is configured as LCD SEG driver.

24. Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VDD	Supply voltage	2.2	-	5.5	V	

DC Characteristics

TA = -40℃ to 85℃, V5V = 5.0V

Symbol	Parameter	Valid	Min	Typical	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0~6	-0.5	-	0.8	V	V5V=5V
VIL2	Input Low-voltage	RES, XTAL1	0	-	0.8	V	-
VIH1	Input High-voltage	Port 0~6	2.5	-	V5V + 0.5	V	-
VIH2	Input High-voltage	RES, XTAL1	70%V5V	-	V5V + 0.5	V	-
VOL	Output Low-voltage	Port 0~6	-	-	0.45	V	IOL=20mA V5V=5V
VOH1	Output High-voltage using Strong Pull-up(1)	Port 0~6	4.6	-	-	V	IOH= -7mA
VOH2	Output High-voltage using Weak Pull-up(2)	Port 0~6	2.6	-	-	V	IOH= -350uA
IIL	Logic 0 Input Current	Port 0~6	-	-	-75	uA	Vin= 0.45V
ITL	Logical Transition Current	Port 0~6	-	-	-650	uA	Vin= 2.0V
ILI	Input Leakage Current	Port 0~6	-	-	±10	uA	0.45V<Vin<V5V
RRST	Reset Pull-up Resistor	RES	50	-	300	kΩ	-
CIO	Pin Capacitance	-	-	-	10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	V5V	-	3.19	4.78	mA	Active mode ,IRC=22.1184MHz
			-	5.5	8.25	mA	Active mode, 12MHz V5V=5V 25 ℃
			-	4.5	7.25	mA	Idle mode, 12MHz V5V =5V 25 ℃
			-	3	7	uA	Power down mode V5V =5V 25 ℃

Notes:
(1) Port in Push-Pull Output Mode
(2) Port in Quasi-Bidirectional Mode
(3) Maximum IOL per port0~6 pin : 20mA

TA = -40℃ to 85℃, V5V = 3.0V

Symbol	Parameter	Valid	Min	Typical	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0~6	-0.5	-	0.8	V	V5V=3.0V
VIL2	Input Low-voltage	RES, XTAL1	0	-	0.8	V	-
VIH1	Input High-voltage	Port 0~6	2.0	-	V5V + 0.5	V	-
VIH2	Input High-voltage	RES, XTAL1	70%V5V	-	V5V + 0.5	V	-
VOL	Output Low-voltage	Port 0~6	-	-	0.45	V	IOL=12mA V5V=3V
VOH1	Output High-voltage using Strong Pull-up(1)	Port 0~6	2.6	-	-	V	IOH= -5mA
VOH2	Output High-voltage using Weak Pull-up(2)	Port 0~6	2.4	-	-	V	IOH= -70uA
IIL	Logic 0 Input Current	Port 0~6	-	-	-75	uA	Vin= 0.45V
ITL	Logical Transitio n Current	Port 0~6	-	-	-650	uA	Vin=1.5V
ILI	Input Leakage Current	Port 0~6	-	-	±10	uA	0.45V<Vin<V5V
RRST	Reset Pull-up Resistor	RES	50	-	300	kΩ	-
CIO	Pin Capacitance		-	-	10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	V5V	-	3.15	4.73	mA	Active mode ,IRC=11.0592MHz
			-	2.77	4.16	mA	Active mode ,12MHz V5V = 3.0 V 25 ℃
			-	1.77	3.16	mA	Idle mode, 12MHz V5V =3.0V 25 ℃
			-	2	5	uA	Power down mode V5V =3.0V 25 ℃

Notes:
(4) Port in Push-Pull Output Mode
(5) Port in Quasi-Bidirectional Mode
(6) Maximum IOL per port0~6 pin : 12mA

Absolute Maximum Ratings

SYMBOL	PARAMETER	MAX	UNIT
Maximum sourced current	An I/O pin	N/A	mA
	Total I/O pins	150	mA
Maximum sink current	An I/O pin	N/A	mA
	Total I/O pins	150	mA
Tj	Max. Junction Temperature	150	℃

Comparator Characteristics

Ta=25℃

Symbol	Description	Test Condition		MIN	TPY	MAX	Unit
		V5V	Condition				
I_{OP}	Operating current	5	-	-	-	10	uA
-	Power Down Current	5	-	-	-	0.1	uA
-	Offset voltage	5	-	-10	-	+10	mV
V_{CM}	Input voltage commom mode range	-	-	Vss	-	V5V-1.5	V
Tp	Propagation delay	5	△ Vin=10mV	-	3	6	us

LVI& LVR Characteristics

V5V	LVR		
	Min	Typical	Max
2.2V ~ 5.5V	VIL=1.42V (VIH=1.62V)	VIL=1.50V (VIH=1.70V)	VIL=1.57V (VIH=1.77V)

V5V	LVI		
	Min	Typical	Max
LVIS[1:0] = 00	VIL=1.57V (VIH=1.77V)	VIL=1.65V (VIH=1.85V)	VIL=1.73V (VIH=1.93V)
LVIS[1:0] = 01	VIL=2.47V (VIH=2.67V)	VIL=2.60V (VIH=2.80V)	VIL=2.73V (VIH=2.93V)
LVIS[1:0] = 10	VIL=3.04V (VIH=3.24V)	VIL=3.20V (VIH=3.40V)	VIL=3.36V (VIH=3.56V)
LVIS[1:0] = 11	VIL=3.80V (VIH=4.00V)	VIL=4.00V (VIH=4.20V)	VIL=4.20V (VIH=4.40V)