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Product List

SM39R16A6U24,
SM39R16A6U28,
SM39R16A6U32,

Description

The SM39R16A6 is a 1T (one machine cycle per clock) single-chip 8-bit microcontroller. It has 16K-byte embedded Flash for program, and executes all ASM51 instructions fully compatible with MCS-51

SM39R16A6 contains 1K+256B on-chip RAM, up to 30 GPIOs (32L package), various serial interfaces and many peripheral functions as described below. It can be programmed via writers. Its on-chip ICE is convenient for users in verification during development stage.

The high performance of SM39R16A6 can achieve complicated manipulation within short time. About one third of the instructions are pure 1T, and the average speed is 8 times of traditional 8051, the fastest one among all the 1T 51-series.Its excellent EMI and ESD characteristics are advantageous for many different applications.

Ordering Information

SM39R16A6ihhkL
YWW
i: process identifier { U = 1.8V ~ 5.5V}
hh: pin count
k: package type postfix {as table below }
L:PB Free identifier
{No text is Non-PB free，”P” is PB free}
Y: year
WW: week

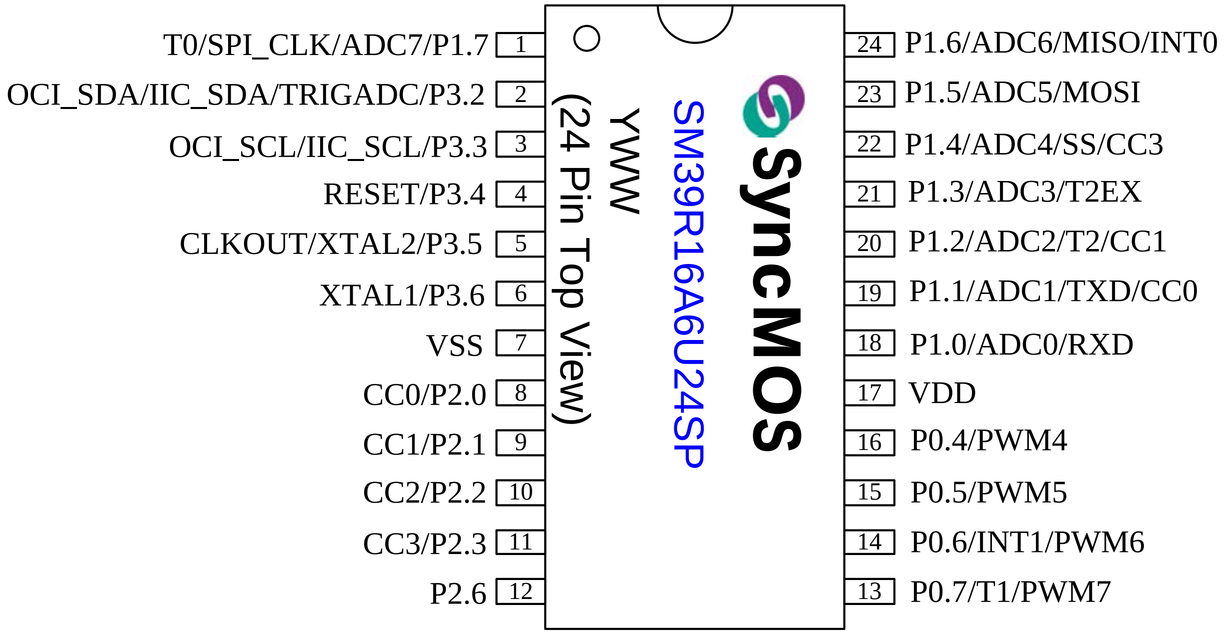
Postfix	Package
S	SOP (300 mil)
V	LQFP

Features

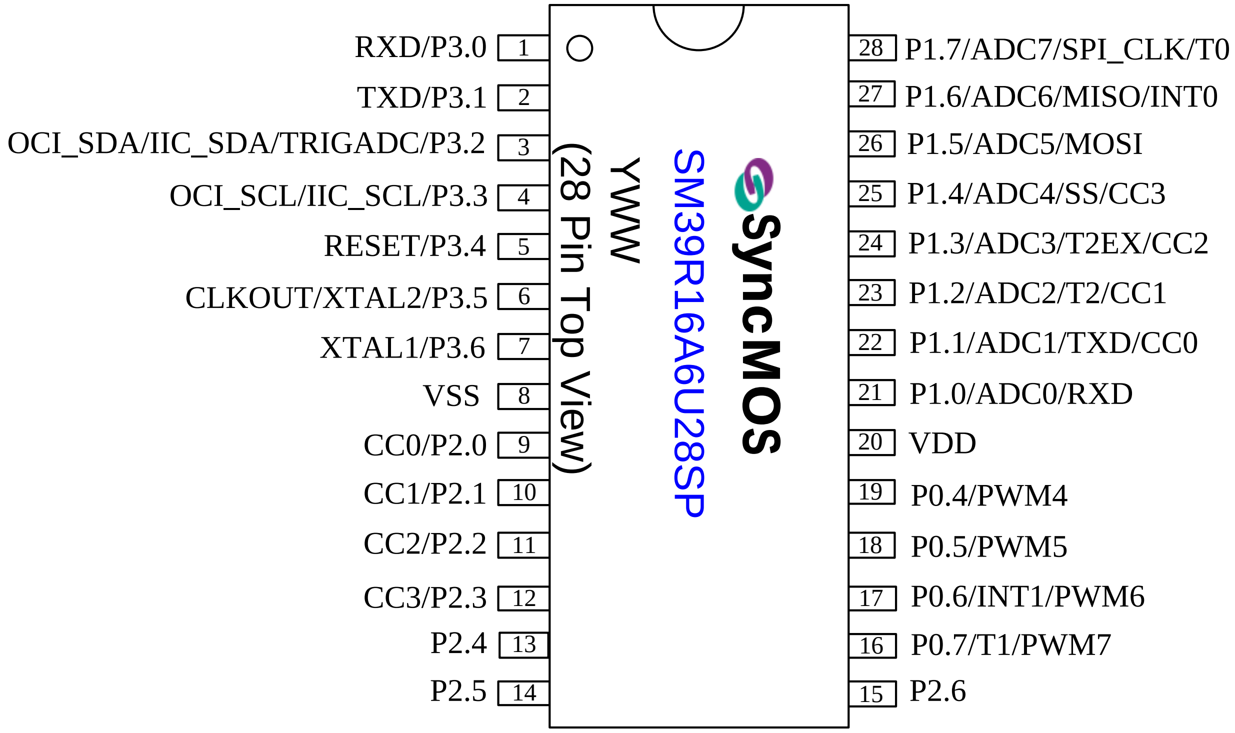
- Main Flash ROM 16KB , 128B/page
- Working voltage 1.8V~5.5V
- High speed architecture of 1 clock/machine cycle runs up to 25MHz.
- 256 bytes SRAM as standard 8052, plus 1K bytes on-chip expandable SRAM.
- Dual 16-bit Data Pointers (DPTR0 & DPTR1).
- One serial peripheral interfaces in full duplex mode (UART).
  - Synchronous mode, fixed baud rate.
  - 8-bit UART mode, variable baud rate.
  - 9-bit UART mode, fixed baud rate.
  - 9-bit UART mode, variable baud rate.
- Additional Baud Rate Generator for Serial port.
- Three 16-bit Timer/Counters. (Timer 0, 1, 2).
- Programmable watchdog timer.
- One IIC interface. (Master/Slave mode).
- One SPI interface. (Master/Slave mode)
- 4-channel 14-bit PWM for motor control
- 4-channel 16-bit compare / capture / load functions.
  - Comparator out can be CCU input source internally.
  - Noise filter with CCU input with sample frequency select.
- ISP/IAP/ICP functions.
- EEPROM function.
- On-Chip in-circuit emulator (ICE) functions with On-Chip Debugger (OCD).
- Fast multiplication-division unit (MDU): 16*16, 32/16, 16/16, 32-bit L/R shifting and 32-bit normalization.
- LVI/LVR (LVR deglitch 500ns).
- Enhance user code protection.
- Power management unit for IDLE and power down modes.

Pin Configuration

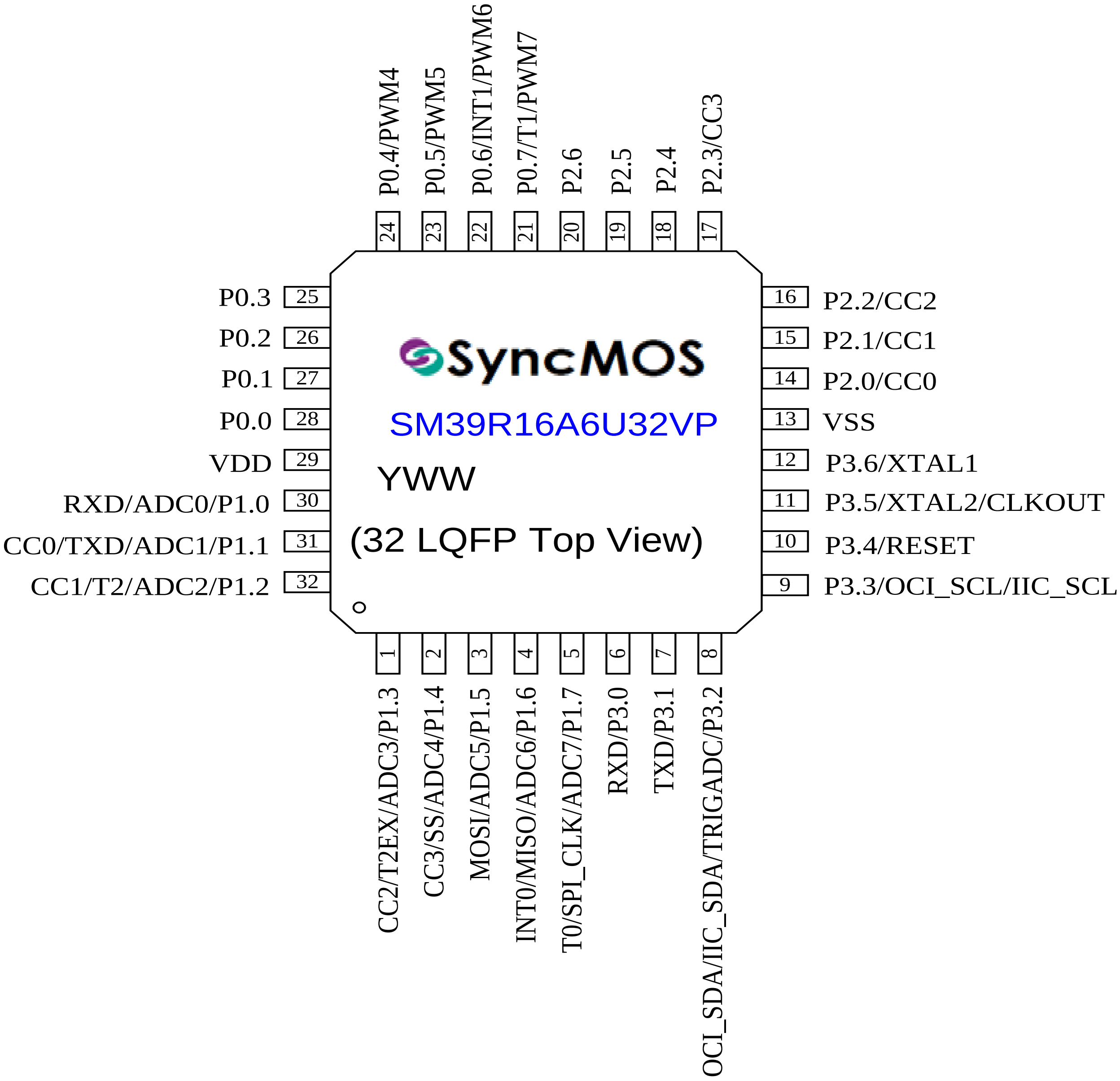
24 Pin SOP


T0/SPI_CLK/ADC7/P1.7 1
OCI_SDA/IIC_SDA/TRIGADC/P3.2 2
OCI_SCL/IIC_SCL/P3.3 3
RESET/P3.4 4
CLKOUT/XTAL2/P3.5 5
XTAL1/P3.6 6
VSS 7
CC0/P2.0 8
CC1/P2.1 9
CC2/P2.2 10
CC3/P2.3 11
P2.6 12
13 P0.7/T1/PWM7
14 P0.6/INT1/PWM6
15 P0.5/PWM5
16 P0.4/PWM4
17 VDD
18 P1.0/ADC0/RXD
19 P1.1/ADC1/TXD/CC0
20 P1.2/ADC2/T2/CC1
21 P1.3/ADC3/T2EX
22 P1.4/ADC4/SS/CC3
23 P1.5/ADC5/MOSI
24 P1.6/ADC6/MISO/INT0
SyncMOS
SM39R16A6U24SP
YWW
(24 Pin Top View)

28 Pin SOP


RXD/P3.0 1
TXD/P3.1 2
OCI_SDA/IIC_SDA/TRIGADC/P3.2 3
OCI_SCL/IIC_SCL/P3.3 4
RESET/P3.4 5
CLKOUT/XTAL2/P3.5 6
XTAL1/P3.6 7
VSS 8
CC0/P2.0 9
CC1/P2.1 10
CC2/P2.2 11
CC3/P2.3 12
P2.4 13
P2.5 14
15 P2.6
16 P0.7/T1/PWM7
17 P0.6/INT1/PWM6
18 P0.5/PWM5
19 P0.4/PWM4
20 VDD
21 P1.0/ADC0/RXD
22 P1.1/ADC1/TXD/CC0
23 P1.2/ADC2/T2/CC1
24 P1.3/ADC3/T2EX/CC2
25 P1.4/ADC4/SS/CC3
26 P1.5/ADC5/MOSI
27 P1.6/ADC6/MISO/INT0
28 P1.7/ADC7/SPI_CLK/T0
SyncMOS
SM39R16A6U28SP
YWW
(28 Pin Top View)

32 Pin LQFP


P0.4/PWM4 24
P0.5/PWM5 23
P0.6/INT1/PWM6 22
P0.7/T1/PWM7 21
P2.6 20
P2.5 19
P2.4 18
P2.3/CC3 17
P0.3 25
P0.2 26
P0.1 27
P0.0 28
VDD 29
RXD/ADC0/P1.0 30
CC0/TXD/ADC1/P1.1 31
CC1/T2/ADC2/P1.2 32
16 P2.2/CC2
15 P2.1/CC1
14 P2.0/CC0
13 VSS
12 P3.6/XTAL1
11 P3.5/XTAL2/CLKOUT
10 P3.4/RESET
9 P3.3/OCI_SCL/IIC_SCL
SyncMOS
SM39R16A6U32VP
YWW
(32 LQFP Top View)
1 CC2/T2EX/ADC3/P1.3
2 CC3/SS/ADC4/P1.4
3 MOSI/ADC5/P1.5
4 INT0/MISO/ADC6/P1.6
5 T0/SPI_CLK/ADC7/P1.7
6 RXD/P3.0
7 TXD/P3.1
8 OCI_SDA/IIC_SDA/TRIGADC/P3.2

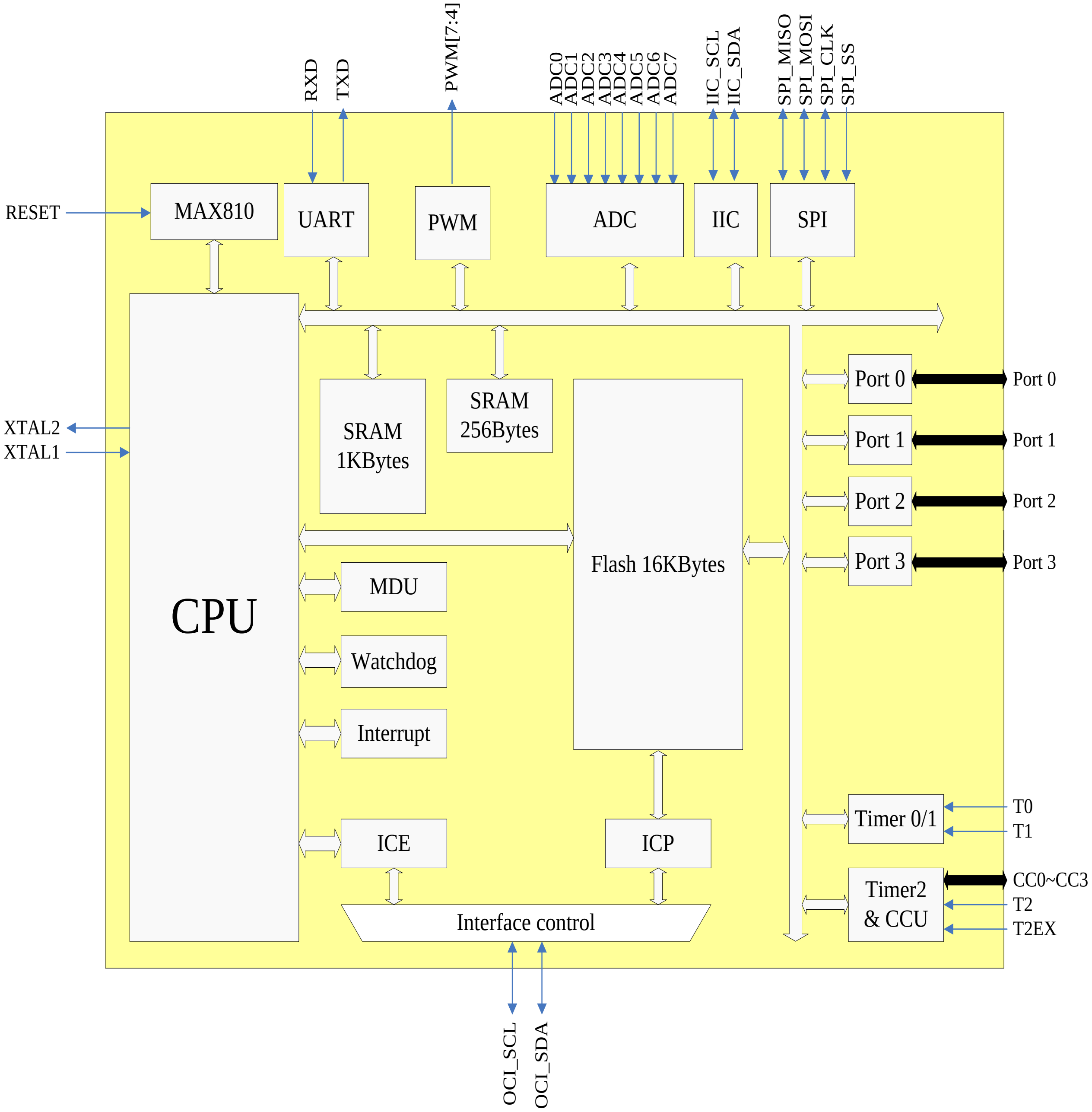
Notes：

(1) The pin Reset/P3.4 factory default is GPIO (P3.4). User can configure it to reset by a flash programmer.

(2) To avoid accidentally entering ISP-Mode(refer to section 18.4), care must be taken not asserting pulse signal at RXD P3.0 during power-up while P1.2, P1.3 or P1.4 are set to high.

(3) To apply ICP function, OCI_SDA/P3.2 and OCI_SCL/P3.3 are ICP pins during reset period. When reset finish, they are GPIO.

Block Diagram


RXD
TXD
PWM[7:4]
ADC0
ADC1
ADC2
ADC3
ADC4
ADC5
ADC6
ADC7
IIC_SCL
IIC_SDA
SPI_MISO
SPI_MOSI
SPI_CLK
SPI_SS
RESET
MAX810
UART
PWM
ADC
IIC
SPI
XTAL2
XTAL1
CPU
SRAM 1KBytes
SRAM 256Bytes
Flash 16KBytes
MDU
Watchdog
Interrupt
ICE
ICP
Interface control
Port 0
Port 1
Port 2
Port 3
Port 0
Port 1
Port 2
Port 3
Timer 0/1
T0
T1
Timer2 & CCU
CC0~CC3
T2
T2EX
OCI_SCL
OCI_SDA

Pin Description

32L LQFP	28L SOP	24L SOP	Symbol	I/O	Description
1	24	21	P1.3/ADC3/T2EX/CC2	I/O	Bit 3 of port 1 & ADC input channel 3 & Timer 2 capture trigger & Timer 2 compare/capture Channel 2
2	25	22	P1.4/ADC4/SS/CC3	I/O	Bit 4 of port 1 & ADC input channel 4 & SPI interface Slave Select pin & Timer 2 compare/capture Channel 3
3	26	23	P1.5/ADC5/MOSI	I/O	Bit 5 of port 1 & ADC input channel 5 & SPI interface Serial Data Master Output or Slave Input pin
4	27	24	P1.6/ADC6/MISO/INT0	I/O	Bit 6 of port 1 & ADC input channel 6 & SPI interface Serial Data Master Input or Slave Output pin & External interrupt 0
5	28	1	P1.7/ADC7/SPI_CLK/T0	I/O	Bit 7 of port 1 & ADC input channel 7 & SPI interface Clock pin & Timer 0 external input
6	1		P3.0/RXD	I/O	Bit 0 of port 3 & Serial interface channel Receive data
7	2		P3.1/TXD	I/O	Bit 1 of port 3 & Serial interface channel Transmit data or receive clock in mode 0
8	3	2	P3.2/TRIGADC/IIC_SDA/OCI_SDA	I/O	Bit 2 of port 3 & external pin to trigger ADC & IIC SDA pin & On-Chip Instrumentation SDA
9	4	3	P3.3/IIC_SCL/OCI_SCL	I/O	Bit 3 of port 3 & IIC SCL pin & On-Chip Instrumentation SCL
10	5	4	P3.4/RESET	I/O	Bit 4 of port 3 & Reset pin
11	6	5	P3.5/XTAL2/CLKOUT	I/O	Bit 5 of port 3 & Crystal output & clock out
12	7	6	P3.6/XTAL1	I/O	Bit 6 of port 3 & Crystal input
13	8	7	VSS		Ground
14	9	8	P2.0/CC0	I/O	Bit 0 of port 2 & Timer 2 compare/capture Channel 0
15	10	9	P2.1/CC1	I/O	Bit 1 of port 2 & Timer 2 compare/capture Channel 1
16	11	10	P2.2/CC2	I/O	Bit 2 of port 2 & Timer 2 compare/capture Channel 2
17	12	11	P2.3/CC3	I/O	Bit 3 of port 2 & Timer 2 compare/capture Channel 3
18	13		P2.4	I/O	Bit 4 of port 2
19	14		P2.5	I/O	Bit 5 of port 2
20	15	12	P2.6	I/O	Bit 6 of port 2
21	16	13	P0.7/PWM7/T1	I/O	Bit 7 of port 0 & PWM Channel 7 & Timer 1 external input
22	17	14	P0.6/PWM6/INT1	I/O	Bit 6 of port 0 & PWM Channel 6 & External interrupt 1
23	18	15	P0.5/PWM5	I/O	Bit 5 of port 0 & PWM Channel 5
24	19	16	P0.4/PWM4	I/O	Bit 4 of port 0 & PWM Channel 4
25			P0.3	I/O	Bit 3 of port 0
26			P0.2	I/O	Bit 2 of port 0
27			P0.1	I/O	Bit 1 of port 0
28			P0.0	I/O	Bit 0 of port 0
29	20	17	VDD	I	Power supply
30	21	18	P1.0/ADC0/RXD	I/O	Bit 0 of port 1 & ADC input channel 0 & Serial interface channel receive data
31	22	19	P1.1/ADC1/TXD/CC0	I/O	Bit 1 of port 1 & ADC input channel 1 & Serial interface channel Transmit data & Timer 2 compare/capture Channel 0
32	23	20	P1.2/ADC2/T2/CC1	I/O	Bit 2 of port 1 & ADC input channel 2 & Timer 2 external input clock & Timer 2 compare/capture Channel 1

Special Function Register (SFR)

A map of the Special Function Registers is shown as below:

In-direct access Mode

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8	IICS	IICCTL	IICA1	IICA2	IICRWD	IICEBT			**FF**
F0	B	SPIC1	SPIC2	SPITXD	SPIRXD	SPIS		TAKEY	**F7**
E8		MD0	MD1	MD2	MD3	MD4	MD5	ARCON	**EF**
E0	ACC	ISPFAH	ISPFAL	ISPFD	ISPFC		LVC	SWRES	**E7**
D8		PFCON	P3M0	P3M1					**DF**
D0	PSW	CCEN2	P0M0	P0M1	P1M0	P1M1	P2M0	P2M1	**D7**
C8	T2CON	CCCON	CRCL	CRCH	TL2	TH2			**CF**
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3	**C7**
B8	IEN1	IP1	SRELH				PAGESEL		**BF**
B0	P3						WDTC	WDTK	**B7**
A8	IEN0	IP0	SRELL	ADCC1	ADCC2	ADCDH	ADCDL	ADCCS	**AF**
A0	P2	RSTS	PWM ADDR	PWM DATA					**A7**
98	SCON	SBUF	IEN2						**9F**
90	P1	AUX						IRCON2	**97**
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	IFCON	**8F**
80	P0	SP	DPL	DPH	DPL1	DPH1	RCON	PCON	**87**
Hex\Bin	**X000**	**X001**	**X010**	**X011**	**X100**	**X101**	**X110**	**X111**	**Bin/Hex**

Page Mode: page0

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8	IICS	IICCTL	IICA1	IICA2	IICRWD	IICEBT			**FF**
F0	B	SPIC1	SPIC2	SPITXD	SPIRXD	SPIS		TAKEY	**F7**
E8		MD0	MD1	MD2	MD3	MD4	MD5	ARCON	**EF**
E0	ACC	ISPFAH	ISPFAL	ISPFD	ISPFC		LVC	SWRES	**E7**
D8		PFCON	P3M0	P3M1					**DF**
D0	PSW	CCEN2	P0M0	P0M1	P1M0	P1M1	P2M0	P2M1	**D7**
C8	T2CON	CCCON	CRCL	CRCH	TL2	TH2	OpPin2	Cmp2CON	**CF**
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3	**C7**
B8	IEN1	IP1	SRELH				PAGESEL		**BF**
B0	P3						WDTC	WDTK	**B7**
A8	IEN0	IP0	SRELL	ADCC1	ADCC2	ADCDH	ADCDL	ADCCS	**AF**
A0	P2	RSTS							**A7**
98	SCON	SBUF	IEN2						**9F**
90	P1	AUX						IRCON2	**97**
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	IFCON	**8F**
80	P0	SP	DPL	DPH	DPL1	DPH1	RCON	PCON	**87**
Hex\Bin	**X000**	**X001**	**X010**	**X011**	**X100**	**X101**	**X110**	**X111**	**Bin/Hex**

Page Mode: page1

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8		PWMTBC0	PWMTBC1	PWMOPMOD					**FF**
F0	B	PERIODL	PERIODH			PWMEN		TAKEY	**F7**
E8							PWMTBPOSTSCALE		**EF**
E0	ACC	ISPFAH	ISPFAL	ISPFD	ISPFC		LVC	SWRES	**E7**
D8		PFCON				PWMPOLARITY			**DF**
D0	PSW					DUTY2L	DUTY2H	DUTY3L	**D7**
C8	T2CON	DUTY3H			TL2	TH2			**CF**
C0	IRCON								**C7**
B8	IEN1	IP1	SRELH		PWMINTF		PAGESEL		**BF**
B0	P3						WDTC	WDTK	**B7**
A8	IEN0	IP0	SRELL	ADCC1	ADCC2	ADCDH	ADCDL	ADCCS	**AF**
A0	P2								**A7**
98	SCON	SBUF	IEN2						**9F**
90	P1	AUX						IRCON2	**97**
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	IFCON	**8F**
80	P0	SP	DPL	DPH	DPL1	DPH1	RCON	PCON	**87**
Hex\Bin	**X000**	**X001**	**X010**	**X011**	**X100**	**X101**	**X110**	**X111**	**Bin/Hex**

Note: Special Function Registers reset values and description for SM39R16A6.

Register	**Location: 80h ~ 8Fh**			**Reset value**	**Description**
	Method 1	**Method 2 Page 0**	**Method 2 Page 1**		
SYSTEM					
SP	81h	81h	81h	07h	Stack Pointer
ACC	E0h	E0h	E0h	00h	Accumulator
PSW	D0h	D0h	D0h	00h	Program Status Word
B	F0h	F0h	F0h	00h	B Register
DPL	82h	82h	82h	00h	Data Pointer 0 low byte
DPH	83h	83h	83h	00h	Data Pointer 0 high byte
DPL1	84h	84h	84h	00h	Data Pointer 1 low byte
DPH1	85h	85h	85h	00h	Data Pointer 1 high byte
AUX	91h	91h	91h	00h	Auxiliary register
PCON	87h	87h	87h	40h	Power Control
CKCON	8Eh	8Eh	8Eh	10h	Clock control register
PAGESEL	BEh	BEh	BEh	00h	Page select
INTERRUPT & PRIORITY					
IRCON	C0h	C0h	C0h	00h	Interrupt Request Control Register
IRCON2	97h	97h	97h	00h	Interrupt Request Control Register 2
IEN0	A8h	A8h	A8h	00h	Interrupt Enable Register 0
IEN1	B8h	B8h	B8h	00h	Interrupt Enable Register 1
IEN2	9Ah	9Ah	9Ah	00h	Interrupt Enable Register 2
IP0	A9h	A9h	A9h	00h	Interrupt Priority Register 0
IP1	B9h	B9h	B9h	00h	Interrupt Priority Register 1
UART					
PCON	87h	87h	87h	40h	Power Control
AUX	91h	91h	91h	00h	Auxiliary register
SCON	98h	98h	98h	00h	Serial Port, Control Register
SBUF	99h	99h	99h	00h	Serial Port, Data Buffer
SRELL	AAh	AAh	AAh	00h	Serial Port, Reload Register, low byte
SRELH	BAh	BAh	BAh	00h	Serial Port, Reload Register, high byte
PFCON	D9h	D9h	D9h	00h	Peripheral Frequency control register
ADC					
ADCC1	ABh	ABh	ABh	00h	ADC Control 1 Register
ADCC2	ACh	ACh	ACh	08h	ADC Control 2 Register
ADCDH	ADh	ADh	ADh	00h	ADC data high byte
ADCDL	AEh	AEh	AEh	00h	ADC data low byte
ADCCS	AFh	AFh	AFh	00h	ADC clock select
WDT					
RSTS	A1h	A1h		00h	Reset status register
WDTC	B6h	B6h	B6h	04h	Watchdog timer control register

Register	**Location: 80h ~ 8Fh**			**Reset value**	**Description**
	Method 1	**Method 2 Page 0**	**Method 2 Page 1**		
WDTK	B7h	B7h	B7h	00h	Watchdog timer refresh key.
TAKEY	F7h	F7h	F7h	00h	Time Access Key register
PWM					
PWMTBC0			F9h	00h	PWM Time Base Control 0 Reg.
PWMTBC1			FAh	10h	PWM Time Base Control 1 Reg.
PWMOPMOD			FBh	00h	PWM Output Pair Mode Reg.
PERIODL			F1h	FFh	PWM Period (Low) Reg.
PERIODH			F2h	3Fh	PWM Period (High) Reg.
PWMEN			F5h	00h	PWM Output Enable Reg.
PWMTBPOST SCALE			EEh	00h	PWM Time Base Post Scale Reg.
PWMINTF			BCh	00h	PWM INT Flag Reg.
PWMPOLARITY			DDh	FFh	PWM Polarity Reg.
DUTY2L			D5h	00h	PWM 2 Duty Low byte Reg.
DUTY2H			D6h	00h	PWM 2 Duty High byte Reg.
DUTY3L			D7h	00h	PWM 3 Duty Low byte Reg.
DUTY3H			C9h	00h	PWM 3 Duty High byte Reg.
PWMADDR	A2h			00h	PWM Address Register
PWMDATA	A3h			00h	PWM Data Register
TIMER0/TIMER1					
TCON	88h	88h	88h	00h	Timer/Counter Control
TMOD	89h	89h	89h	00h	Timer Mode Control
TL0	8Ah	8Ah	8Ah	00h	Timer 0, low byte
TL1	8Bh	8Bh	8Bh	00h	Timer 1, low byte
TH0	8Ch	8Ch	8Ch	00h	Timer 0, high byte
TH1	8Dh	8Dh	8Dh	00h	Timer 1, high byte
PFCON	D9h	D9h	D9h	00h	Peripheral Frequency control register
PCA(TIMER2)					
CCEN	C1h	C1h		00h	Compare/Capture Enable Register
CCL1	C2h	C2h		00h	Compare/Capture Register 1, low byte
CCH1	C3h	C3h		00h	Compare/Capture Register 1, high byte
CCL2	C4h	C4h		00h	Compare/Capture Register 2, low byte
CCH2	C5h	C5h		00h	Compare/Capture Register 2, high byte
CCL3	C6h	C6h		00h	Compare/Capture Register 3, low byte
CCH3	C7h	C7h		00h	Compare/Capture Register 3, high byte
T2CON	C8h	C8h	C8h	00h	Timer 2 Control
CCCON	C9h	C9h		00h	Compare/Capture Control
CRCL	CAh	CAh		00h	Compare/Reload/Capture Register, low byte

Register	**Location: 80h ~ 8Fh**			**Reset value**	**Description**
	Method 1	**Method 2 Page 0**	**Method 2 Page 1**		
CRCH	CBh	CBh		00h	Compare/Reload/Capture Register, high byte
TL2	CCh	CCh	CCh	00h	Timer 2, low byte
TH2	CDh	CDh	CDh	00h	Timer 2, high byte
CCEN2	D1h	D1h		00h	Compare/Capture Enable 2 register
GPIO					
P0	80h	80h	80h	User define	Port 0
P1	90h	90h	90h	FFh	Port 1
P2	A0h	A0h	A0h	7Fh	Port 2
P3	B0h	B0h	B0h	7Fh	Port 3
P0M0	D2h	D2h		User define	Port 0 output mode 0
P0M1	D3h	D3h		00h	Port 0 output mode 1
P1M0	D4h	D4h		00h	Port 1 output mode 0
P1M1	D5h	D5h		00h	Port 1 output mode 1
P2M0	D6h	D6h		00h	Port 2 output mode 0
P2M1	D7h	D7h		00h	Port 2 output mode 1
P3M0	DAh	DAh		00h	Port 3 output mode 0
P3M1	DBh	DBh		00h	Port 3 output mode 1
ISP/IAP/EEPROM					
IFCON	8Fh	8Fh	8Fh	00h	Interface control register
ISPFAH	E1h	E1h	E1h	FFh	ISP Flash Address-High register
ISPFAL	E2h	E2h	E2h	FFh	ISP Flash Address-Low register
ISPFD	E3h	E3h	E3h	FFh	ISP Flash Data register
ISPFC	E4h	E4h	E4h	00h	ISP Flash control register
TAKEY	F7h	F7h	F7h	00h	Time Access Key register
LVI/LVR/SOFTRESET					
RSTS	A1h	A1h		00h	Reset status register
LVC	E6h	E6h	E6h	20h	Low voltage control register
SWRES	E7h	E7h	E7h	00h	Software Reset register
TAKEY	F7h	F7h	F7h	00h	Time Access Key register
SPI					
SPIC1	F1h	F1h		08h	SPI control register 1
SPIC2	F2h	F2h		00h	SPI control register 2
SPITXD	F3h	F3h		00h	SPI Transmit data buffer
SPIRXD	F4h	F4h		00h	SPI receive data buffer
SPIS	F5h	F5h		40h	SPI status register
IIC					
IICS	F8h	F8h		00h	IIC status register
IICCTL	F9h	F9h		04h	IIC control register

Register	**Location: 80h ~ 8Fh**			**Reset value**	**Description**
	Method 1	**Method 2 Page 0**	**Method 2 Page 1**		
IICA1	FAh	FAh		A0h	IIC channel 1 Address 1 register
IICA2	FBh	FBh		60h	IIC channel 1 Address 2 register
IICRWD	FCh	FCh		00h	IIC channel 1 Read / Write Data buffer
IICEBT	FDh	FDh		00h	IIC Enable Bus Transaction register

Function Description

1. General Features

SM39R16A6 is an 8-bit micro-controller. All of its functions and the detailed meanings of SFR will be given in the following sections.

1.1 Embedded Flash

The program can be loaded into the embedded 16KB Flash memory via its writer or In-System Programming (ISP). The high-quality Flash suitable for re-programming and data recording as EEPROM.

1.2 IO Pads

The SM39R16A6 has Four I/O ports: Port 0, Port 1, Port 2 and Port 3. Ports 0, 1 are 8-bit ports and Port 2, 3 are 7-bit ports. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. As description in section 5.

All the pads for P0, P1, P2 and P3 are with slew rate to reduce EMI. The IO pads can withstand 4KV ESD in human body mode guaranteeing the SM39R16A6's quality in high electro-static environments.

The RESET Pin can define as General I/O P3.4 when user use Internal RESET.

The XTAL2 and XTAL1 can define as P3.5 and P3.6 by writer or ISP when user use internal OSC as system clock. When user use external OSC as system clock and input into XTAL1, only XTAL2 can be defined as P3.5.

1.3 Instruction timing Selection

The conventional 52-series MCUs are 12T, i.e., 12 oscillator clocks per machine cycle. SM39R16A6 is a 1T to 8T MCU, i.e., its machine cycle is one-clock to eight-clock. In the other words, it can execute one instruction within one clock to only eight clocks.

Mnemonic: CKCON **Address: 8Eh**

7	6	5	4	3	2	1	0	Reset
-	ITS[2:0]			-	-	CLKOUT[1:0]		10H

ITS: Instruction timing select.

ITS [2:0]	Instruction timing
000	1T mode
001	2T mode (default)
010	3T mode
011	4T mode
100	5T mode
101	6T mode
110	7T mode
111	8T mode

The default is in 2T mode, and it can be changed to another Instruction timing mode if CKCON [6:4] (at address 8Eh) is change any time. Not every instruction can be executed with one machine cycle. The exact machine cycle number for all the instructions are given in the next section.

1.4 Clock Out Selection

The SM39R16A6 can generate a clock out signal at P3.5 when user use Oscillator (XTAL1 as clock input) or internal OSC as system clock. The CKCON [1:0] (at address 8Eh) can change any time.

CLKOUT: Clock output select.

CKCON [1:0]	Mode.
00	GPIO(default)
01	Fosc
10	Fosc/2
11	Fosc/4

1.5 RESET

1.5.1 Hardware RESET function

SM39R16A6 provides Internal reset circuit inside, the Internal reset time can set by writer or ISP.

Internal Reset time
25ms (default)
200ms
100ms
50ms
16ms
8ms
4ms

1.5.2 Software RESET function

SM39R16A6 provides one software reset mechanism to reset whole chip. To perform a software reset, the firmware must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the Software Reset register (SWRES) write attribute. After SWRES register obtain the write authority, the firmware can write FFh to the SWRES register. The hardware will decode a reset signal that “OR” with the other hardware reset. The SWRES register is self-reset at the end of the software reset procedure.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Software Reset function											
RSTS	Reset status register	A1h	-	LVRLP INTF	LVRLP F	PDRF	WDTF	SWRF	LVRF	PORF	00H
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
SWRES	Software Reset register	E7h	SWRES [7:0]								00H

1.5.3 Reset status

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	LVRLP INTF	LVRLPF	PDRF	WDTF	SWRF	LVRF	PORF	00H

LVRLPINTF: "Internal" Low voltage reset flag.

When MCU is reset by LVR_LP_INT, LVRLPINTF flag will be set to one by hardware. This flag clear by software.

LVRLPF: Low voltage reset (Low Power) flag.

When MCU is reset by LVR (Low Power), LVRLPF flag will be set to one by hardware. This flag clear by software.

PDRF: Pad reset flag.

When MCU is reset by reset pad, PDRF flag will be set to one by hardware. This flag clear by software.

WDTF: Watchdog timer reset flag.

When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software.

SWRF: Software reset flag.

When MCU is reset by software, SWRF flag will be set to one by hardware. This flag clear by software.

LVRF: Low voltage reset flag.

When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.

PORF: Power on reset flag.

When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

1.5.4 Time Access Key register (TAKEY)

Mnemonic: TAKEY **Address:F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Software reset register (SWRES) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the SWRES register write attribute.

That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

1.5.5 Software Reset register (SWRES)

Mnemonic: SWRES

Address:E7H

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**Reset**
SWRES [7:0]								00H

SWRES [7:0]: Software reset register bit. These 8-bit is self-reset at the end of the reset procedure.

SWRES [7:0] = FFh, software reset.

SWRES [7:0] = 00h ~ FEh, MCU no action.

1.5.6 Example of software reset

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah     ; enable SWRES write attribute
MOV SWRES, #0FFh ; software reset MCU
```

1.6 Clocks

The default clock is the 22.1184MHz Internal OSC. This clock is used during the initialization stage. The major work of the initialization stage is to determine the clock source used in normal operation.

The internal clock sources are from the internal OSC with difference frequency division As shown in Table 1-1, the clock source can set by writer.

Table 1-1: Selection of clock source

Clock source
external crystal (use XTAL1 and XTAL2 pins)
external crystal (only use XTAL1, the XTAL2 define as I/O)
22.1184MHz from internal OSC
11.0592MHz from internal OSC
5.5296MHz from internal OSC
2.7648MHz from internal OSC
1.3824MHz from internal OSC

There may be having a little variance in the frequency from the internal OSC. The max variance as giving in Table 1-2.

Table 1-2: Temperature with variance

Temperature	**Max Variance**
25℃	±2%

2. Instruction Set

All SM39R16A6 instructions are binary code compatible and perform the same functions as they do with the industry standard 8051. The following tables give a summary of the instruction set cycles of the SM39R16A6 Microcontroller core.

Table 2-1: Arithmetic operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	28-2F	1	1
ADD A,direct	Add direct byte to accumulator	25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	26-27	1	2
ADD A,#data	Add immediate data to accumulator	24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	38-3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	36-37	1	2
ADDC A,#data	Add immediate data to A with carry flag	34	2	2
SUBB A,Rn	Subtract register from A with borrow	98-9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	96-97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	94	2	2
INC A	Increment accumulator	04	1	1
INC Rn	Increment register	08-0F	1	2
INC direct	Increment direct byte	05	2	3
INC @Ri	Increment indirect RAM	06-07	1	3
INC DPTR	Increment data pointer	A3	1	1
DEC A	Decrement accumulator	14	1	1
DEC Rn	Decrement register	18-1F	1	2
DEC direct	Decrement direct byte	15	2	3
DEC @Ri	Decrement indirect RAM	16-17	1	3
MUL AB	Multiply A and B	A4	1	5
DIV	Divide A by B	84	1	5
DA A	Decimal adjust accumulator	D4	1	1

Table 2-2: Logic operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	58-5F	1	1
ANL A,direct	AND direct byte to accumulator	55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	56-57	1	2
ANL A,#data	AND immediate data to accumulator	54	2	2
ANL direct,A	AND accumulator to direct byte	52	2	3
ANL direct,#data	AND immediate data to direct byte	53	3	4
ORL A,Rn	OR register to accumulator	48-4F	1	1
ORL A,direct	OR direct byte to accumulator	45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	46-47	1	2
ORL A,#data	OR immediate data to accumulator	44	2	2
ORL direct,A	OR accumulator to direct byte	42	2	3
ORL direct,#data	OR immediate data to direct byte	43	3	4
XRL A,Rn	Exclusive OR register to accumulator	68-6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	66-67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	63	3	4
CLR A	Clear accumulator	E4	1	1
CPL A	Complement accumulator	F4	1	1
RL A	Rotate accumulator left	23	1	1
RLC A	Rotate accumulator left through carry	33	1	1
RR A	Rotate accumulator right	03	1	1
RRC A	Rotate accumulator right through carry	13	1	1
SWAP A	Swap nibbles within the accumulator	C4	1	1

Table 2-3: Data transfer

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	E8-EF	1	1
MOV A,direct	Move direct byte to accumulator	E5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	E6-E7	1	2
MOV A,#data	Move immediate data to accumulator	74	2	2
MOV Rn,A	Move accumulator to register	F8-FF	1	2
MOV Rn,direct	Move direct byte to register	A8-AF	2	4
MOV Rn,#data	Move immediate data to register	78-7F	2	2
MOV direct,A	Move accumulator to direct byte	F5	2	3
MOV direct,Rn	Move register to direct byte	88-8F	2	3
MOV direct1,direct2	Move direct byte to direct byte	85	3	4
MOV direct,@Ri	Move indirect RAM to direct byte	86-87	2	4
MOV direct,#data	Move immediate data to direct byte	75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	F6-F7	1	3
MOV @Ri,direct	Move direct byte to indirect RAM	A6-A7	2	5
MOV @Ri,#data	Move immediate data to indirect RAM	76-77	2	3
MOV DPTR,#data16	Load data pointer with a 16-bit constant	90	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	93	1	3
MOVC A,@A+PC	Move code byte relative to PC to accumulator	83	1	3
MOVX A,@Ri	Move external RAM (8-bit addr.) to A	E2-E3	1	3
MOVX A,@DPTR	Move external RAM (16-bit addr.) to A	E0	1	3
MOVX @Ri,A	Move A to external RAM (8-bit addr.)	F2-F3	1	4
MOVX @DPTR,A	Move A to external RAM (16-bit addr.)	F0	1	4
PUSH direct	Push direct byte onto stack	C0	2	4
POP direct	Pop direct byte from stack	D0	2	3
XCH A,Rn	Exchange register with accumulator	C8-CF	1	2
XCH A,direct	Exchange direct byte with accumulator	C5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator	C6-C7	1	3
XCHD A,@Ri	Exchange low-order nibble indir. RAM with A	D6-D7	1	3

Table 2-4: Program branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	xxx11	2	6
LCALL addr16	Long subroutine call	12	3	6
RET	from subroutine	22	1	4
RETI	from interrupt	32	1	4
AJMP addr11	Absolute jump	xxx01	2	3
LJMP addr16	Long iump	02	3	4
SJMP rel	Short jump (relative addr.)	80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	73	1	2
JZ rel	Jump if accumulator is zero	60	2	3
JNZ rel	Jump if accumulator is not zero	70	2	3
JC rel	Jump if carry flag is set	40	2	3
JNC	Jump if carry flag is not set	50	2	3
JB bit,rel	Jump if direct bit is set	20	3	4
JNB bit,rel	Jump if direct bit is not set	30	3	4
JBC bit,direct rel	Jump if direct bit is set and clear bit	10	3	4
CJNE A,direct rel	Compare direct byte to A and jump if not equal	B5	3	4
CJNE A,#data rel	Compare immediate to A and jump if not equal	B4	3	4
CJNE Rn,#data rel	Compare immed. to reg. and jump if not equal	B8-BF	3	4
CJNE @Ri,#data rel	Compare immed. to ind. and jump if not equal	B6-B7	3	4
DJNZ Rn,rel	Decrement register and jump if not zero	D8-DF	2	3
DJNZ direct,rel	Decrement direct byte and jump if not zero	D5	3	4
NOP	No operation	00	1	1

Table 2-5: Boolean manipulation

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	C3	1	1
CLR bit	Clear direct bit	C2	2	3
SETB C	Set carry flag	D3	1	1
SETB bit	Set direct bit	D2	2	3
CPL C	Complement carry flag	B3	1	1
CPL bit	Complement direct bit	B2	2	3
ANL C,bit	AND direct bit to carry flag	82	2	2
ANL C,/bit	AND complement of direct bit to carry	B0	2	2
ORL C,bit	OR direct bit to carry flag	72	2	2
ORL C,/bit	OR complement of direct bit to carry	A0	2	2
MOV C,bit	Move direct bit to carry flag	A2	2	2
MOV bit,C	Move carry flag to direct bit	92	2	3

3. Memory Structure

The SM39R16A6 memory structure follows general 8052 structure. It is integrate the expanded 1KB data memory and 16KB program memory.

3.1 Program Memory

The SM39R16A6 has 16KB on-chip flash memory which can be used as general program memory or EEPROM, on which include up to 1K byte specific ISP service program memory space. The address range for the 16K byte is $0000 to $3FFF. The address range for the ISP service program is $3C00 to $3FFF. The ISP service program size can be partitioned as N blocks of 128 byte (N=0 to 8). When N=0 means no ISP service program space available, total 16K byte memory used as program memory. When N=1 means address $3F80 to $3FFF reserved for ISP service program. When N=2 means memory address $3F00 to $3FFF reserved for ISP service program…etc. Value N can be set and programmed into SM39R16A6 information block by writer. As shown in Fig. 3-1

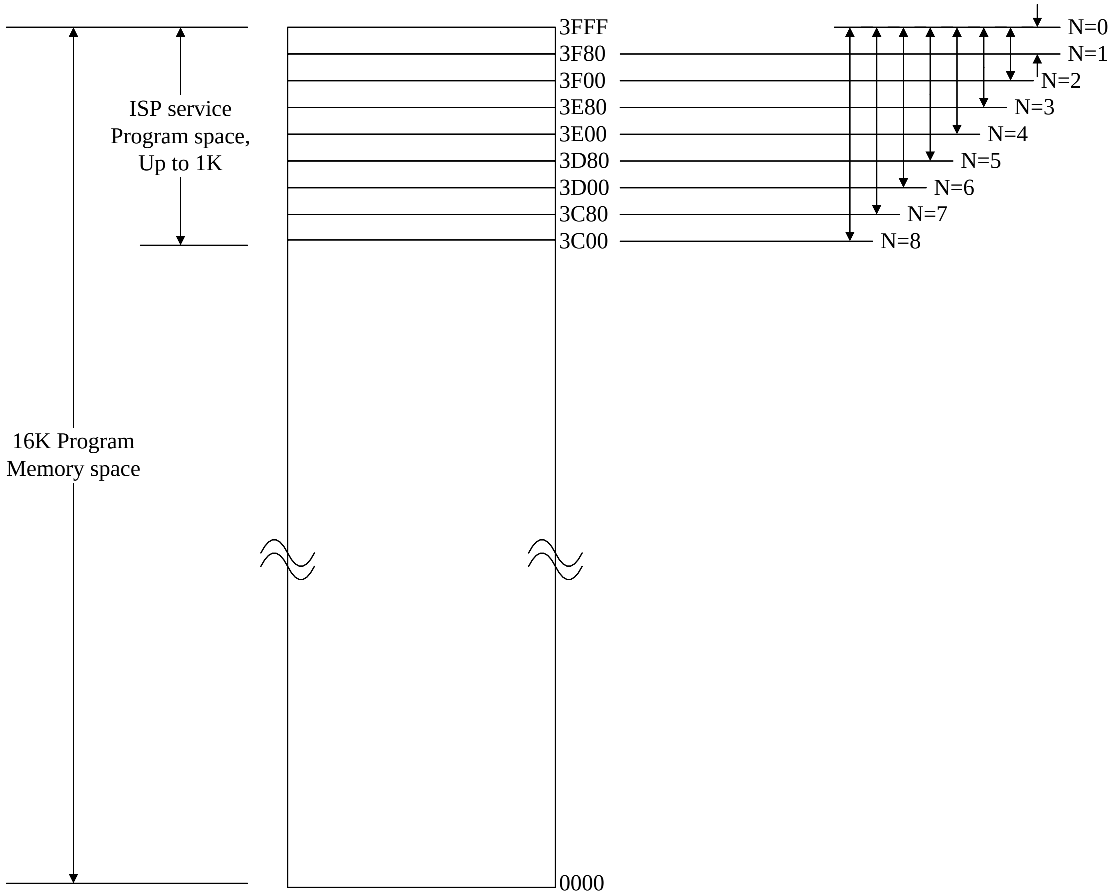


Fig. 3-1: SM39R16A6 programmable Flash

3.2 Data Memory

The SM39R16A6 has 1K + 256B on-chip SRAM, 256B of it are the same as general 8052 internal memory structure while the expanded 1K Bytes on-chip SRAM can be accessed by external memory addressing method (by instruction MOVX.). As shown in Fig. 3-2

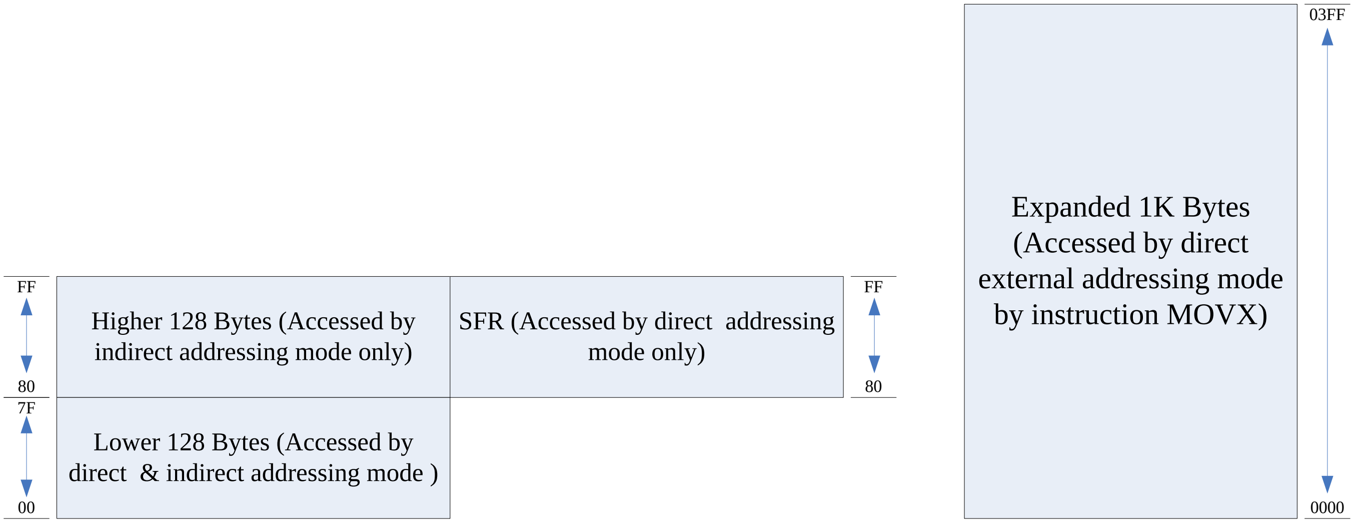

Expanded 1K Bytes (Accessed by direct external addressing mode by instruction MOVX)
03FF
0000
FF
80
7F
00
Higher 128 Bytes (Accessed by indirect addressing mode only)
SFR (Accessed by direct addressing mode only)
FF
80
Lower 128 Bytes (Accessed by direct & indirect addressing mode)

Fig. 3-2: RAM architecture

3.3 Data memory - lower 128 byte (00h to 7Fh)

Data memory 00h to FFh is the same as 8052.
The address 00h to 7Fh can be accessed by direct and indirect addressing modes.
Address 00h to 1Fh is register area.
Address 20h to 2Fh is memory bit area.
Address 30h to 7Fh is for general memory area.

3.4 Data memory - higher 128 byte (80h to FFh)

The address 80h to FFh can be accessed by indirect addressing mode.
Address 80h to FFh is data area.

3.5 Data memory - Expanded 1K Bytes (0000h ~ 03FFh)

From external address 0000h to 03FFh is the on-chip expanded SRAM area, total 1K Bytes. This area can be accessed by external direct addressing mode (by instruction MOVX). The address space of instruction MOVX @Ri, i=0, 1 is determined by RCON [7:0] of special function register $86 RCON (internal RAM control register). The default setting of RCON [7:0] is 00h (page0). One page of data RAM is 256 bytes.

Note: SM39R16A6 can not access (off-chip) external RAM.

MOVX @Ri, A MOVX A, @Ri	0 ≦ RCON[7:0] ≦ 3
	Addr [15:8] <= RCON[7:0]

4. CPU Engine

The SM39R16A6 engine is composed of four components:

(1) Control unit
(2) Arithmetic – logic unit
(3) Memory control unit
(4) RAM and SFR control unit

The SM39R16A6 engine allows to fetch instruction from program memory and to execute using RAM or SFR. The following chapter describes the main engine register.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
8051 Core											
ACC	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00H
B	B register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00H
PSW	Program status word	D0h	CY	AC	F0	RS[1:0]		OV	PSW.1	P	00H
SP	Stack Pointer	81h	SP[7:0]								07H
DPL	Data pointer low 0	82h	DPL[7:0]								00H
DPH	Data pointer high 0	83h	DPH[7:0]								00H
DPL1	Data pointer low 1	84h	DPL1[7:0]								00H
DPH1	Data pointer high 1	85h	DPH1[7:0]								00H
AUX	Auxiliary register	91h	BRGS	P21CC	-	P1UR	-	-	-	DPS	00H
CKCON	Clock control register	8Eh	-	ITS[2:0]			-	-	CLKOUT[1:0]		10H
IFCON	Interface control register	8Fh	-	CDPR	-	-	-	-	-	ISPE	00H
PAGESEL	Page Select	BEh	-	-	-	-	-	-	Page_ num	Page_ mode	00H

4.1 Accumulator

ACC is the Accumulator register. Most instructions use the accumulator to store the operand.

Mnemonic: ACC **Address: E0h**

7	6	5	4	3	2	1	0	Reset
ACC.7	ACC.6	ACC05	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00h

ACC[7:0]: The A (or ACC) register is the standard 8052 accumulator.

4.2 B Register

The B register is used during multiply and divide instructions. It can also be used as a scratch pad register to store temporary data.

Mnemonic: B **Address: F0h**

7	6	5	4	3	2	1	0	Reset
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00h

B[7:0]: The B register is the standard 8052 register that serves as a second accumulator.

4.3 Program Status Word

Mnemonic: PSW **Address: D0h**

7	6	5	4	3	2	1	0	Reset
CY	AC	F0	RS [1:0]		OV	F1	P	00h

CY: Carry flag.

AC: Auxiliary Carry flag for BCD operations.

F0: General purpose Flag 0 available for user.

RS[1:0]: Register bank select, used to select working register bank.

RS[1:0]	Bank Selected	Location
00	Bank 0	00h – 07h
01	Bank 1	08h – 0Fh
10	Bank 2	10h – 17h
11	Bank 3	18h – 1Fh

OV: Overflow flag.

F1: General purpose Flag 1 available for user.

P: Parity flag, affected by hardware to indicate odd/even number of “one” bits in the Accumulator, i.e. even parity.

4.4 Stack Pointer

The stack pointer is a 1-byte register initialized to 07h after reset. This register is incremented before PUSH and CALL instructions, causing the stack to start from location 08h.

Mnemonic: SP **Address: 81h**

7	6	5	4	3	2	1	0	Reset
SP [7:0]								07h

SP[7:0]: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

4.5 Data Pointer

The data pointer (DPTR) is 2-bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (e.g. MOV DPTR, #data16) or as two separate registers (e.g. MOV DPL,#data8). It is generally used to access the external code or data space (e.g. MOVC A, @A+DPTR or MOVX A,@DPTR respectively).

Mnemonic: DPL **Address: 82h**

7	6	5	4	3	2	1	0	Reset
DPL [7:0]								00h

DPL[7:0]: Data pointer Low 0

Mnemonic: DPH **Address: 83h**

7	6	5	4	3	2	1	0	Reset
DPH [7:0]								00h

DPH [7:0]: Data pointer High 0

4.6 Data Pointer 1

The Dual Data Pointer accelerates the moves of data block. The standard DPTR is a 16-bit register that is used to address external memory or peripherals. In the SM39R16A6 core the standard data pointer is called DPTR, the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit is located in LSB of AUX register (DPS).

The user switches between pointers by toggling the LSB of AUX register. All DPTR-related instructions use the currently selected DPTR for any activity.

Mnemonic: DPL1 **Address: 84h**

7	6	5	4	3	2	1	0	Reset
DPL1 [7:0]								00h

DPL1[7:0]: Data pointer Low 1

Mnemonic: DPH1 **Address: 85h**

7	6	5	4	3	2	1	0	Reset
DPH1 [7:0]								00h

DPH1[7:0]: Data pointer High 1

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	P21CC	-	P1UR	-	-	-	DPS	00H

DPS: Data Pointer select register.

DPS = 1 is selected DPTR1.

4.7 Clock control register

Mnemonic: CKCON **Address: 8Eh**

7	6	5	4	3	2	1	0	Reset
-	ITS[2:0]			-	-	CLKOUT[1:0]		10H

ITS[2:0]: Instruction timing select.

ITS [2:0]	Mode
000	1T mode
001	2T mode (default)
010	3T mode
011	4T mode
100	5T mode
101	6T mode
110	7T mode
111	8T mode

CLKOUT[1:0]: Clock output select.

CLKOUT[1:0]	Mode
00	GPIO(default)
01	Fosc
10	Fosc/2
11	Fosc/4

It can be used when the system clock is the internal RC oscillator.

4.8 Interface control register

Mnemonic: IFCON **Address: 8Fh**

7	6	5	4	3	2	1	0	Reset
-	CDPR	-	-	-	-	-	ISPE	00H

CDPR: Code protect (Read Only)

ISPE: ISP function enable bit

ISPE = 1, enable ISP function

ISPE = 0, disable ISP function

4.9 PAGESEL (Page Select)

The SM39R16A6 provide two different methods to set Special Function Register (SFR) are as follow:

- SFR Method 1 (Indirect Mode): This method is only an SFR page. If you want to use PWM registers of the Method 2, can be used indirectly addressable setting.

  Example: Write a data 0x80h to PWMEN Register in Method 1.

  ```
  PAGESEL = 0x00;                   // Method 1.
  PWMADDR = 0xF5;                   // PWMEN indirect address: 0xF5 (Indirect mode)
                                        // (Refer Page1 Table of the Method 2)
  PWMDATA = 0x80;                // Write data 0x80 to PWMEN.
  ```

- SFR Method 2 (Page Mode): This method provides two SFR page to set the registers.

  Example: Write a data 0x80 to PWMEN Register in Method 2, Page 1.

  ```
  PAGESEL = 0x03;   // Method 2, Page 1 (Page mode)
  PWMEN = 0x80;     // Write data 0x80 to PWMEN.
  ```

- SFR Page Mode Table:

Page_mode	Page_num	SFR Select
0	0	SFR Method 1
0	1	SFR Method 1
1	0	SFR Method 2, Page 0
1	1	SFR Method 2, Page 1

Mnemonic: PAGESEL **Address: BEh**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	Page_ num	Page_ mode	00H

Page_num: This flag is used only in the SFR method 2

0 = page 0 mode.

1 = page 1 mode.

Page_mode: This flag is used to select SFR register table.

0 : SFR Method 1 (indirect mode).

1 : SFR Method 2 (page mode).

5. GPIO

5.1 SFR Setting Method

The SM39R16A6 has four I/O ports: Port 0, Port 1, Port 2, Port 3. Ports 0, 1, 2 are 8-bit ports and Ports 2, 3 are 7-bit ports. These are: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin. All I/O port pins on the SM39R16A6 may be configured by software to one fo four types on a pin-by-pin basis, shown as below:

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
I/O port function register											
P0M0	Port 0 output mode 0	D2h	P0M0 [7:0]								~OP18
P0M1	Port 0 output mode 1	D3h	P0M1[7:0]								00H
P1M0	Port 1 output mode 0	D4h	P1M0[7:0]								00H
P1M1	Port 1 output mode 1	D5h	P1M1[7:0]								00H
P2M0	Port 2 output mode 0	D6h	-	P2M0[6:0]							00H
P2M1	Port 2 output mode 1	D7h	-	P2M1[6:0]							00H
P3M0	Port 3 output mode 0	DAh	-	P3M0[6:0]							00H
P3M1	Port 3 output mode 1	DBh	-	P3M1[6:0]							00H

*OP18 by writer programming set.

PxM1.y	PxM0.y	Port output mode
0	0	Quasi-bidirectional (standard 8051 port outputs) (pull-up)
0	1	Push-pull
1	0	Input only (high-impedance)
1	1	Open drain

The RESET Pin can define as General I/O P3.4 when user use Internal RESET.

The XTAL2 and XTAL1 can define as P3.5 and P3.6 by writer when user use internal OSC as system clock. When user use external OSC as system clock and input into XTAL1, only XTAL2 can be defined as P3.5.

For general-purpose applications, every pin can be assigned to either high or low independently. As shown below:

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Ports											
Port 3	Port 3	B0h	-	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	7Fh
Port 2	Port 2	A0h	-	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	7Fh
Port 1	Port 1	90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh
Port 0	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	OP19

*OP19 by writer programming set.

Mnemonic: P0 **Address: 80h**

7	6	5	4	3	2	1	0	Reset
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	OP19

P0.7~ 0: Port0 [7] ~ Port0[0]

Mnemonic: P1 **Address: 90h**

7	6	5	4	3	2	1	0	Reset
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh

P1.7~ 0: Port1 [7] ~ Port1 [0]

Mnemonic: P2 **Address: A0h**

7	6	5	4	3	2	1	0	Reset
-	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	7Fh

P2.6~ 0: Port2 [6] ~ Port2 [0]

Mnemonic: P3 **Address: B0h**

7	6	5	4	3	2	1	0	Reset
-	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	7Fh

P3.6~ 0: Port3 [6] ~ Port3 [0]

5.2 Software of Writer Setting Method

Please Setting the “IO Output Mode" item in the "Configuration" window, it can change the I/O mode of P1~P3 to the “Quasi-bidirectional (standard 8051 port outputs) (pull-up)” or Input only (high-impedance) mode, When MCU after reset and initial. It is supported the version D of MCU after.

6. Multiplication Division unit

This on-chip arithmetic unit provides 32-bit division, 16-bit multiplication, shift and normalize features. All operations are unsigned integer operation.

Mnemonic	Description	Direct	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Multiplication Division Unit											
PCON	Power control	87H	SMOD	MDUF	-	-	-	-	STOP	IDLE	40H
ARCON	Arithmetic Control register	EFh	MDEF	MDOV	SLR	SC[4:0]					00H
MD0	Multiplication/Division Register 0	E9h	MD0[7:0]								00H
MD1	Multiplication/Division Register 1	EAh	MD1[7:0]								00H
MD2	Multiplication/Division Register 2	EBh	MD2[7:0]								00H
MD3	Multiplication/Division Register 3	ECh	MD3[7:0]								00H
MD4	Multiplication/Division Register 4	EDh	MD4[7:0]								00H
MD5	Multiplication/Division Register 5	EEh	MD5[7:0]								00H

6.1 Operating registers of the MDU

The MDU is handled by eight registers, which are memory mapped as special function registers. The arithmetic unit allows operations concurrently to and independent of the CPU’s activity. Operands and results registers are MD0 to MD5. Control register is ARCON. Any calculation of the MDU overwrites its operands.

Mnemonic: ARCON **Address: EFh**

7	6	5	4	3	2	1	0	Reset
MDEF	MDOV	SLR	SC[4:0]					00H

MDEF- Multiplocation Division Errot Flag.

The MDEF is an error flag. The error flag is read only. The error flag indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation). The error flag mechanism is automatically enabled with the first write to MD0 and disabled with the final read instruction from MD3 multiplication or shift/normalizing) or MD5 (division) in phase three.

The error flag is set when:

1. Phase two in process and write access to MDx registers (restart or interrupt calculations)

The error flag is reset only if:

The second phase two finished (arithmetic operation successful completed) and read access to MDx registers.

MDOV - Multiplication Division Overflow flag. The overflow flag is read only.

The overflow flag is set when:

1. Division by Zero

2. Multiplication with a result greater then 0000FFFFh

3. Start of normalizing if the most significant bit of MD3 is set(MD3.7 = 1)

   The overflow flag is reset when:

   Write access to MD0 register (Start Phase one)

SLR - Shift direction bit.

SLR = 0 – shift left operation.

SLR = 1 – shift right operation.

SC[4:0] - Shift counter.

When preset with 00000b, normalizing is selected. After normalize sc.0 – sc.4 contains the number of normalizing shifts performed. When sc.4 – sc.0 ≠ 0, shift- operation is started. The number of shifts performed is determined by the count written to sc.4 to sc.0. sc.4 – MSB ... sc.0 – LSB

6.2 Operation of the MDU

Operations of the MDU consist of three phases:

6.2.1 First phase: Loading the MDx registers.

The type of calculation the MDU has to perform is selected following the order in which the mdx registers are written to.

Table 6-1 MDU registers write sequence

Operation	32bit/16bit	16bit/16bit	16bit x 16bit	shift/normalizing
First write	MD0 Dividend Low	MD0 Dividend Low	MD0 Multiplicand Low	MD0 LSB
	MD1 Dividend	MD1 Dividend High	MD4 Multiplicator Low	MD1
	MD2 Dividend		MD1 Multiplicand High	MD2
	MD3 Dividend High			MD3 MSB
	MD4 Divisor Low	MD4 Divisor Low		
Last write	MD5 Divisor High	MD5 Divisor High	MD5 Multiplicator High	ARCON start conversion

A write to MD0 is the first transfer to be done in any case. Next writes must be done as shown in Table 6-1 to determine MDU operation. Last write finally starts selected operation.

6.2.2 Second phase: Executing calculation.

During executing operation, the MDU works on its own parallel to the CPU. When MDU is finished, the MDUF register will be set to one by hardware and the flag will clear at next calculation.

Mnemonic: PCON **Address: 87h**

7	6	5	4	3	2	1	0	Reset
SMOD	MDUF					STOP	IDLE	40H

MDUF: MDU finish flag.

When MDU is finished, the MDUF will be set by hardware and the bit will clear by hardware at next calculation.

Table 6-2 MDU execution times

Operation	Number of Tclk
Division 32bit/16bit	17 clock cycles
Division 16bit/16bit	9 clock cycles
Multiplication	11 clock cycles

Shift	min 3 clock cycles , max 18 clock cycles
Normalize	min 4 clock cycles , max 19 clock cycles

6.2.3 Third phase: Reading the result from the MDx registers.

Read out sequence of the first MDx registers is not critical but the last read (from MD5 - division and MD3 - multiplication, shift and normalizing) determines the end of a whole calculation (end of phase three).

Table 6-3 MDU registers read sequence

Operation	32Bit/16Bit	16Bit/16Bit	16Bit x 16Bit	shift/normalizing
First read	MD0 Quotient Low	MD0 Quotien Low	MD0 Product Low	MD0 LSB
	MD1 Quotient	MD1 Quotien High	MD1 Product	MD1
	MD2 Quotient		MD2 Product	MD2
	MD3 Quotient High			
	MD4 Remainder L	MD4 Remainder Low		
Last read	MD5 Remainder H	MD5 Remainder High	MD3 Product High	MD3 MSB

6.3 Normalizing

All reading zeroes of integers variables in registers MD0 to MD3 are removed by shift left operations. The whole operation is completed when the MSB (most significant bit) of MD3 register contains a ’1’. After normalizing, bits ARCON.4 (MSB) to ARCON.0 (LSB) contain the number of shift left operations, which were done.

6.4 Shifting

SLR bit (ARCON.5) has to contain the shift direction, and ARCON.4 to ARCON.0 the shift count (which must not be 0). During shift, zeroes come into the left or right end of the registers MD0 or MD3, respectively.

7. Timer 0 and Timer 1

The SM39R16A6 has three 16-bit timer/counter registers: Timer 0, Timer 1 and Timer 2. All can be configured for counter or timer operations.

In timer mode, the Timer 0 register or Timer 1 register is incremented every 1/12/96 machine cycles, which means that it counts up after every 1/12/96 periods of the clk signal. It's dependent on SFR(PFCON).

In counter mode, the register is incremented when the falling edge is observed at the corresponding input pin T0 or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function registers (TMOD and TCON) are used to select the appropriate mode.

Mnemonic	**Description**	**Dir.**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**RST**
Timer 0 and 1											
TL0	Timer 0 , low byte	8Ah	TL0[7:0]								00H
TH0	Timer 0 , high byte	8Ch	TH0[7:0]								00H
TL1	Timer 1 , low byte	8Bh	TL1[7:0]								00H
TH1	Timer 1 , high byte	8Dh	TH1[7:0]								00H
TMOD	Timer Mode Control	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
TCON	Timer/Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H
PFCON	Peripheral Frequency control register	D9h	-	-	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

7.1 Timer/Counter mode control register (TMOD)

Mnemonic: TMOD **Address: 89h**

7	6	5	4	3	2	1	0	Reset
GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
Timer 1				Timer 0				

GATE: If set, enables external gate control (pin INT0 or INT1 for Counter 0 or 1, respectively). When INT0 or INT1 is high, and TRx bit is set (see TCON register), a counter is incremented every falling edge on T0 or T1 input pin.

C/T: Selects Timer or Counter operation. When set to 1, a counter operation is performed, when cleared to 0, the corresponding register will function as a timer.

M1	M0	Mode	Function
0	0	Mode0	13-bit counter/timer, with 5 lower bits in TL0 or TL1 register and 8 bits in TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are hold at zero.
0	1	Mode1	16-bit counter/timer.
1	0	Mode2	8-bit auto-reload counter/timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.
1	1	Mode3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8 bit timers / counters.

7.2 Timer/counter control register (TCON)

Mnemonic: TCON **Address: 88h**

7	6	5	4	3	2	1	0	Reset
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

TF1: Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR1: Timer 1 Run control bit. If cleared, Timer 1 stops.

TF0: Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR0: Timer 0 Run control bit. If cleared, Timer 0 stops.

IE1: Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.

IT1: Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt. IT1=1, interrupt 1 select falling edge trigger. IT1=0, interrupt1 select low level trigger.

IE0: Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT0 is observed. Cleared when interrupt is processed.

IT0: Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt. IT0=1, interrupt 0 select falling edge trigger. IT0=0, interrupt 0 select low level trigger.

7.3 Enhance Interrupt Trigger SFR(ENHIT)

Mnemonic: ENHIT **Address: E5h**

7	6	5	4	3	2	1	0	Reset
-	ENHIT1	-	ENHIT0	-	-	-	-	07H

Note: It is supported the version D of MCU after.

ENHIT1: Interrupt 1 edge trigger control bit.

When ENHIT1 is set to 0 and IT1 is set to 1, The method of edge trigger is falling edge trigger.

When ENHIT1 and IT1 both are set to 1, The method of edge trigger is rising edge trigger.

	ENHIT1=0	**ENHIT1=1**
IT1=0	INT1 low level trigger	INT1 low level trigger
IT1=1	INT1 failing edge trigger	INT1 rising edge trigger

ENHIT0: Interrupt 0 edge trigger control bit.

When ENHIT0 is set to 0 and IT0 is set to 1, The method of edge trigger is falling edge trigger.

When ENHIT0 and IT0 both are set to 1, The method of edge trigger is rising edge trigger.

	ENHIT0=0	**ENHIT0=1**
IT0=0	INT0 low level trigger	INT0 low level trigger
IT0=1	INT0 failing edge trigger	INT0 rising edge trigger

7.4 Peripheral Frequency control register

Mnemonic: PFCON **Address: D9h**

7	6	5	4	3	2	1	0	Reset
-	-	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

T1PS[1:0]: Timer1 Prescaler select

T0PS[1:0]	**Prescaler**
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

T0PS[1:0]: Timer0 Prescaler select

T0PS[1:0]	Prescaler
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

7.5 Mode 0 (13-bit Counter/Timer)

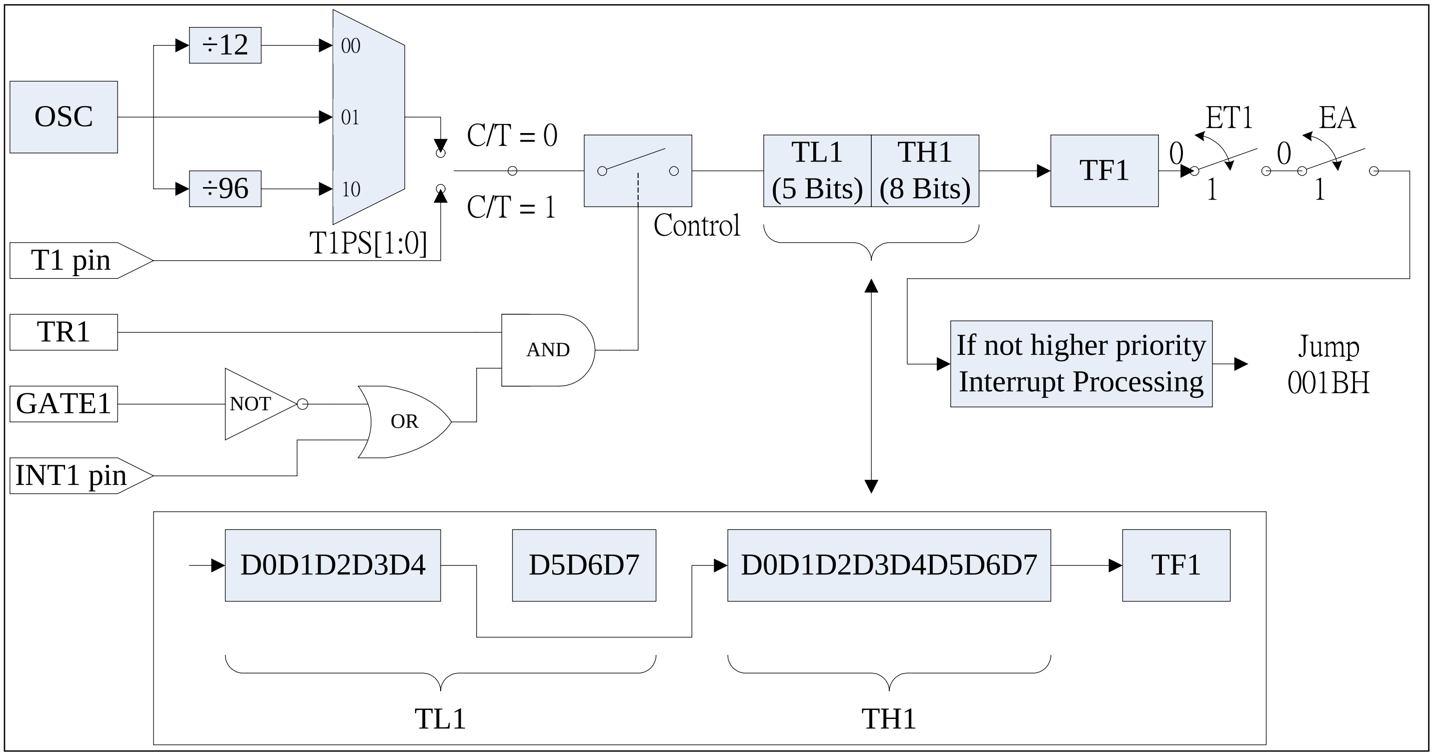

÷12
00
OSC
01
÷96
10
T1PS[1:0]
C/T = 0
C/T = 1
Control
TL1
(5 Bits)
TH1
(8 Bits)
TF1
ET1
EA
0
1
0
1
T1 pin
TR1
AND
GATE1
NOT
OR
INT1 pin
If not higher priority
Interrupt Processing
Jump
001BH
D0D1D2D3D4
D5D6D7
D0D1D2D3D4D5D6D7
TF1
TL1
TH1

Fig. 7-1: Mode 0 -13 bit Timer / Counter operation

7.6 Mode 1 (16-bit Counter/Timer)

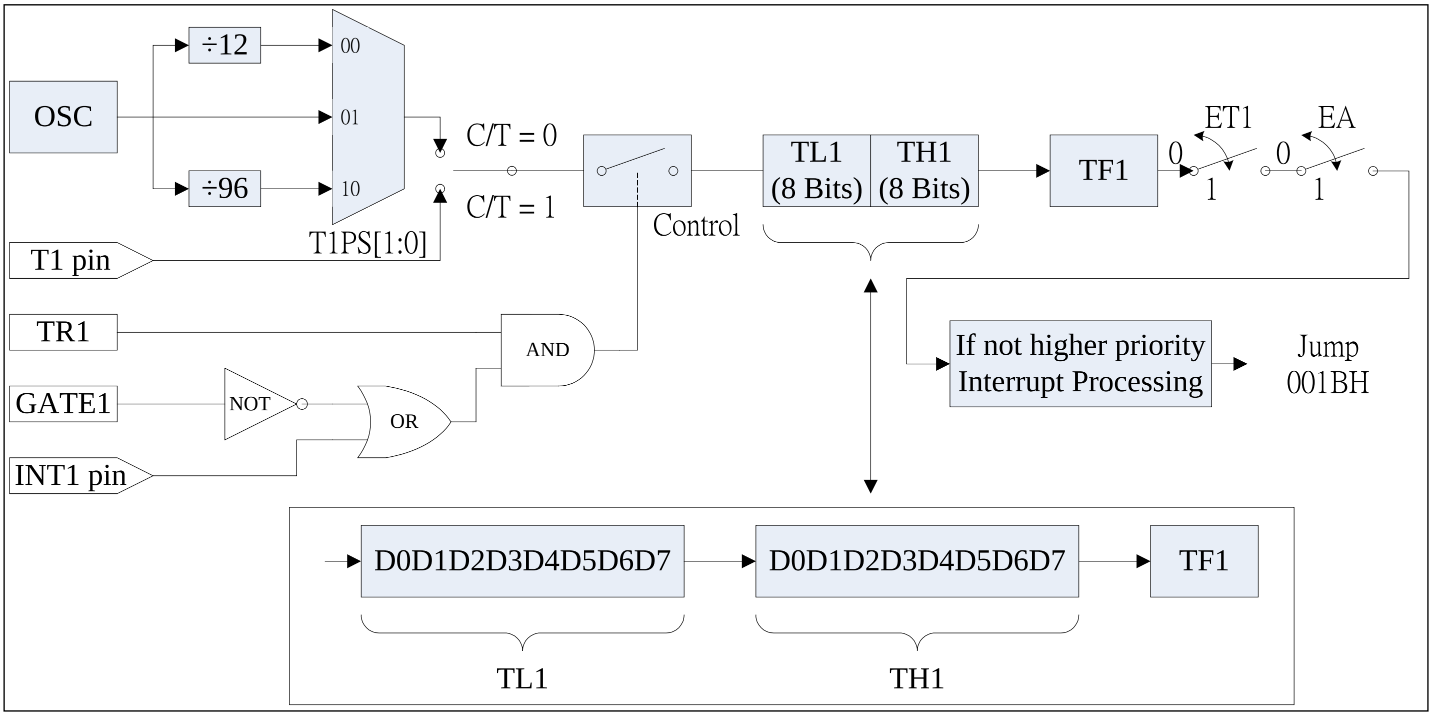

÷12
00
OSC
01
÷96
10
T1PS[1:0]
C/T = 0
C/T = 1
Control
TL1 (8 Bits)
TH1 (8 Bits)
TF1
ET1
EA
0
1
0
1
T1 pin
TR1
AND
GATE1
NOT
OR
INT1 pin
If not higher priority Interrupt Processing
Jump 001BH
D0D1D2D3D4D5D6D7
D0D1D2D3D4D5D6D7
TF1
TL1
TH1

Fig. 7-2: Mode 1 16 bit Counter/Timer operation

7.7 Mode 2 (8-bit auto-reload Counter/Timer)

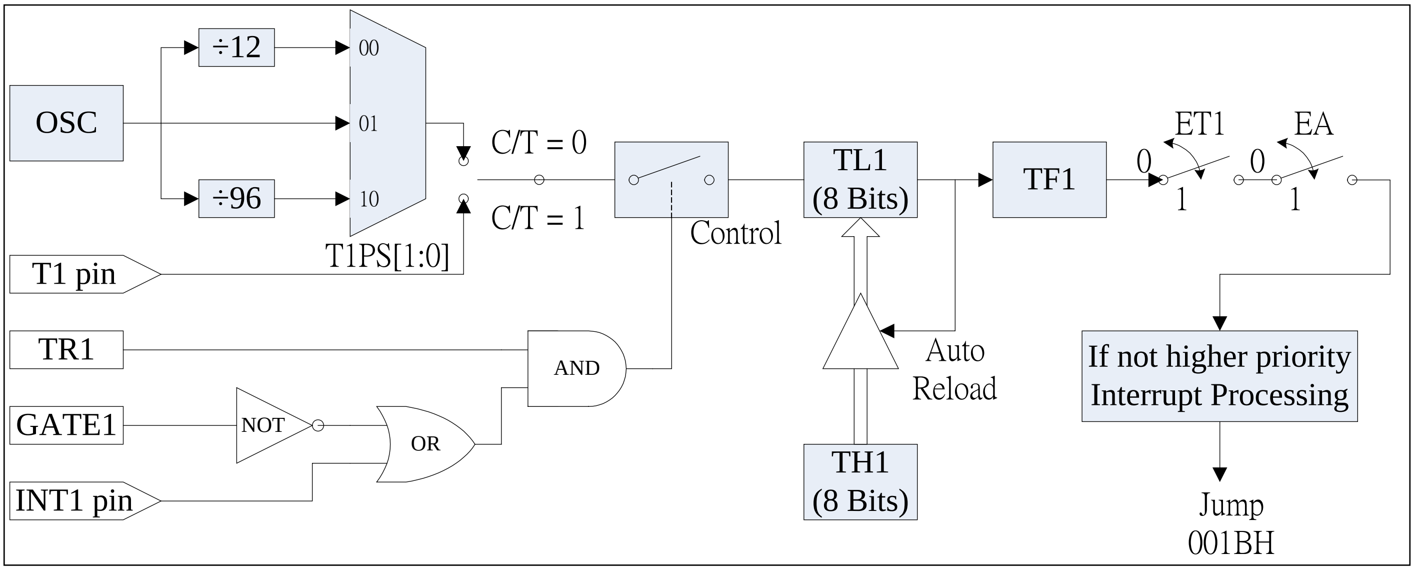

÷12
00
OSC
01
÷96
10
T1PS[1:0]
C/T = 0
C/T = 1
Control
TL1 (8 Bits)
TF1
ET1
EA
0
1
0
1
T1 pin
TR1
AND
GATE1
NOT
OR
INT1 pin
Auto Reload
TH1 (8 Bits)
If not higher priority Interrupt Processing
Jump 001BH

Fig. 7-3: Mode 2 8-bit auto-reload Counter/Timer operation.

7.8 Mode 3 (Timer 0 acts as two independent 8 bit Timers / Counters)

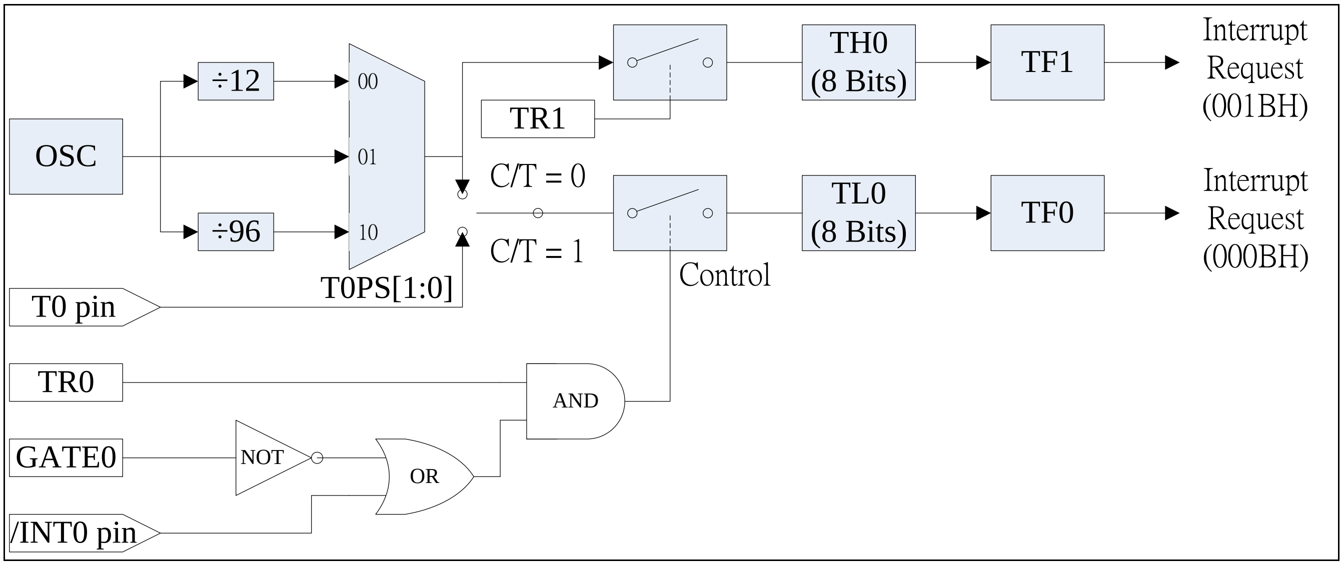

OSC
÷12
÷96
00
01
10
T0PS[1:0]
TR1
C/T = 0
C/T = 1
Control
TH0
(8 Bits)
TL0
(8 Bits)
TF1
TF0
Interrupt
Request
(001BH)
Interrupt
Request
(000BH)
T0 pin
TR0
GATE0
/INT0 pin
NOT
OR
AND

Fig. 7-4: Mode 3 Timer 0 acts as two independent 8 bit Timers / Counters operatin

8. Timer 2 and Capture Compare Unit

Timer 2 is not only a 16-bit timer, also a 4-channel unit with compare, capture and reload functions. It is very similar to the programmable counter array (PCA) in some other MCUs except pulse width modulation (PWM).

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Timer 2 and Capture Compare Unit											
AUX	Auxiliary register	91h	BRGS	P21CC	-	P1UR	-	-	-	DPS	00H
T2CON	Timer 2 control	C8h	T2PS[2:0]			T2R[1:0]		-	T2I[1:0]		00H
CCCON	Compare/Capture Control	C9h	CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H
CCEN	Compare/Capture Enable register	C1h	-	COCAM1[2:0]			-	COCAM0[2:0]			00H
CCEN2	Compare/Capture Enable 2 register	D1h	-	COCAM3[2:0]			-	COCAM2[2:0]			00H
TL2	Timer 2, low byte	CCh	TL2[7:0]								00H
TH2	Timer 2, high byte	CDh	TH2[7:0]								00H
CRCL	Compare/Reload/ Capture register, low byte	CAh	CRCL[7:0]								00H
CRCH	Compare/Reload/ Capture register, high byte	CBh	CRCH[7:0]								00H
CCL1	Compare/Capture register 1, low byte	C2h	CCL1[7:0]								00H
CCH1	Compare/Capture register 1, high byte	C3h	CCH1[7:0]								00H
CCL2	Compare/Capture register 2, low byte	C4h	CCL2[7:0]								00H
CCH2	Compare/Capture register 2, high byte	C5h	CCH2[7:0]								00H
CCL3	Compare/Capture register 3, low byte	C6h	CCL3[7:0]								00H
CCH3	Compare/Capture register 3, high byte	C7h	CCH3[7:0]								00H

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	P21CC	-	P1UR	-	-	-	DPS	00H

P21CC : P21CC = 0 – Capture/Compare function on P1.

P21CC = 1 – Capture/Compare function on P2.

Mnemonic: T2CON **Address: C8h**

7	6	5	4	3	2	1	0	Reset
T2PS[2:0]			T2R[1:0]		-	T2I[1:0]		00H

T2PS[2:0]: Prescaler select bit:

T2PS = 000 – timer 2 is clocked with the oscillator frequency.

T2PS = 001 – timer 2 is clocked with 1/2 of the oscillator frequency.

T2PS = 010 – timer 2 is clocked with 1/4 of the oscillator frequency.

T2PS = 011 – timer 2 is clocked with 1/6 of the oscillator frequency.

T2PS = 100 – timer 2 is clocked with 1/8 of the oscillator frequency.

T2PS = 101 – timer 2 is clocked with 1/12 of the oscillator frequency.

T2PS = 110 – timer 2 is clocked with 1/24 of the oscillator frequency.

T2R[1:0]: Timer 2 reload mode selection

T2R[1:0] = 0X – Reload disabled.

T2R[1:0] = 10 – Mode 0: Auto Reload.

T2R[1:0] = 11 – Mode 1: T2EX Falling Edge Reload.

T2I[1:0]: Timer 2 input selection

T2I[1:0] = 00 – Timer 2 stop.

T2I[1:0] = 01 – Input frequency from prescaler (T2PS[2:0]).

T2I[1:0] = 10 – Timer 2 is incremented by external signal at pin T2.

T2I[1:0] = 11 – internal clock input is gated to the Timer 2.

Mnemonic: CCCON **Address: C9h**

7	6	5	4	3	2	1	0	Reset
CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H

CCI3: Compare/Capture 3 interrupt control bit.

CCI3 = 1 is enable.

CCI2: Compare/Capture 2 interrupt control bit.

CCI3 = 1 is enable.

CCI1: Compare/Capture 1 interrupt control bit.

CCI3 = 1 is enable.

CCI0: Compare/Capture 0 interrupt control bit.

CCI3 = 1 is enable.

CCF3: Compare/Capture 3 flag set by hardware. This flag can be cleared by software.

CCF2: Compare/Capture 2 flag set by hardware. This flag can be cleared by software.

CCF1: Compare/Capture 1 flag set by hardware. This flag can be cleared by software.

CCF0: Compare/Capture 0 flag set by hardware. This flag can be cleared by software.

Compare/Capture interrupt share T2 interrupt vector.

Mnemonic: CCEN **Address: C1h**

7	6	5	4	3	2	1	0	Reset
-	COCAM1[2:0]			-	COCAM0[2:0]			00H

COCAM1[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC1.

101 - Capture on falling edge at pin CC1.

110 - Capture on both rising and falling edge at pin CC1.

111 - Capture on write operation into register CC1.

COCAM0[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC0.

101 - Capture on falling edge at pin CC0.

110 - Capture on both rising and falling edge at pin CC0.

111 - Capture on write operation into register CC0.

Mnemonic: CCEN2 **Address: D1h**

7	6	5	4	3	2	1	0	Reset
-	COCAM3[2:0]			-	COCAM2[2:0]			00H

COCAM3[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC3.

101 - Capture on falling edge at pin CC3.

110 - Capture on both rising and falling edge at pin CC3.

111 - Capture on write operation into register CC3.

COCAM2[2:0] 000 - Compare/Capture disable.

001 - Compare enable but no output on Pin.

010 - Compare mode 0.

011 - Compare mode 1.

100 - Capture on rising edge at pin CC2.

101 - Capture on falling edge at pin CC2.

110 - Capture on both rising and falling edge at pin CC2.

111 - Capture on write operation into register CC2.

8.1 Timer 2 function

Timer 2 can operate as timer, event counter, or gated timer as explained later.

8.1.1 Timer mode

In this mode Timer 2 can by incremented in various frequency that depending on the prescaler. The prescaler is selected by bit T2PS[2:0] in register T2CON. As shown in Fig. 8-1

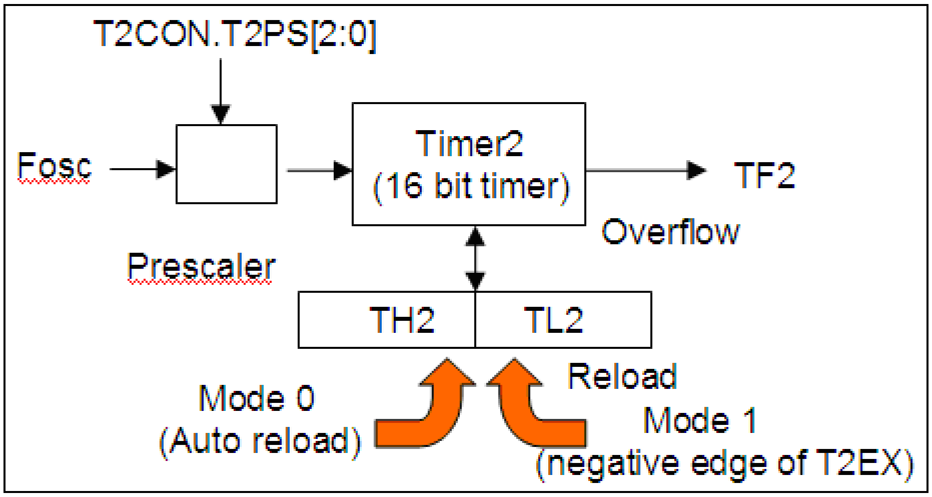

T2CON.T2PS[2:0]
Fosc
Prescaler
Timer2
(16 bit timer)
TF2
Overflow
TH2
TL2
Reload
Mode 0
(Auto reload)
Mode 1
(negative edge of T2EX)

Fig. 8-1: Timer mode and Reload mode function

8.1.2 Event counter mode

In this mode, the timer is incremented when external signal T2 change value from 1 to 0. The T2 input is sampled in every cycle. Timer 2 is incremented in the cycle following the one in which the transition was detected. As shown in Fig. 8-2.

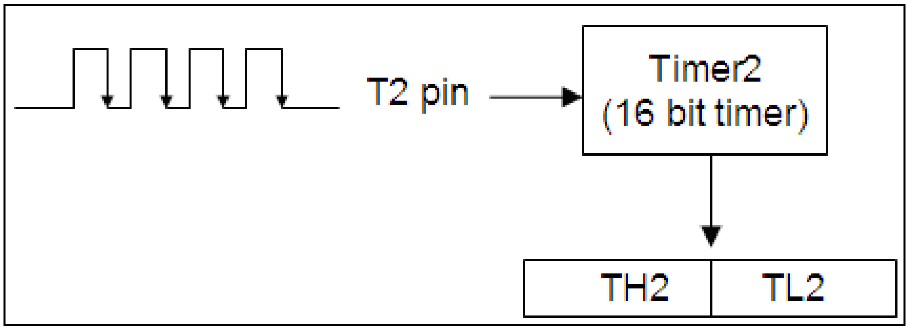

T2 pin
Timer2
(16 bit timer)
TH2
TL2

Fig. 8-2: Event counter mode function

8.1.3 Gated timer mode

In this mode, the internal clock which incremented timer 2 is gated by external signal T2. As shown in Fig. 8-3

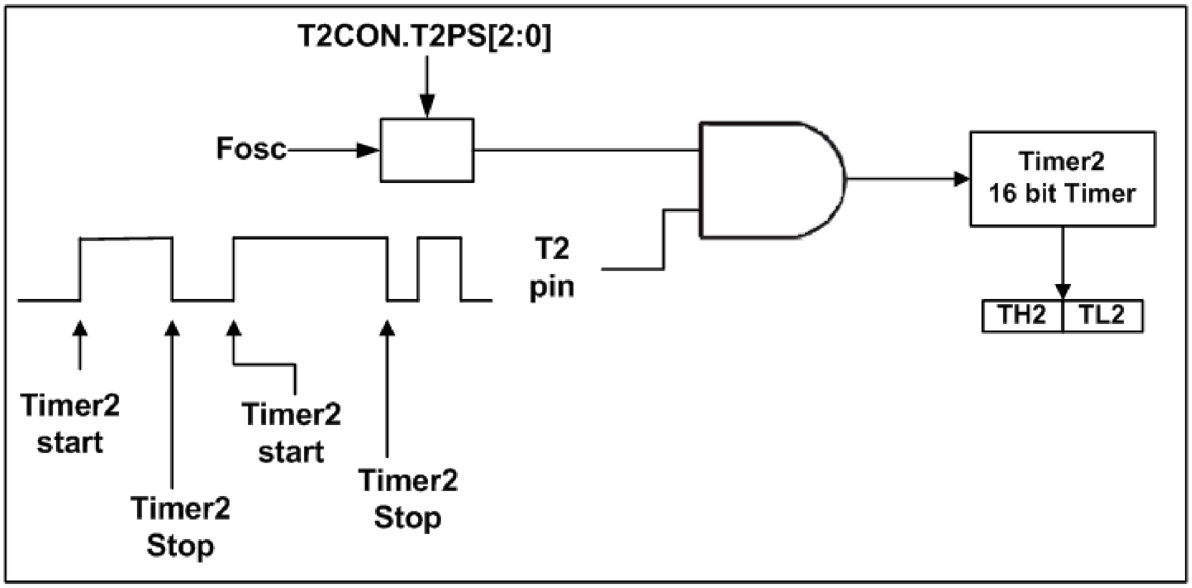

T2CON.T2PS[2:0]
Fosc
T2
pin
Timer2
16 bit Timer
TH2
TL2
Timer2
start
Timer2
Stop
Timer2
start
Timer2
Stop

Fig. 8-3: Gated timer mode function

8.1.4 Reload of Timer 2

Reload (16-bit reload from the crc register) can be executed in the following two modes:

Mode 0: Reload signal is generate by a Timer 2 overflows – autoreload.

Mode 1: Reload signal is generate by a negative transition at the corresponding input pin T2EX.

8.2 Compare function

In the four independent comparators, the value stored in any compare/capture register is compared with the contents of the timer register. The compare modes 0 and 1 are selected by bits C0CAMx. In both compare modes, the results of comparison arrives at Port 1 within the same machine cycle in which the internal compare signal is activated.

8.2.1 Compare Mode 0

In mode 0, when the value in Timer 2 equals the value of the compare register, the output signal changes from low to high. It goes back to a low level on timer overflow. In this mode, writing to the port will have no effect, because the input line from the internal bus and the write-to-latch line are disconnected. As shown in Fig. 8-4 illustrates the function of compare mode 0.

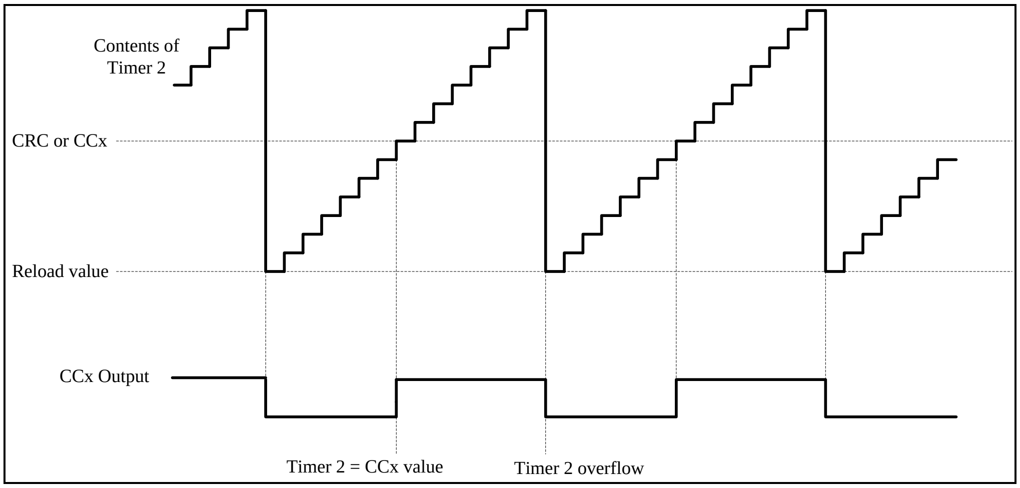


Fig. 8-4: Compare mode 0 function

8.2.2 Compare Mode 1

In compare mode 1, the transition of the output signal can be determined by software. A timer 2 overflow causes no output change. In this mode, both transitions of a signal can be controlled. As shown in Fig. 8-5 and Fig. 8-6 a functional diagram of a register/port configuration in compare Mode 1. In compare Mode 1, the value is written first to the "Shadow Register", when compare signal is active, this value is transferred to the output register.

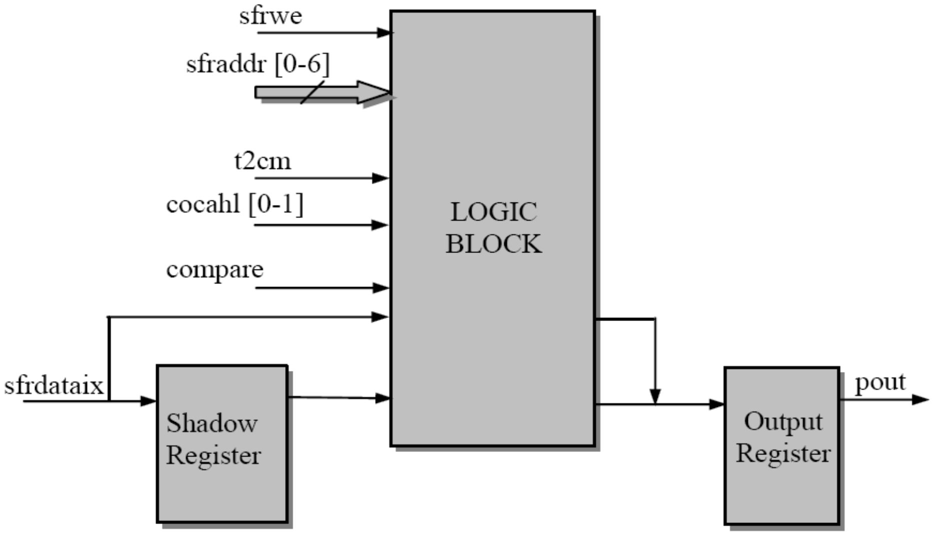


Fig. 8-5: Mode 1 Register/Port Function

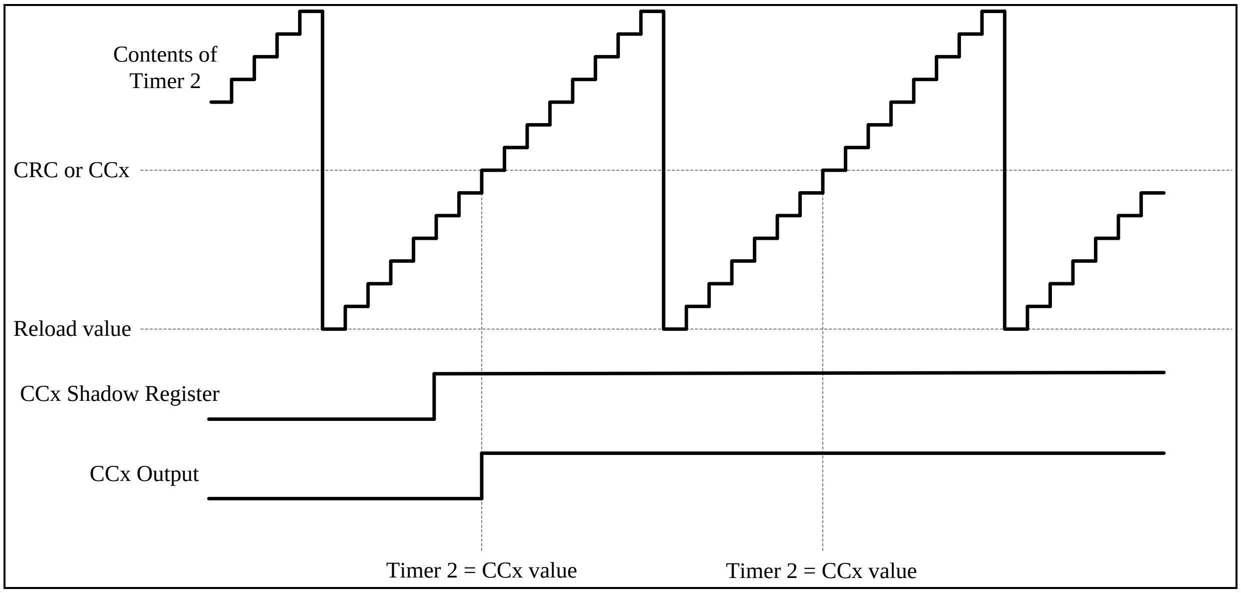

Contents of Timer 2
CRC or CCx
Reload value
CCx Shadow Register
CCx Output
Timer 2 = CCx value
Timer 2 = CCx value

Fig. 8-6: Compare mode 1 function

8.3 Capture function

Actual timer/counter contents can be saved into registers CCx or CRC upon an external event (mode 0) or a software write operation (mode 1).

8.3.1 Capture Mode 0 (by Hardware)

In mode 0, value capture of Timer 2 is executed when:
(1) Rising edge on input CC0-CC3
(2) Falling edge on input CC0-CC3
(3) Both rising and falling edge on input CC0-CC3

The contents of Timer 2 will be latched into the appropriate capture register. As shown in Fig. 8-7

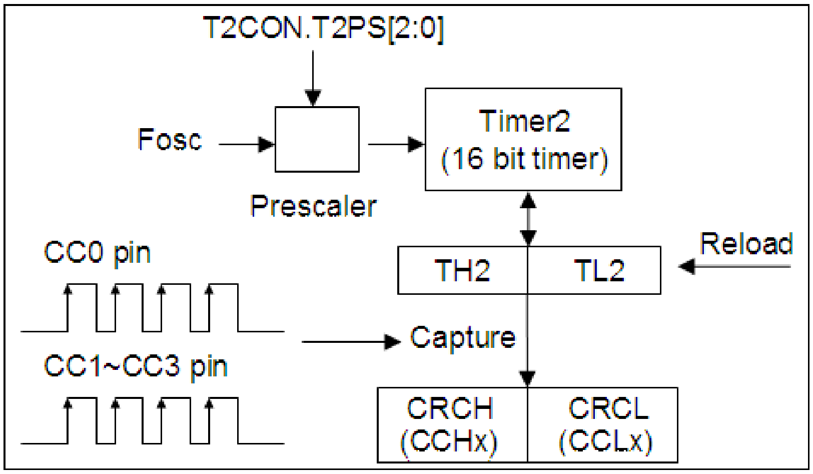

T2CON.T2PS[2:0]
Fosc
Prescaler
Timer2
(16 bit timer)
CC0 pin
TH2
TL2
Reload
Capture
CC1~CC3 pin
CRCH
(CCHx)
CRCL
(CCLx)

Fig. 8-7: Capture mode 0 function

8.3.2 Capture Mode 1(by Software)

In mode 1, value capture of timer 2 is caused by writing any value into the low-order byte of the dedicated capture register. The value written to the capture register is irrelevant to this function. The contents of Timer 2 will be latched into the appropriate capture register. As shown in Fig. 8-8

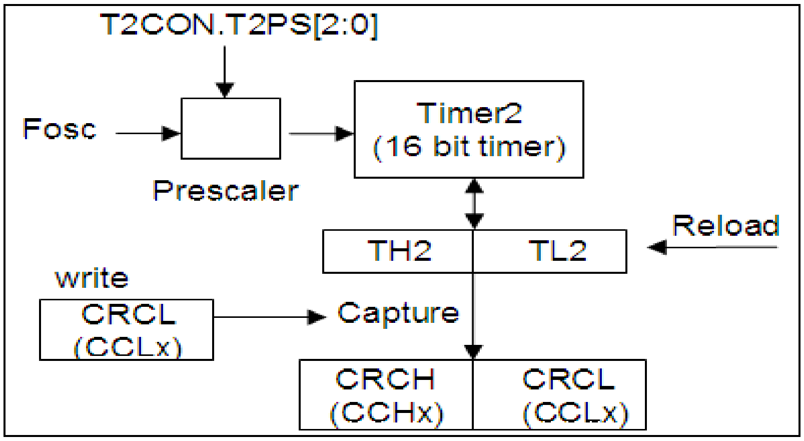

T2CON.T2PS[2:0]
Fosc
Prescaler
Timer2
(16 bit timer)
TH2
TL2
Reload
write
CRCL
(CCLx)
Capture
CRCH
(CCHx)
CRCL
(CCLx)

Fig. 8-8: Capture mode 1 function

9. Serial interface

The serial buffer consists of two separate registers, a transmit buffer and a receive buffer.

Writing data to the Special Function Register SBUF sets this data in serial output buffer and starts the transmission. Reading from the SBUF reads data from the serial receive buffer. The serial port can simultaneously Transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the first byte before transmission of the second byte is completed.

Mnemonic	**Description**	**Dir.**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**RST**
Serial interface											
PCON	Power control	87H	SMOD	MDUF	-	-	-	-	STOP	IDLE	40H
AUX	Auxiliary register	91h	BRGS	P21CC	-	P1UR	-	-	-	DPS	00H
SCON	Serial Port control register	98H	SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H
SRELL	Serial Port reload register low byte	AAH	SREL.7	SREL.6	SREL.5	SREL.4	SREL.3	SREL.2	SREL.1	SREL.0	00H
SRELH	Serial Port reload register high byte	BAH	-	-	-	-	-	-	SREL.9	SREL.8	00H
SBUF	Serial Port data buffer	99H	SBUF[7:0]								00H
PFCON	Peripheral Frequency control register	D9h	-	-	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

Mnemonic: AUX **Address: 91h**

7	6	5	4	3	2	1	0	Reset
BRGS	P21CC		P1UR		-	-	DPS	00H

BRGS: Baud rate generator.

BRGS = 0 - baud rate generator from Timer 1.

BRGS = 1 - baud rate generator by SREL.

P1UR: P1UR = 0 - Serial interface function on P3.

P1UR = 1 - Serial interface function on P1.

Mnemonic: SCON **Address: 98h**

7	6	5	4	3	2	1	0	Reset
SM0	SM1	SM2	REN	TB8	RB8	TI	RI	00H

SM0, SM1: Serial Port 0 mode selection.

SM0	SM1	Mode
0	0	0
0	1	1
1	0	2
1	1	3

The 4 modes in UART, Mode 0 ~ 3, are explained later.

SM2: Enables multiprocessor communication feature.

REN: If set, enables serial reception. Cleared by software to disable reception.

TB8: The 9th transmitted data bit in modes 2 and 3. Set or cleared by the CPU depending on the function it performs such as parity check, multiprocessor communication etc.

RB8: In modes 2 and 3, it is the 9th data bit received. In mode 1, if SM2 is 0, RB8 is the stop bit. In mode 0, this bit is not used. Must be cleared by software.

TI: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.

RI: Receive interrupt flag, set by hardware after completion of a serial reception. Must be cleared by software.

9.1 Serial interface

The Serial Interface can operate in the following 4 modes:

SM0	SM1	Mode	Description	Board Rate
0	0	0	Shift register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Variable

Here Fosc is the crystal or oscillator frequency.

9.1.1 Mode 0

Pin RXD serves as input and output. TXD outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in SCON as follows: RI = 0 and REN = 1. In other modes, a start bit when REN = 1 starts receiving serial data. As shown in Fig. 9-1 and Fig. 9-2

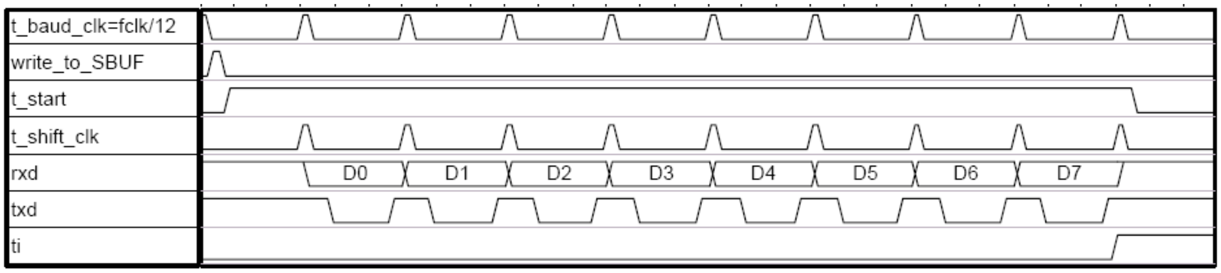


Fig. 9-1: Transmit mode 0

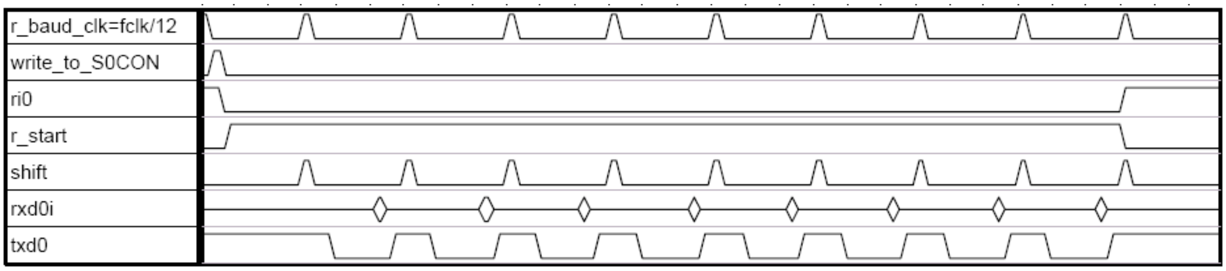


Fig. 9-2: Receive mode 0

9.1.2 Mode 1

Pin RXD serves as input, and TXD serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading SBUF, and stop bit sets the flag RB8 in the Special Function Register SCON. In mode 1 either internal baud rate generator or timer 1 can be use to specify baud rate. As shown in Fig. 9-3 and Fig. 9-4

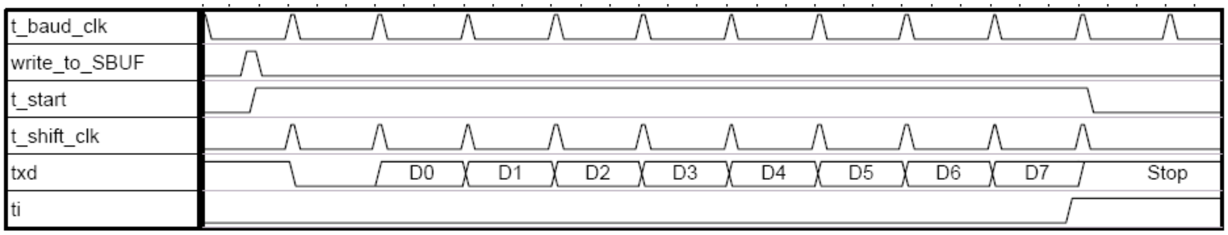

t_baud_clk
write_to_SBUF
t_start
t_shift_clk
txd
ti
D0
D1
D2
D3
D4
D5
D6
D7
Stop

Fig. 9-3: Transmit mode 1

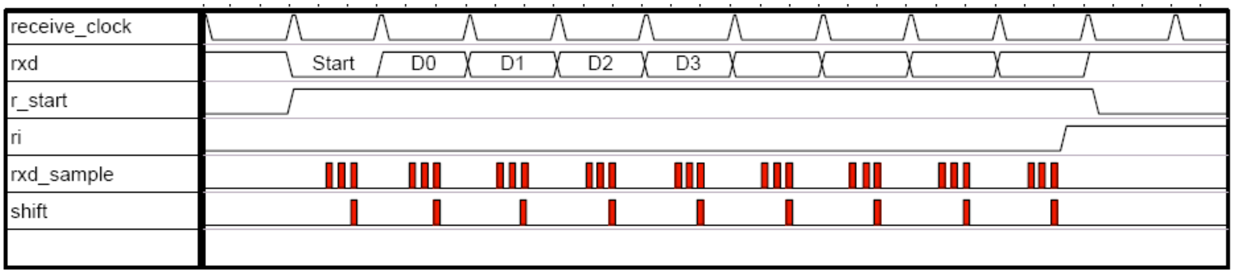

receive_clock
rxd
r_start
ri
rxd_sample
shift
Start
D0
D1
D2
D3

Fig. 9-4: Receive mode 1

9.1.3 Mode 2

This mode is similar to Mode 1, with two differences. The baud rate is fixed at 1/32 (SMOD=1) or 1/64(SMOD=0) of oscillator frequency and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable 9th bit, and a stop bit (1). The 9th bit can be used to control the parity of the serial interface: at transmission, bit TB8 in SCON is output as the 9th bit, and at receive, the 9th bit affects RB8 in Special Function Register SCON.

9.1.4 Mode 3

The only difference between Mode 2 and Mode 3 is that in Mode 3 either internal baud rate generator or timer 1 can be use to specify baud rate. As shown in Fig. 9-5 and Fig. 9-6.

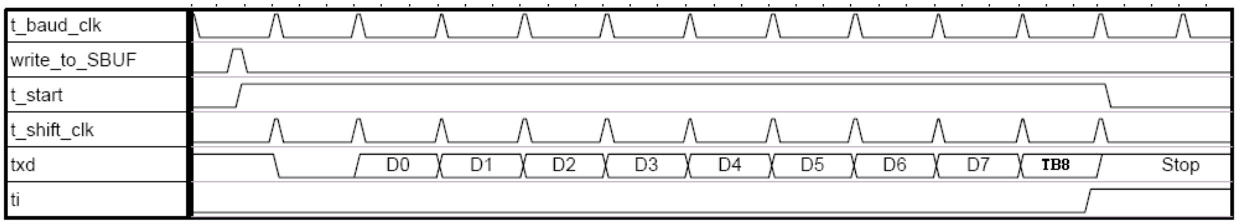

t_baud_clk
write_to_SBUF
t_start
t_shift_clk
txd
ti
D0
D1
D2
D3
D4
D5
D6
D7
TB8
Stop

Fig. 9-5: Transmit modes 2 and 3

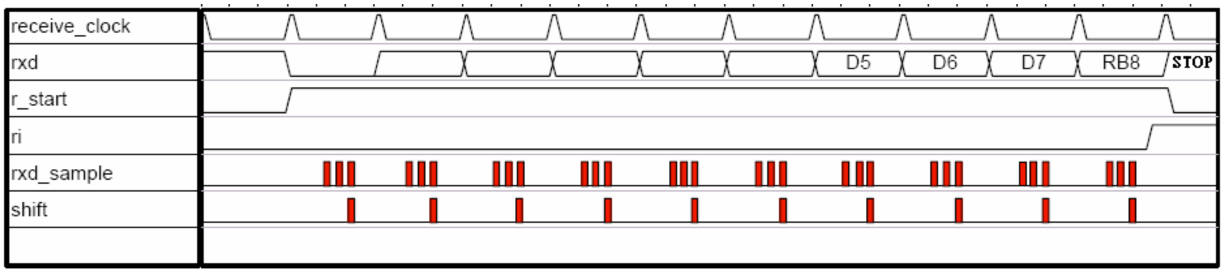


Fig. 9-6: Receive modes 2 and 3

9.2 Multiprocessor Communication of Serial Interface

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface can be used for multiprocessor communication. In this case, the slave processors have bit SM2 in SCON set to 1. When the master processor outputs slave's address, it sets the 9th bit to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If there is a match, the addressed slave will clear SM2 and receive the rest of the message, while other slaves will leave SM2 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the 9th bit set to 0, so no serial port receive interrupt will be generated in unselected slaves.

9.3 Peripheral Frequency control register

Mnemonic: PFCON **Address: D9h**

7	6	5	4	3	2	1	0	Reset
-	-	SRELPS[1:0]		T1PS[1:0]		T0PS[1:0]		00H

SRELPS[1:0]: SREL Prescaler select

SRELPS[1:0]	**Prescaler**
00	Fosc/64
01	Fosc /32

T1PS[1:0]: Timer1 Prescaler select

T1PS[1:0]	**Prescaler**
00	Fosc/12
01	Fosc
10	Fosc/96
11	reserved

9.4 Baud rate generator

9.4.1 Serial interface modes 1 and 3

9.4.1.1 When BRGS = 0 (in Special Function Register AUX).

(1) T1PS[1:0] is 00

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times \text{F}_{\text{osc}}}{32 \times 12 \times (256 - \text{TH1})}$$

(2) T1PS[1:0] is 01

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times \text{F}_{\text{osc}}}{32 \times (256 - \text{TH1})}$$

(3) T1PS[1:0] is 10

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times \text{F}_{\text{osc}}}{32 \times 96 \times (256 - \text{TH1})}$$

9.4.1.2 When BRGS = 1 (in Special Function Register AUX).

(1) SRELPS[1:0] is 00

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times \text{F}_{\text{osc}}}{64 \times (2^{10} - \text{SREL})}$$

(2) SRELPS[1:0] is 01

$$\text{Baud Rate} = \frac{2^{\text{SMOD}} \times \text{F}_{\text{osc}}}{32 \times (2^{10} - \text{SREL})}$$

10. Watchdog timer

The Watch Dog Timer (WDT) is an 8-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter. User should check WDTF bit of WDTC register whenever un-predicted reset happened. After an external reset the watchdog timer is disabled and all registers are set to zeros.

The watchdog timer has a free running on-chip RC oscillator (23 KHz). The WDT will keep on running even after the system clock has been turned off (for example, in sleep mode). During normal operation or sleep mode, a WDT time-out (if enabled) will cause the MCU to reset. The WDT can be enabled or disabled any time during the normal mode. Please refer the WDTE bit of WDTC register. The default WDT time-out period is approximately 178.0ms (WDTM [3:0] = 0100b).

The WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit3 ~ bit0 (WDTM [3:0]) of Watch Dog Timer Control Register (WDTC) should be set accordingly. As shown in Table 10-1.

$$WDTCLK = \frac{23\mathrm{KHz}}{2^{\mathrm{WDTM}}}$$

$$\text{Watchdog reset time} = \frac{256}{\mathrm{WDTCLK}}$$

Table 10-1: WDT time-out period

WDTM [3:0]	Divider (23 KHz RC oscillator in)	Time period @ 23KHz
0000	1	11.1ms
0001	2	22.2ms
0010	4	44.5ms
0011	8	89.0ms
0100	16	178.0ms (default)
0101	32	356.1ms
0110	64	712.3ms
0111	128	1.4246s
1000	256	2.8493s
1001	512	5.6987s
1010	1024	11.397s
1011	2048	22.795s
1100	4096	45.590s
1101	8192	91.180s
1110	16384	182.36s
1111	32768	364.72s

Note: RC oscillator (23 KHz), about ± 20% of variation

When MCU is reset, the MCU will be read WDTEN control bit status. When WDTEN bit is set to 1, the watchdog function will be disabled no matter what the WDTE bit status is. When WDTEN bit is clear to 0, the watchdog function will be enabled if WDTE bit is set to 1 by program. User can to set WDTEN on the writer or ISP.

The program can enable the WDT function by programming 1 to the WDTE bit premise that WDTEN control bit is clear to 0. After WDTE set to 1, the 8 bit-counter starts to count with the selected time base source clock which set by WDTM [3:0]. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when MCU been reset, either hardware reset or WDT reset. As shown in Fig. 10-1.

Once the watchdog is started it cannot be stopped. User can refreshed the watchdog timer to zero by writing 0x55 to Watch Dog Timer refresh Key (WDTK) register. This will clear the content of the 8-bit counter and let the counter re-start to count from the beginning. The watchdog timer must be refreshed regularly to prevent reset request signal from becoming active.

When Watchdog timer is overflow, the WDTF flag will set to one and automatically reset MCU. The WDTF flag can be clear by software or external reset or power on reset.

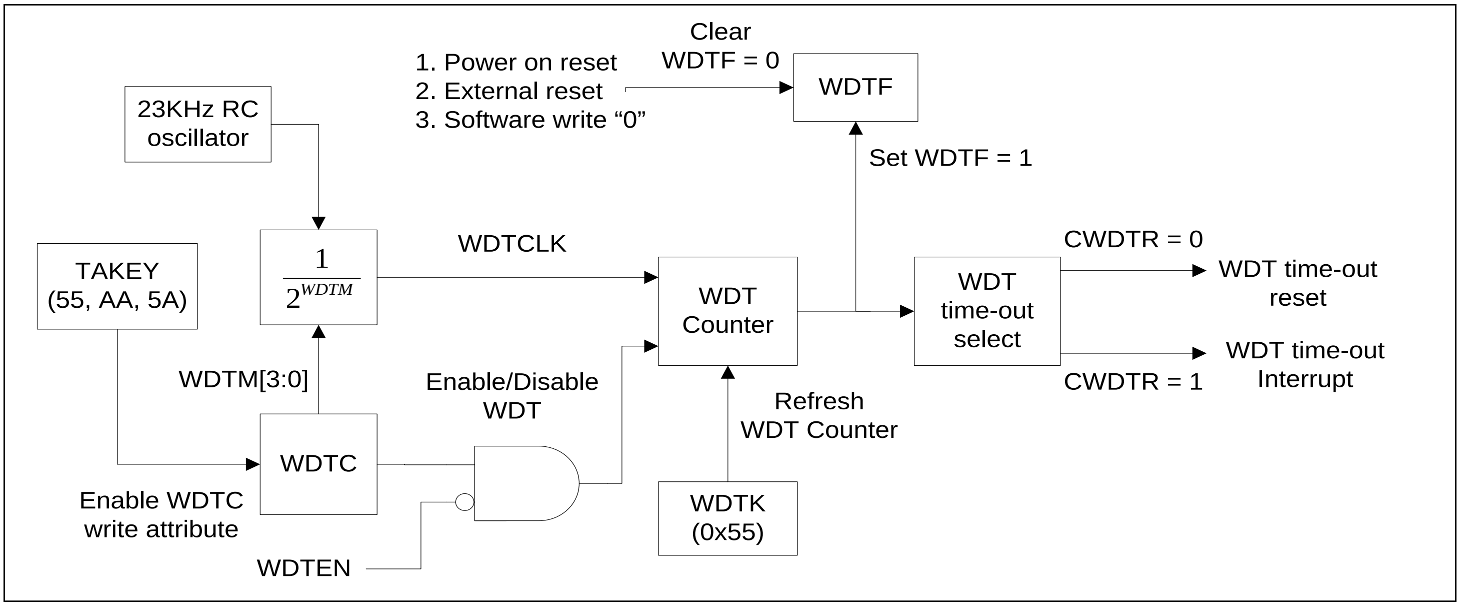

Clear
WDTF = 0
1. Power on reset
2. External reset
3. Software write “0”
WDTF
23KHz RC oscillator
Set WDTF = 1
TAKEY (55, AA, 5A)
$\frac{1}{2^{WDTM}}$
WDTCLK
WDT Counter
WDT time-out select
CWDTR = 0
WDT time-out reset
CWDTR = 1
WDT time-out Interrupt
WDTM[3:0]
Enable/Disable WDT
Refresh WDT Counter
WDTC
Enable WDTC write attribute
WDTK (0x55)
WDTEN

Fig. 10-1: Watchdog timer block diagram

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Watchdog Timer											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
WDTC	Watchdog timer control register	B6h	-	CWDTR	WDTE	-	WDTM [3:0]				04H
WDTK	Watchdog timer refresh key	B7h	WDTK[7:0]								00H
RSTS	Reset status register	A1h	-	LVRLP INTF	LVRLP F	PDRF	WDTF	SWRF	LVRF	PORF	00H

Mnemonic: TAKEY **Address: F7h**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Watchdog timer control register (WDTC) is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the WDTC write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

Mnemonic: WDTC **Address: B6h**

7	6	5	4	3	2	1	0	Reset
-	CWDTR	WDTE	-	WDTM [3:0]				04H

CWDTR: Watch dog states select bit(Support stop mode wakeup)

CWDTR = 0 - Enable watch dog reset.

CWDTR = 1 - Enable watch dog interrupt.

WDTE: Control bit used to enable Watchdog timer.
The WDTE bit can be used only if WDTEN is "0". If the WDTEN bit is "0", then WDT can be disabled / enabled by the WDTE bit.

WDTE = 0 - Disable WDT.

WDTE = 1 - Enable WDT.
The WDTE bit is not used if WDTEN is "1". That is, if the WDTEN bit is "1", WDT is always disabled no matter what the WDTE bit status is. The WDTE bit can be read and written.

WDTM [3:0]: WDT clock source divider bit. As seen in Fig. 10-1 to reference the WDT time-out period.

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	LVRLP INTF	LVRLP F	PDRF	WDTF	SWRF	LVRF	PORF	00h

WDTF: Watchdog timer reset flag. When MCU is reset by watchdog, WDTF flag will be set to one by hardware. This flag clear by software

Mnemonic: WDTK **Address: B7h**

7	6	5	4	3	2	1	0	Reset
WDTK[7:0]								00h

WDTK: Watchdog timer refresh key.
A programmer must write 0x55 into WDTK register, and then the watchdog timer will be cleared to zero.

For example 1, if enable WDT and select time-out reset period is 2.8493s.

First, programming the information block OP3 bit7 WDTEN to “0”.

Secondly,

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah     ; enable WDTC write attribute.
MOV WDTC, #28h      ; Set WDTM [3:0] = 1000b. Set WDTE =1 to enable WDT function.
.
.
.
MOV WDTK, #55h      ; Clear WDT timer to 0.
```

For example 2, if enable WDT and select time-out Interrupt period is 178.0ms.

First, programming the information block OP3 bit7 WDTEN to “0”.

Secondly,

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah     ; enable WDTC write attribute.
MOV WDTC, #64h      ;Set WDTM [3:0] = 0100b. ;Set WDTE =1 to enable WDT function
                    ; and Set CWDTR =1 to enable period interrupt function
```

11. Interrupt

The SM39R16A6 provides 12 interrupt sources with four priority levels. Each source has its own request flag(s) located in a special function register. Each interrupt requested by the corresponding flag could individually be enabled or disabled by the enable bits in SFR's IEN0, IEN1.

When the interrupt occurs, the engine will vector to the predetermined address as given in Table 11-1. Once interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction RETI. When an RETI is performed, the processor will return to the instruction that would have been next when interrupt occurred.

When the interrupt condition occurs, the processor will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled once per machine cycle, and then samples are polled by hardware. If the sample indicates a pending interrupt when the interrupt is enabled, then interrupt request flag is set. On the next instruction cycle the interrupt will be acknowledged by hardware forcing an LCALL to appropriate vector address.

Interrupt response will require a varying amount of time depending on the state of microcontroller when the interrupt occurs. If microcontroller is performing an interrupt service with equal or greater priority, the new interrupt will not be invoked. In other cases, the response time depends on current instruction. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle for detecting the interrupt and six cycles for perform the LCALL.

Table 11-1: Interrupt vectors

	Interrupt Request Flags	**Interrupt Vector Address**	**Interrupt Number *(use Keil C Tool)**
1	IE0 – External interrupt 0	0003h	0
2	TF0 – Timer 0 interrupt	000Bh	1
3	IE1 – External interrupt 1	0013h	2
4	TF1 – Timer 1 interrupt	001Bh	3
5	RI/TI – Serial channel interrupt	0023h	4
6	TF2/EXF2 – Timer 2 interrupt	002Bh	5
7	PWMIF – PWM interrupt	0043h	8
8	SPIIF – SPI interrupt	004Bh	9
9	ADCIF – A/D converter interrupt	0053h	10
10	LVIIF – Low Voltage Interrupt	0063h	12
11	IICIF – IIC interrupt	006Bh	13
12	WDT – Watchdog interrupt	008Bh	17

*See Keil C about C51 User's Guide about Interrupt Function description

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
Interrupt											
IEN0	Interrupt Enable 0 register	A8H	EA	-	ET2	ES	ET1	EX1	ET0	EX0	00H
IEN1	Interrupt Enable 1 register	B8H	EXEN2	-	IEIIC	IELVI	-	IEADC	IESPI	-	00H
IEN2	Interrupt Enable 2 register	9AH	-	-	-	-	-	-	EWDT	-	00H
IRCON	Interrupt request register	C0H	EXF2	TF2	IICIF	LVIIF	-	ADCIF	SPIIF	-	00H
IRCON2	Interrupt request register 2	97H	-	-	-	-	-	-	WDTIF	-	00H
IP0	Interrupt priority level 0	A9H	-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00H
IP1	Interrupt priority level 1	B9H	-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00H

Mnemonic: IEN0 **Address: A8h**

7	6	5	4	3	2	1	0	Reset
EA	-	ET2	ES	ET1	EX1	ET0	EX0	00h

EA: EA=0 – Disable all interrupt.
EA=1 – Enable all interrupt.

ET2: ET2=0 – Disable Timer 2 overflow or external reload interrupt.
ET2=1 – Enable Timer 2 overflow or external reload interrupt.

ES: ES=0 – Disable Serial channel interrupt.
ES=1 – Enable Serial channel interrupt.

ET1: ET1=0 – Disable Timer 1 overflow interrupt.
ET1=1 – Enable Timer 1 overflow interrupt.

EX1: EX1=0 – Disable external interrupt 1.
EX1=1 – Enable external interrupt 1.

ET0: ET0=0 – Disable Timer 0 overflow interrupt.
ET0=1 – Enable Timer 0 overflow interrupt.

EX0: EX0=0 – Disable external interrupt 0.
EX0=1 – Enable external interrupt 0.

Mnemonic: IEN1 **Address: B8h**

7	6	5	4	3	2	1	0	Reset
EXEN2	-	IEIIC	IELVI	-	IEADC	IESPI	-	00H

EXEN2: Timer 2 reload interrupt enable.
EXEN2 = 0 – Disable Timer 2 external reload interrupt.
EXEN2 = 1 – Enable Timer 2 external reload interrupt.

IEIIC: IIC interrupt enable.
IEIICS = 0 – Disable IIC interrupt.

IEIICS = 1 – Enable IIC interrupt.

IELVI: LVI interrupt enable.

IELVI = 0 – Disable LVI interrupt.

IELVI = 1 – Enable LVI interrupt.

IEADC: A/D converter interrupt enable

IEADC = 0 – Disable ADC interrupt.

IEADC = 1 – Enable ADC interrupt.

IESPI: SPI interrupt enable.

IESPI = 0 – Disable SPI interrupt.

IESPI = 1 – Enable SPI interrupt.

Mnemonic: IEN2 **Address: 9Ah**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	EWDT	-	00H

EWDT: Enable Watch dog interrupt.

EWDT = 0 – Disable Watch dog interrupt.

EWDT = 1 – Enable Watch dog interrupt.

Mnemonic: IRCON **Address: C0h**

7	6	5	4	3	2	1	0	Reset
EXF2	TF2	IICIF	LVIIF	-	ADCIF	SPIIF	-	00H

EXF2: Timer 2 external reload flag. Must be cleared by software.

TF2: Timer 2 overflow flag. Must be cleared by software.

IICIF: IIC interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

LVIIF: LVI interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

ADCIF: A/D converter end interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

SPIIF: SPI interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

Mnemonic:IRCON2 **Address: 97h**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	WDTIF	-	00H

WDTIF: Watch dog interrupt flag. Hardware will clear this flag automatically when enter interrupt vector.

11.1 Priority level structure

All interrupt sources are combined in groups, As given in Table 11-2.

Table 11-2: Priority level groups

Groups		
External interrupt 0	-	PWM interrupt
Timer 0 interrupt	Watchdog interrupt	SPI interrupt
External interrupt 1	-	ADC interrupt
Timer 1 interrupt	-	-
Serial channel interrupt	-	LVI interrupt
Timer 2 interrupt	-	IIC interrupt

Each group of interrupt sources can be programmed individually to one of four priority levels by setting or clearing one bit in the special function register IP0 and one in IP1. If requests of the same priority level will be received simultaneously, an internal polling sequence determines which request is serviced first. As given in Table 11-3 and Table 11-4 and Table 11-5.

Mnemonic: IP0 **Address: A9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00h

Mnemonic: IP1 **Address: B9h**

7	6	5	4	3	2	1	0	Reset
-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00h

Table 11-3: Priority levels

IP1.x	**IP0.x**	**Priority Level**
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

Table 11-4: Groups of priority

Bit	**Group**		
IP1.0, IP0.0	External interrupt 0	-	PWM interrupt
IP1.1, IP0.1	Timer 0 interrupt	Watchdog interrupt	SPI interrupt
IP1.2, IP0.2	External interrupt 1	-	ADC interrupt
IP1.3, IP0.3	Timer 1 interrupt	-	-
IP1.4, IP0.4	Serial channel interrupt	-	LVI interrupt
IP1.5, IP0.5	Timer 2 interrupt	-	IIC interrupt

Table 11-5: Polling sequence

Interrupt source	**Sequence**
External interrupt 0	↓ Polling sequence
PWM interrupt	
Timer 0 interrupt	
Watchdog interrupt	
SPI interrupt	
External interrupt 1	
ADC interrupt	
Timer 1 interrupt	
Serial channel interrupt	
LVI interrupt	
Timer 2 interrupt	
IIC interrupt	

12. Power Management Unit

Power management unit serves two power management modes, IDLE and STOP, for the users to do power saving function.

Mnemonic: PCON **Address: 87h**

7	6	5	4	3	2	1	0	Reset
SMOD	MDUF	-	-	-	-	STOP	IDLE	40h

STOP: Stop mode control bit. Setting this bit turning on the Stop Mode.
Stop bit is always read as 0

IDLE: Idle mode control bit. Setting this bit turning on the Idle Mode.
Idle bit is always read as 0

12.1 Idle mode

Setting the IDLE bit of PCON register invokes the IDLE mode. The IDLE mode leaves internal clocks and peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any interrupts or a reset.

12.2 Stop mode

Setting the STOP bit of PCON register invokes the STOP mode. All internal clocking in this mode is turn off. The CPU will exit this state from a no-clocked interrupt (external INT0/1, LVI and Watchdog interrupt) or a reset (WDT and LVR) condition. Internally generated interrupts (timer, serial port ...) have no effect on stop mode since they require clocking activity.

13. Pulse Width Modulation (PWM)

PWM module features:

- Four-channel (tow-pair) PWM output pins.
- 14-bit resolution.

The interrupt vector is 43h.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
PWM											
PWMTBC0	PWM Time Base Control 0 Reg.	F9h	-	-	-	-	PWMTBPRE [1:0]		PWMTBMOD [1:0]		00H
PWMTBC1	PWM Time Base Control 1 Reg.	FAh	PWM TBEN	-	-	PWM ProtectDIS	-	-	-	PWMP IE	10H
PWMOP MOD	PWM Output Pair Mode Reg.	FBh	-	-	-	-	PWM OP3 MOD	PWMO P2 MOD	-	-	00H
PERIODL	PWM Period (Low) Reg.	F1h	PWM Period Low 8 bit								FFH
PERIODH	PWM Period (High) Reg.	F2h	-	-	PWM Period High 6 bit						3FH
PWMEN	PWM Output Enable Reg.	F5h	PWM7 EN	PWM6 EN	PWM5 EN	PWM4 EN	-	-	-	-	00H
PWMTB POST SCALE	PWM Time Base Post Scale Reg.	EEh	PWMTBPOST[7:0]								00H
PWMINTF	PWM INT Flag Reg.	BCh	PWM TBDIR	-	-	-	-	-	-	PWMP IF	00H
PWMPOLARITY	PWM Polarity Reg.	DDh	Polarity 7	Polarity 6	Polarity 5	Polarity 4	-	-	-	-	FFH
DUTY2L	PWM 2 Duty Low byte Reg.	D5h	PWM2 Duty Low 8 bit								00H
DUTY2H	PWM 2 Duty High byte Reg.	D6h	-	-	PWM2 Duty High 6 bit						00H
DUTY3L	PWM 3 Duty Low byte Reg.	D7h	PWM3 Duty Low 8 bit								00H
DUTY3H	PWM 3 Duty High byte Reg.	C9h	-	-	PWM3 Duty High 6 bit						00H

Mnemonic: PWMTBC0
(PWM Time Base Control 0)
Address: F9h

7	6	5	4	3	2	1	0	Reset
-	-	-	-	PWMTBPRE[1:0]		PWMTBMOD[1:0]		00H

PWMTBPRE[1:0]: PWM Time Base PreScale.

PWMTBPRE [1:0]	Mode
00	Fosc
01	Fosc/4
10	Fosc/16
11	Fosc/64

PWMTBMOD: PWM Time Base Mode.

PWMTBMOD [1:0] = 00 - Free Running mode (Edge-align).

PWMTBMOD [1:0] = 01 - Single-shot mode (Edge-align).

PWMTBMOD [1:0] = 10 - Continuous up/down counting mode (Center-align). (TBCOUNTER = PERIOD generate an interrupt)

PWMTBMOD [1:0] = 11 - Continuous up/down counting with interrupt for double PWM updates (Center-align). (TBCOUNTER = PERIOD and TBCOUNTER = 0 generate an interrupt)

Freq = 24MHz, Period = 14 bit		
Prescale	PWM Frequency Edge-align	PWM Frequency Center-align
1:1	1500 Hz	750 Hz
1:4	375 Hz	188 Hz
1:16	94 Hz	47 Hz
1:64	23 Hz	12 Hz

Mnemonic: PWMTBC1
(PWM Time Base Control 1)
Address: FAh

7	6	5	4	3	2	1	0	Reset
PWMTB EN	-	-	PWMPro tectDIS	-	-	-	PWMPIE	10H

PWMTBEN: PWM Time Base Enable

0 = PWM Time Base Disable.

1 = PWM Time Base Enable.

WMProtectDIS: PWM Protect Set (fool proof circuit)

0 = Enable. (Aaply to complementary mode)

1 = Disable.

PWM4/PWM5, PWM6/PWM7, Protect enable/disable.

PWMPIE: PWM Period Interrupt Enable

PWMPIE = 0 - PWM Period Interrupt Diable.

PWMPIE = 1 - PWM Period Interrupt Enable.

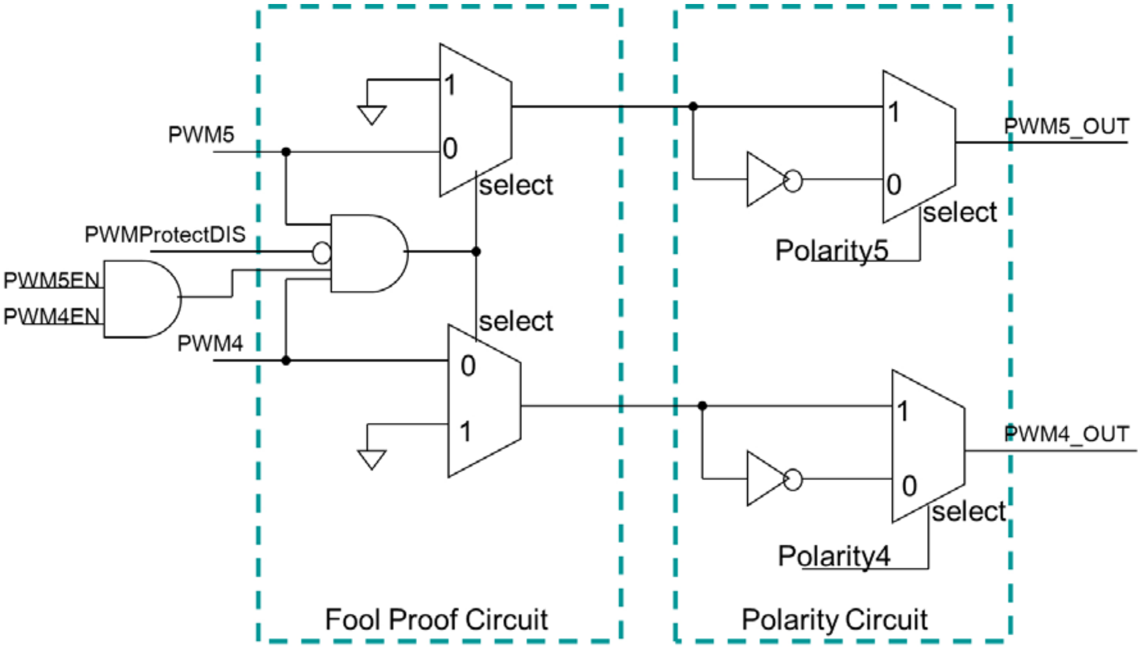

PWM5
PWMProtectDIS
PWM5EN
PWM4EN
PWM4
1
0
select
select
0
1
1
0
select
Polarity5
PWM5_OUT
1
0
select
Polarity4
PWM4_OUT
Fool Proof Circuit
Polarity Circuit

Fig. 13-1: Opertion of the PWM Protect Mode

Mnemonic: PWMOPMOD
(PWM Output Pair Mode)
Address: FBh

7	6	5	4	3	2	1	0	Reset
-	-	-	-	PWMOP3 MOD	PWMOP2 MOD	-	-	00H

PWMOP3MOD: PWM Output Pair 3 Mode.
0 = (PWM6, PWM7) is complementary mode.
1 = (PWM6, PWM7) is independent mode.
PWMOP2MOD: PWM Output Pair 2 Mode.
0 = (PWM4, PWM5) is complementary mode.
1 = (PWM4, PWM5) is independent mode.

Mnemonic: PWMEN
Address: F5h

7	6	5	4	3	2	1	0	Reset
PWM7EN	PWM6EN	PWM5EN	PWM4EN	-	-	-	-	00H

PWM7EN: PWM 7 Enable.
PWM7EN = 0 - PWM7 Output Disable.
PWM7EN = 1 - PWM7 Output Enable.
PWM6EN: PWM 6 Enable.
PWM6EN = 0 - PWM6 Output Disable.
PWM6EN = 1 - PWM6 Output Enable.
PWM5EN: PWM 5 Enable.

PWM5EN = 0 - PWM5 Output Disable.
PWM5EN = 1 - PWM5 Output Enable.

PWM4EN: PWM 4 Enable.
PWM4EN = 0 - PWM4 Output Disable.
PWM4EN = 1 - PWM4 Output Enable.

Mnemonic: PWMTBPOSTSCALE **Address: EEh**

7	6	5	4	3	2	1	0	Reset
PWMTBPOST [7:0]								00H

PWMTBPOST[7:0] PWM Time Base Post Scale. (How many PWM period happen will a triger need)
0000_0000 = 1: 1 Postscale
0000_0001 = 1: 2 Postscale
:
:
0000_1111 = 1: 16 Postscale
0001_0000 = 1: 17 Postscale
:
:
1111_1111 = 1: 256 Postscale

Mnemonic: PWMINTF
(PWM Interrupt Flag) **Address: BCh**

7	6	5	4	3	2	1	0	Reset
PWMTB DIR	-	-	-	-	-	-	PWMP IF	00H

PWMTBDIR: PWM Time Base Count Direction Status.(Read only)
0 = counts up.
1 = counts down.

PWMPIF: PWM Period Interrupt Flag. Must be cleared by software.

Mnemonic: PWMPOLARITY **Address: DDh**

7	6	5	4	3	2	1	0	Reset
POLARITY 7	POLARITY 6	POLARITY 5	POLARITY 4	-	-	-	-	FFH

POLARITY7: PWM Polarity 7
POLARITY7 = 0 - PWM7 Polarity active low.
POLARITY7 = 1 - PWM7 Polarity active high.

POLARITY6: PWM Polarity 6
POLARITY6 = 0 - PWM6 Polarity active low.

POLARITY6 = 1 - PWM6 Polarity active high.

POLARITY5: PWM Polarity 5

POLARITY5 = 0 - PWM5 Polarity active low.

POLARITY5 = 1 - PWM5 Polarity active high.

POLARITY4: PWM Polarity 4

POLARITY4 = 0 - PWM4 Polarity active low.

POLARITY4 = 1 - PWM4 Polarity active high.

14. IIC function

The IIC module uses the SCL (clock) and the SDA (data) line to communicate with external IIC interface. Its speed can be selected to 400Kbps (maximum) by software setting the IICBR [2:0] control bit. The IIC module provided 2 interrupts (RXIF, TXIF). It will generate START, repeated START and STOP signals automatically in master mode and can detects START, repeated START and STOP signals in slave mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

The interrupt vector is 6Bh.

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
IIC function											
IICCTL	IIC control register	F9h	IICEN	MSS	MAS	AB_EN	BF_EN	IICBR[2:0]			04H
IICS	IIC status register	F8h	-	MPIF	LAIF	RXIF	TXIF	RXAK	TXAK	RW or BB	00H
IICA1	IIC Address 1 register	FAh	IICA1[7:1]							MATCH1or RW1	A0H
IICA2	IIC Address 2 register	FBh	IICA2[7:1]							MATCH2 or RW2	60H
IICRWD	IIC Read/Write register	FCh	IICRWD[7:0]								00H
IICEBT	IIC Enaable Bus Transaction	FDh	FU_EN		-	-	-	-	-	-	00H

Mnemonic: IICCTL **Address: F9h**

7	6	5	4	3	2	1	0	Reset
IICEN	MSS	MAS	AB_EN	BF_EN	IICBR[2:0]			04h

IICEN: Enable IIC module

IICEN = 1 is Enable.

IICEN = 0 is Disable.

MSS: Master or slave mode select.

MSS = 1 is master mode.

MSS = 0 is slave mode.

*The software must set this bit before setting others register.

MAS: Master address select (master mode only)

MAS = 0 is to use IICA1.

MAS = 1 is to use IICA2.

AB_EN: Arbitration lost enable bit. (Master mode only)

If set AB_EN bit, the hardware will check arbitration lost. Once arbitration lost occurred, hardware will return to IDLE state. If this bit is cleared, hardware will not care arbitration lost condition. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

BF_EN: Bus busy enable bit. (Master mode only)

If set BF_EN bit, hardware will not generate a start condition to bus until BF=0. Clear this bit will always generate a start condition to bus when MStart is set. Set this bit when multi-master and slave connection. Clear this bit when single master to single slave.

IICBR[2:0]: Baud rate selection (master mode only), where Fosc is the external crystal or oscillator frequency. The default is Fosc/512 for users' convenience.

IICBR[2:0]	Baud rate
000	Fosc/32
001	Fosc/64
010	Fosc/128
011	Fosc/256
100	Fosc/512
101	Fosc/1024
110	Fosc/2048
111	Fosc/4096

Mnemonic: IICS **Address: F8H**

7	6	5	4	3	2	1	0	Reset
-	MPIF	LAIF	RXIF	TXIF	RXAK	TxAK	RW or BB	00H

MPIF: The Stop condition Interrupt Flag

The stop condition occurred and this bit will be set. Software need to clear this bit

LAIF: Arbitration lost bit. (Master mode only)

The Arbitration Interrupt Flag, the bus arbitration lost occurred and this bit will be set. Software need to clear this bit

RxIF: The data Receive Interrupt Flag (RXIF) is set after the IICRWD (IIC Read Write Data Buffer) is loaded with a newly receive data.

TxIF: The data Transmit Interrupt Flag (TXIF) is set when the data of the IICRWD (IIC Read Write Data Buffer) is downloaded to the shift register.

RxAK: The Acknowledge Status indicate bit. When clear, it means an acknowledge signal has been received after the complete 8 bits data Transmit on the bus.

TxAK: The Acknowledge status Transmit bit. When received complete 8 bits data, this bit will set (NoAck) or clear (Ack) and Transmit to master to indicate the receive status.

RW or BB: Master Mode:

BB : Bus busy bit
If detect scl=0 or sda=0 or bus start, this bit will be set. If detect stop,this bit will be cleared. This bit can be cleared by software to return ready state.

Slave Mode:
RW:The slave mode read (received) or wrote (Transmit) on the IIC bus. When this bit is clear, the slave module received data on the IIC bus (SDA).(Slave mode only).
As shown in Fig. 14-1

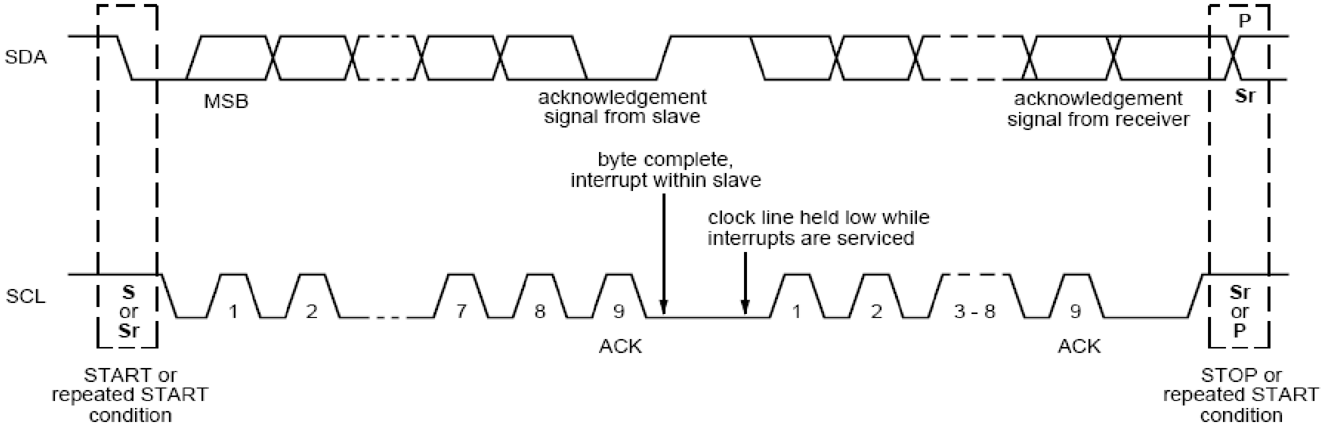

SDA
SCL
P
MSB
acknowledgement signal from slave
acknowledgement signal from receiver
Sr
byte complete, interrupt within slave
clock line held low while interrupts are serviced
S or Sr
1
2
7
8
9
ACK
1
2
3 - 8
9
ACK
Sr or P
START or repeated START condition
STOP or repeated START condition

Fig. 14-1: Acknowledgement bit in the 9th bit of a byte transmission

Mnemonic: IICA1 **Address: FA**

7	6	5	4	3	2	1	0	Reset
IICA1[7:1]							Match1 or RW1	A0H
R/W							R or R/W	

Slave mode:

IICA1[7:1]: IIC Address registers

This is the first 7-bit address for this slave module. It will be checked when an address (from master) is received

Match1: When IICA1 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.

Master mode:

IICA1[7:1]: IIC Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW1: This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It appears at the 8th bit after the IIC address as below figure. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master Transmit mode. As shown in Fig. 14-2

RW1=1, master receive mode

RW1=0, master Transmit mode

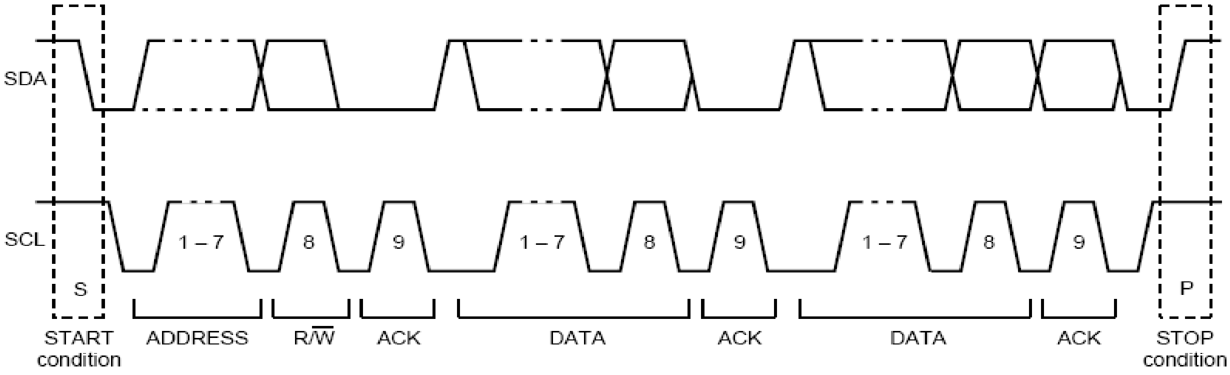

SDA
SCL
S
1 – 7
8
9
1 – 7
8
9
1 – 7
8
9
P
START condition
ADDRESS
R/$\overline{W}$
ACK
DATA
ACK
DATA
ACK
STOP condition

Fig. 14-2: RW bit in the 8th bit after IIC address

Mnemonic: IICA2 **Address: FB**

7	6	5	4	3	2	1	0	Reset
IICA2[7:1]							Match2 or RW2	60H
R/W							R or R/W	

Slave mode:

IICA2[7:1]: IIC Address registers

This is the second 7-bit address for this slave module.

It will be checked when an address (from master) is received

Match2: When IICA2 matches with the received address from the master side, this bit will set to 1 by hardware. When IIC bus gets first data, this bit will clear.

Master mode:

IICA2[7:1]: IIC Address registers

This 7-bit address indicates the slave with which it wants to communicate.

RW2: This bit will be sent out as RW of the slave side if the module has set the MStart or RStart bit. It is used to tell the salve the direction of the following communication. If it is 1, the module is in master receive mode. If 0, the module is in master Transmit mode.

RW2=1, master receive mode

RW2=0, master Transmit mode

Mnemonic: IICRWD **Address: FCh**

7	6	5	4	3	2	1	0	Reset
IICRWD[7:0]								00h

IICRWD[7:0]: IIC read write data buffer.

In receiving (read) mode, the received byte is stored here.

In Transmitting mode, the byte to be shifted out through SDA stays here.

Mnemonic: IICEBT **Address: FDH**

7	6	5	4	3	2	1	0	Reset
FU_EN		-	-	-	-	-	-	00H

Master Mode：

00: reserved

01: IIC bus module will enable read/write data transfer on SDA and SCL.

10: IIC bus module generate a start condition on the SDA/SCL, then send out address which is stored in the IICA1/IICA2(selected by MAS control bit)

11: IIC bus module generates a stop condition on the SDA/SCL.

FU_EN[7:6] will be auto-clear by hardware, so setting FU_EN[7:6] repeatedly is necessary.

Slave mode:

01: FU_EN[7:6] should be set as 01 only. The other value is inhibited.

Notice:

FU_EN[7:6] should be set as 01 before read/write data transfer for bus release; otherwise, SCL will be locked(pull low).

FU_EN[7:6] should be set as 01 after read/write data transfer for receiving a stop condition from bus master.

In Transmit data mode (slave mode), the output data should be filled into IICRWD before setting FU_EN[7:6] as 01.

FU_EN[7:6] will be auto-clear by hardware, so setting FU_EN[7:6] repeatedly is necessary.

15. SPI Function - Serial Peripheral Interface

Serial Peripheral Interface (SPI) is a synchronous protocol that allows a master device to initiate communication with slave devices.

The interrupt vector is 4Bh.

There are 4 signals used in SPI, they are
SPI_MOSI: data output in the master mode, data input in the slave mode,
SPI_MISO: data input in the master mode, data output in the slave mode,
SPI_SCK: clock output from the master, the above data are synchronous to this signal.
SPI_SS: input in the slave mode.

This slave device detects this signal to judge if it is selected by the master. As shown in Fig. 15-1

In the master mode, it can select the desired slave device by any IO with value = 0. As below figure is an example showing the relation of the 4 signals between master and slaves.

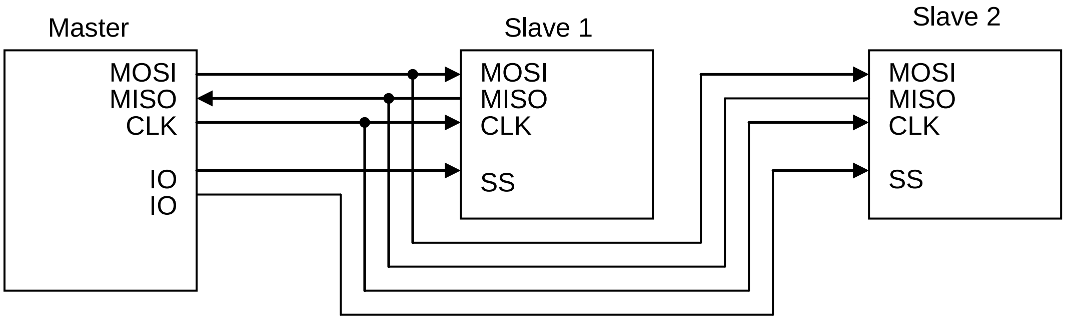


Fig. 15-1: SPI signals between master and slave devices

There is only one channel SPI interface. The SPI SFRs are shown as below:

Mnemonic	**Description**	**Dir.**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**RST**
SPI function											
SPIC1	SPI control register 1	F1h	SPIEN	SPIMSS	SPISSP	SPICKP	SPICKE	SPIBR[2:0]			08H
SPIC2	SPI control register 2	F2h	SPIFD	TBC[2:0]			SPIRST	RBC[2:0]			00H
SPIS	SPI status register	F5h	SPIRF	SPIMLS	SPIOV	SPITXIF	SPITDR	SPIRXIF	SPIRDR	SPIRS	40H
SPITXD	SPI Transmit data buffer	F3h	SPITXD[7:0]								00H
SPIRXD	SPI receive data buffer	F4h	SPIRXD[7:0]								00H

Mnemonic:SPIC1 **Address:F1H**

7	6	5	4	3	2	1	0	Reset
SPIEN	SPIMSS	SPISSP	SPICKP	SPICKE	SPIBR[2:0]			08H

SPIEN: Enable SPI module.

SPIEN = 1 - is Enable.

SPIEN = 0 - is Disable.

SPIMSS: Master or Slave mode Select

SPIMSS = 1 - is Master mode.

SPIMSS = 0 - is Slave mode.

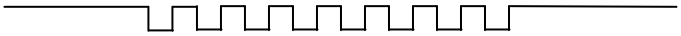
SPISSP: SS or CS active polarity.(Slave mode used only)

SPISSP = 1 - high active.

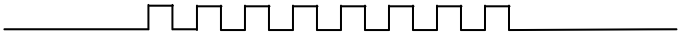
SPISSP = 0 - low active.

SPICKP: Clock idle polarity select.

SPICKP = 1 - SCK will idle high. Ex :



SPICKP = 0 - SCK will idle low. Ex :

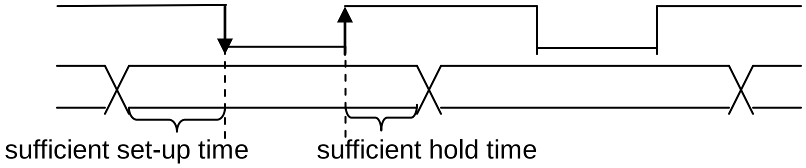


SPICKE: Clock sample edge select.

SPICKE = 1 - rising edge latch data.

SPICKE = 0 - falling edge latch data.

* To ensure the data latch stability, SM39R16A6 generate the output data As shown in the following example, the other side can latch the stable data no matter in rising or falling edge.



SPIBR[2:0]: SPI baud rate select. (Master mode used only)

SPIBR[2:0]	**Baud rate**
0:0:0	Fosc/4
0:0:1	Fosc /8
0:1:0	Fosc /16
0:1:1	Fosc /32
1:0:0	Fosc /64
1:0:1	Fosc /128
1:1:0	Fosc /256
1:1:1	Fosc /512

Mnemonic: SPIC2 **Address: F2H**

7	6	5	4	3	2	1	0	Reset
SPIFD	TBC[2:0]			SPIRST	RBC[2:0]			00H

SPIFD: Full-duplex mode enable.

SPIFD = 1 is enable full-duplex mode.

SPIFD = 0 is disable full-duplex mode.

When it is set, the TBC[2:0] and RBC[2:0] will be reset and keep to zero. When the Master device Transmits data to the Slave device via the MOSI line, the Slave device responds by sending data to the Master device via the MISO line. This implies full-duplex transmission with both data out and data in synchronized with the same clock. As shown in Fig 15-2.

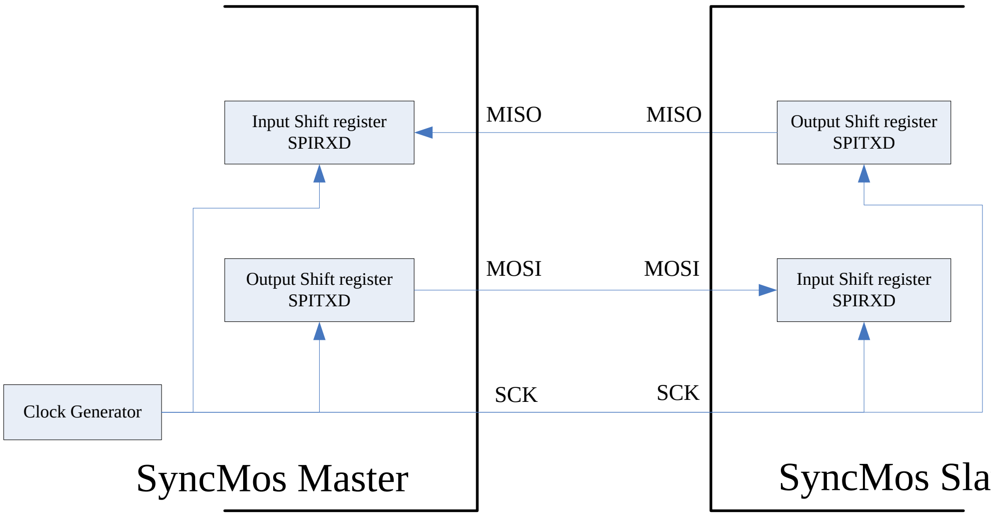

Input Shift register
SPIRXD
MISO
MISO
Output Shift register
SPITXD
Output Shift register
SPITXD
MOSI
MOSI
Input Shift register
SPIRXD
Clock Generator
SCK
SCK
SyncMos Master
SyncMos Slave

Fig. 15-2: SPI Mater and slave transfer method

SPIRST: SPI Re-start (Slave mode used only)

SPIRST = 0 - Re-start function disable.SPI Transmit/receive data when SS active.

In SPITXD/SPIRXD buffer, data got from previous SS active period will not be removed (i.e. it's valid).

SPIRST = 1 - Re-start function enable.SPI Transmit/receive new data when SS re-active;

In SPITXD/SPIRXD buffer, data got from previous SS active period will be removed (i.e. It's invalid).

TBC[2:0]: SPI Transmitter bit counter.

TBC[2:0]	Bit counter
0:0:0	8 bits output
0:0:1	1 bit output
0:1:0	2 bits output
0:1:1	3 bits output
1:0:0	4 bits output
1:0:1	5 bits output
1:1:0	6 bits output
1:1:1	7 bits output

RBC[2:0]: SPI receiver bit counter.

RBC[2:0]	Bit counter
0:0:0	8 bits input
0:0:1	1 bit input
0:1:0	2 bits input
0:1:1	3 bits input
1:0:0	4 bits input
1:0:1	5 bits input
1:1:0	6 bits input
1:1:1	7 bits input

Mnemonic: SPIS **Address:F5H**

7	6	5	4	3	2	1	0	Reset
SPIRF	SPIMLS	SPIOV	SPITXIF	SPITDR	SPIRXIF	SPIRDR	SPIRS	40H

SPIRF: SPI SS pin Release Flag.

This bit is set when SS pin release & SPIRST as ‘1’.

SPIMLS: MSB or LSB first output /input Select.

SPIMLS = 1 is MSB first output/input.

SPIMLS = 0 is LSB first output/input.

SPIOV: Overflow flag.

When SPIRDR is set and next data already into shift register, this flag will be set.

It is clear by hardware, when SPIRDR is cleared.

SPITXIF: Transmit Interrupt Flag.

This bit is set when the data of the SPITXD register is downloaded to the shift register.

SPITDR: Transmit Data Ready.

When MCU finish writing data to SPITXD register, the MCU needs to set this bit to ‘1’ to inform the SPI module to send the data. After SPI module finishes sending the data from SPITXD, this bit will be cleared automatically.

SPIRXIF: Receive Interrupt Flag.

This bit is set after the SPIRXD is loaded with a newly receive data.

SPIRDR: Receive Data Ready.

The MCU must clear this bit after it gets the data from SPIRXD register. The SPI module is able to write new data into SPIRXD only when this bit is cleared.

SPIRS: Receive Start.

This bit set to “1” to inform the SPI module to receive the data into SPIRXD register.

Mnemonic: SPITXD **Address: F3H**

7	6	5	4	3	2	1	0	Reset
SPITXD[7:0]								00H

SPITXD[7:0]: Transmit data buffer.

Mnemonic: SPIRXD **Address: F4H**

7	6	5	4	3	2	1	0	Reset
SPIRXD[7:0]								00H

SPIRXD[7:0]: Receive data buffer.

P.S. MISO pin must be float when SS or CS no-active in slave mode.

16. LVI & LVR – Low Voltage Interrupt and Low Voltage Reset

The interrupt vector 63h

Mnemonic	**Description**	**Dir.**	**Bit 7**	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**RST**
Watchdog Timer											
RSTS	Reset status register	A1h	-	LVRLP INTF	LVRLP F	PDRF	WDTF	SWRF	LVRF	PORF	00H
LVC	Low voltage control register	E6h	LVI_E N	LVRLPE	LVRE	LVIF	LVRLP INTE	-	LVIS[1:0]		20H

Mnemonic: RSTS **Address: A1h**

7	6	5	4	3	2	1	0	Reset
-	LVRLP INTF	LVRLPF	PDRF	WDTF	SWRF	LVRF	PORF	00H

LVRLPINTF: “Internal” Low voltage reset flag.

When MCU is reset by LVR_LP_INT, LVRLPINTF flag will be set to one by hardware. This flag clear by software.

LVRLPF: “External” Low voltage reset flag.

When MCU is reset by LVR(External Low Power), LVRLPF flag will be set to one by hardware. This flag clear by software.

PDRF: Pad reset flag.

When MCU is reset by reset pad, PDRF flag will be set to one by hardware. This flag clear by software.

LVRF: Low voltage reset flag.

When MCU is reset by LVR, LVRF flag will be set to one by hardware. This flag clear by software.

PORF: Power on reset flag.

When MCU is reset by POR, PORF flag will be set to one by hardware. This flag clear by software.

Mnemonic: LVC **Address: E6h**

7	6	5	4	3	2	1	0	Reset
LVI_EN	LVR LPE	LVRE	LVIF	LVRLP INTE	-	LVIS[1:0]		20H

LVI_EN: Low voltage interrupt function enable bit.

LVI_EN = 0 - disable low voltage detect function.

LVI_EN = 1 - enable low voltage detect function.

LVRLPE: External low voltage reset function (Low Power)enable bit.

LVRLPE = 0 - enable external low voltage reset(Low Power) function.

LVRLPE = 1 - disable external low voltage reset(Low Power) function.

LVRE: External low voltage reset function enable bit.

LVRXE = 0 - disable external low voltage reset function.

LVRXE = 1 - enable external low voltage reset function.

Note: LVR = 1.50 V

LVIF:	Low Voltage interrupt Flag(i.e., Low Voltage Interrupt Status Flag)
LVRLPINTE:	LVR_LP_INT(“Internal” low voltage reset) function enable bit. LVRLPINTE = 0 - disable internal low voltage reset function. LVRLPINTE = 1 - enable internal low voltage reset function.
LVIS[1:0]:	LVI level select: 00: 1.65V 01: 2.60V 10: 3.20V 11: 4.00V

17. 10-bit Analog-to-Digital Converter (ADC)

The SM39R16A6 provides 8 channels 10-bit ADC. The Digital output DATA [9:0] were put into ADCD [9:0]. The ADC the block diagram show in Fig. 17-1

The ADC interrupt vector is 53H.

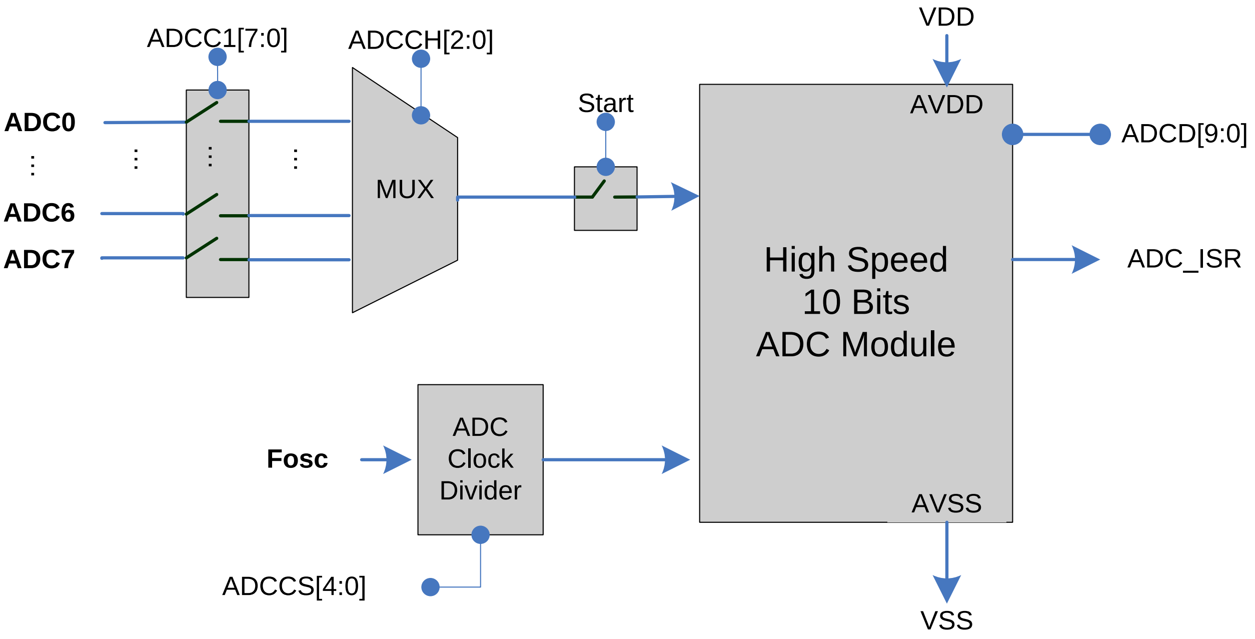

ADCC1[7:0]
ADCCH[2:0]
VDD
Start
AVDD
ADCD[9:0]
ADC0
ADC6
ADC7
MUX
High Speed
10 Bits
ADC Module
ADC_ISR
Fosc
ADC
Clock
Divider
AVSS
ADCCS[4:0]
VSS

Fig. 17-1: ADC Analog to Digital converter operation set

The ADC SFR show as below:

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
ADC											
ADCC1	ADC Control register 1	ABh	ADC7 EN	ADC6 EN	ADC5 EN	ADC4 EN	ADC3 EN	ADC2 EN	ADC1 EN	ADC0 EN	00H
ADCC2	ADC Control register 2	ACh	Start	ADJU ST	-	EXT Trigger EN	ADCM ODE	ADCCH[2:0]			08H
ADCDH	ADC data high byte	ADh	ADCDH [7:0]								00H
ADCDL	ADC data low byte	AEh	ADCDL [7:0]								00H
ADCCS	ADC clock select	AFh	-	-	-	ADCCS[4:0]					00H

Mnemonic: ADCC1 **Address: ABh**

7	6	5	4	3	2	1	0	Reset
ADC7EN	ADC6EN	ADC5EN	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	00H

ADC7EN: ADC channels 7 enable.

ADC7EN = 1 - Enable ADC channel 7

ADC6EN: ADC channels 6 enable.

ADC6EN = 1 - Enable ADC channel 6

ADC5EN: ADC channels 5 enable.

ADC5EN = 1 - Enable ADC channel 5

ADC4EN: ADC channels 4 enable.

ADC4EN = 1 - Enable ADC channel 4

ADC3EN: ADC channels 3 enable.

ADC3EN = 1 - Enable ADC channel 3

ADC2EN: ADC channels 2 enable.

ADC2EN = 1 - Enable ADC channel 2

ADC1EN: ADC channels 1 enable.

ADC1EN = 1 - Enable ADC channel 1

ADC0EN: ADC channels 0 enable.

ADC0EN = 1 - Enable ADC channel 0

Mnemonic: ADCC2 **Address: ACh**

7	6	5	4	3	2	1	0	Reset
Start	ADJUST	-	EXTTriggerEN	ADCMODE	ADCCH[2:0]			08H

Start: When this bit is set, the ADC will be start conversion.

(SW trigger conversion)

ADJUST: Adjust the format of ADC conversion DATA.

ADJUST = 0 - (default value)

ADC data high byte ADCD [9:2] = ADCDH [7:0].

ADC data low byte ADCD [1:0] = ADCDL [1:0].

ADJUST = 1- ADC data high byte ADCD [9:8] = ADCDH [1:0].

ADC data low byte ADCD [7:0] = ADCDL [7:0].

EXTTriggerEN: External Pin trigger ADC to start conversion.

(HW external trigger conversion)

0 = disable.

1 = enable.

ADCMODE: 0 = continuous mode.

1 = single-shot mode.

ADCCH[2:0] ADC channel select.

ADCCH [2:0]	Channel
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

ADJUST = 0:

Mnemonic: ADCDH **Address: ADh**

7	6	5	4	3	2	1	0	Reset
ADCD[9]	ADCD[8]	ADCD[7]	ADCD[6]	ADCD[5]	ADCD[4]	ADCD[3]	ADCD[2]	00H

Mnemonic: ADCDL **Address: AEh**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	ADCD[1]	ADCD[0]	00H

ADJUST = 1:

Mnemonic: ADCDH **Address: ADh**

7	6	5	4	3	2	1	0	Reset
-	-	-	-	-	-	ADCD[9]	ADCD[8]	00H

Mnemonic: ADCDL **Address: AEh**

7	6	5	4	3	2	1	0	Reset
ADCD[7]	ADCD[6]	ADCD[5]	ADCD[4]	ADCD[3]	ADCD[2]	ADCD[1]	ADCD[0]	00H

ADCD[9:0]: ADC data register.

Mnemonic: ADCCS **Address: AFh**

7	6	5	4	3	2	1	0	Reset
-	-	-	ADCCS[4]	ADCCS[3]	ADCCS[2]	ADCCS[1]	ADCCS[0]	00H

ADCCS[4:0]: ADC clock select.

*The ADC clock maximum 12.5MHz.

*The ADC Conversion rate maximum 961 KHz.

ADCCS[4:0]	ADC Clock(Hz)	Clocks for ADC Conversion
00000	Fosc /2	26
00001	Fosc /4	52
00010	Fosc /6	78
00011	Fosc /8	104
00100	Fosc /10	130
00101	Fosc /12	156
00110	Fosc /14	182
00111	Fosc /16	208
01000	Fosc /18	234
01001	Fosc /20	260

01010	Fosc /22	286
01011	Fosc /24	312
01100	Fosc /26	338
01101	Fosc /28	364
01110	Fosc /30	390
01111	Fosc /32	416
10000	Fosc /34	442
10001	Fosc /36	468
10010	Fosc /38	494
10011	Fosc /40	520
10100	Fosc /42	546
10101	Fosc /44	572
10110	Fosc /46	598
10111	Fosc /48	624
11000	Fosc /50	650
11001	Fosc /52	676
11010	Fosc /54	702
11011	Fosc /56	728
11100	Fosc /58	754
11101	Fosc /60	780
11110	Fosc /62	806
11111	Fosc /64	832

$$ADC\_Clock = \frac{\mathrm{Fosc}}{2 \times (ADCCS + 1)}$$

$$ADC\_Conversion\_Rate = \frac{\mathrm{ADC\_Clock}}{13}$$

18. In-System Programming (Internal ISP)

The SM39R16A6 can generate flash control signal by internal hardware circuit. Users utilize flash control register, flash address register and flash data register to perform the ISP function without removing the SM39R16A6 from the system. The SM39R16A6 provides internal flash control signals which can do flash program/chip erase/page erase/protect functions. User need to design and use any kind of interface which SM39R16A6 can input data. User then utilize ISP service program to perform the flash program/chip erase/page erase/protect functions.

18.1 ISP service program

The ISP service program is a user developed firmware program which resides in the ISP service program space. After user developed the ISP service program, user then determine the size of the ISP service program. User need to program the ISP service program in the SM39R16A6 for the ISP purpose.

The ISP service programs were developed by user so that it should includes any features which relates to the flash memory programming function as well as communication protocol between SM39R16A6 and host device which output data to the SM39R16A6. For example, if user utilize UART interface to receive/Transmit data between SM39R16A6 and host device, the ISP service program should include baud rate, checksum or parity check or any error-checking mechanism to avoid data transmission error.

The ISP service program can be initiated under SM39R16A6 active or idle mode. It can not be initiated under power down mode.

18.2 Lock Bit (N)

The Lock Bit N has two functions: one is for service program size configuration and the other is to lock the ISP service program space from flash erase function.

The ISP service program space address range $3C00 to $3FFF. It can be divided as blocks of N*128 byte. (N=0 to 8). When N=0 means no ISP function, all of 16K byte flash memory can be used as program memory. When N=1 means ISP service program occupies 128 byte while the rest of 15.875K byte flash memory can be used as program memory. The maximum ISP service program allowed is 1K byte when N=8. Under such configuration, the usable program memory space is 15K byte.

After N determined, SM39R16A6 will reserve the ISP service program space downward from the top of the program address $3FFF. The start address of the ISP service program located at $3x00 while x is depending on the lock bit N. Please see section 3.1 program memory diagram for this ISP service program space structure.

The lock bit N function is different from the flash protect function. The flash erase function can erase all of the flash memory except for the locked ISP service program space. If the flash not has been protected, the content of ISP service program still can be read. If the flash has been protected, the overall content of flash program memory space including ISP service program space can not be read. As given in Table 18-1.

Table 18-1 ISP code area

	ISP service program address
0	No ISP service program
1	128 bytes ($3F80h ~ $3FFFh)
2	256 bytes ($3F00h ~ $3FFFh)
3	384 bytes ($3E80h ~ $3FFFh)
4	512 bytes ($3E00h ~ $3FFFh)
5	640 bytes ($3D80h ~ $3FFFh)
6	768 bytes ($3D00h ~ $3FFFh)
7	896 bytes ($3C80h ~ $3FFFh)
8	1.0 K bytes ($3C00h ~ $3FFFh)

ISP service program configurable in N*128 byte (N= 0 ~ 8)

18.3 Program the ISP Service Program

After Lock Bit N is set and ISP service program been programmed, the ISP service program memory will be protected (locked) automatically. The lock bit N has its own program/erase timing. It is different from the flash memory program/erase timing so the locked ISP service program can not be erased by flash erase function. If user needs to erase the locked ISP service program, he can do it by writer only. User can not change ISP service program when SM39R16A6 was in system.

18.4 Initiate ISP Service Program

To initiate the ISP service program is to load the program counter (PC) with start address of ISP service program and execute it. There are four ways to do so:

(1) Blank reset. Hardware reset with first flash address blank ($0000=#FFH) will load the PC with start address of ISP service program. The hardware reset includes MAX810 (power on reset) and external pad reset. The hardware will issue a strobe window about 256us after hardware reset.

(2) Execute jump instruction can load the start address of the ISP service program to PC.

(3) Enter's ISP service program by hardware setting. User can force SM39R16A6 enter ISP service program by setting P1.2, P1.3 "active low" or P1.4 " active low" during hardware reset period. The hardware reset includes MAX810 (power on reset) and external pad reset. The hardware will issue after hardware reset. In application system design, user should take care of the setting of P1.2,P1.3 or P1.4 at reset period to prevent SM39R16A6 from entering ISP service program.

(4) Enter's ISP service program by hardware setting, the P3.0(RXD) will be detected the two clock signals during hardware reset period. The hardware reset includes MAX810 (power on reset) and external pad reset. The hardware will issue to detect 2 clock signals after hardware reset.

During the strobe window, the hardware will detect the status of P1.2, P1.3 (or P1.4)/P1.0. If they meet one of above conditions, chip will switch to ISP mode automatically. After ISP service program executed, user need to reset the SM39R16A6, either by hardware reset or by WDT, or jump to the address $0000 to re-start the firmware program.

There are 6 kinds of entry mechanisms for user different applications. This entry method will select on the writer or ISP.

(1) First Address Blank. i.e. $0000 = 0xFF. And triggered by Internal reset signal. (Entry mechanism 1)
(2) First Address Blank. i.e. $0000 = 0xFF. And triggered by PAD reset signal. (Entry mechanism 1)
(3) P1.2 = 0 & P1.3 = 0. And triggered by Internal reset signal. (Entry mechanism 2)
(4) P1.2 = 0 & P1.3 = 0. And triggered by PAD reset signal. (Entry mechanism 2)
(5) P1.4 = 0. And triggered by Internal reset signal. (Entry mechanism 3)
(6) P1.4 = 0. And triggered by PAD reset signal. (Entry mechanism 3)
(7) P3.0 input 2 clocks. And triggered by Internal reset signal. (Entry mechanism 4)
(8) P3.0 input 2 clocks. And triggered by PAD reset signal. (Entry mechanism 4)

18.5 ISP register – TAKEY, IFCON, ISPFAH, ISPFAL, ISPFD and ISPFC

Mnemonic	Description	Dir.	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RST
ISP function											
TAKEY	Time Access Key register	F7h	TAKEY [7:0]								00H
IFCON	Interface Control register	8Fh	-	CDPR	-	-	-	-	-	ISPE	00H
ISPFAH	ISP Flash Address – High register	E1h	ISPFAH [7:0]								FFH
ISPFAL	ISP Flash Address - Low register	E2h	ISPFAL [7:0]								FFH
ISPFD	ISP Flash Data register	E3h	ISPFD [7:0]								FFH
ISPFC	ISP Flash Control register	E4h	EMF1	EMF2	EMF3	EMF4	-	ISPF.2	ISPF.1	ISPF.0	00H

Mnemonic: TAKEY **Address: F7H**

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

ISP enable bit (ISPE) is read-only by default, software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register to enable the ISPE bit write attribute. That is:

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah
```

Mnemonic: IFCON **Address: 8FH**

7	6	5	4	3	2	1	0	Reset
-	CDPR	-	-	-	-	-	ISPE	00H

The bit 0 (ISPE) of IFCON is ISP enable bit. User can enable overall SM39R16A6 ISP function by setting ISPE bit to 1, to disable overall ISP function by set ISPE to 0. The function of ISPE behaves like a security key. User can disable overall ISP function to prevent software program be erased accidentally. ISP registers ISPFAH, ISPFAL, ISPFD and ISPFC are read-only by default. Software must be set ISPE bit to 1 to enable these 4 registers write attribute.

Mnemonic: ISPFAH **Address: E1H**

7	6	5	4	3	2	1	0	Reset
ISPFAH7	ISPFAH6	ISPFAH5	ISPFAH4	ISPFAH3	ISPFAH2	ISPFAH1	ISPFAH0	FFH

ISPFAH [7:0]: Flash address-high for ISP function

Mnemonic: ISPFAL **Address: E2H**

7	6	5	4	3	2	1	0	Reset
ISPFAL7	ISPFAL6	ISPFAL5	ISPFAL4	ISPFAL3	ISPFAL2	ISPFAL1	ISPFAL0	FFH

ISPFAL [7:0]: Flash address-Low for ISP function

The ISPFAH & ISPFAL provide the 16-bit flash memory address for ISP function. The flash memory address should not include the ISP service program space address. If the flash memory address indicated by ISPFAH & ISPFAL registers overlay with the ISP service program space address, the flash program/page erase of ISP function executed thereafter will have no effect.

Mnemonic: ISPFD **Address: E3H**

7	6	5	4	3	2	1	0	Reset
ISPFD7	ISPFD6	ISPFD5	ISPFD4	ISPFD3	ISPFD2	ISPFD1	ISPFD0	FFH

ISPFD [7:0]: Flash data for ISP function.

The ISPFD provide the 8-bit data register for ISP function.

Mnemonic: ISPFC **Address: E4H**

7	6	5	4	3	2	1	0	Reset
EMF1	EMF2	EMF3	EMF4	-	ISPF[2]	ISPF[1]	ISPF[0]	00H

EMF1: Entry mechanism (1) flag, clear by reset. (Read only)

EMF2: Entry mechanism (2) flag, clear by reset. (Read only)

EMF3: Entry mechanism (3) flag, clear by reset. (Read only)

EMF4: Entry mechanism (4) flag, clear by reset. (Read only)

ISPF [2:0]: ISP function select bit.

ISPF[2:0]	ISP function
000	Byte program
001	Chip protect
010	Page erase
011	Chip erase
100	Write option
101	Read option
110	Erase option
111	reserved

One page of flash memory is 128byte

The Option function can access the XTAL1 and XTAL2 swap to I/O pins select(description in section 1.2)、Internal reset time select(description in section

1.4.1)、clock source select(description in section 1.5)、Reset swap to I/O pins function select(description in section 5)、WDTEN control bit(description in section 10)、or ISP entry mechanisms select(description in section 18).

When chip protected or no ISP service, option can only read.

The choice ISP function will start to execute once the software write data to ISPFC register.

To perform byte program/page erases ISP function, user need to specify flash address at first. When performing page erase function, SM39R16A6 will erase entire page which flash address indicated by ISPFAH & ISPFAL registers located within the page.

e.g. flash address: $ XY00

page erase function will erase from $XY00 to $XY7F

To perform the chip erase ISP function, SM39R16A6 will erase all the flash program memory except the ISP service program space. To perform chip protect ISP function, the SM39R16A6 flash memory content will be read #00H.

e.g. ISP service program to do the byte program - to program #22H to the address $1005H

```
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah    ; enable ISPE write attribute
ORL IFCON, #01H    ; enable SM39R16A6 ISP function
MOV ISPFAH, #10H   ; set flash address-high, 10H
MOV ISPFAL, #05H    ; set flash address-low, 05H
MOV ISPFD, #22H    ; set flash data to be programmed, data = 22H
MOV ISPFC, #00H    ; start to program #22H to the flash address $1005H
MOV TAKEY, #55h
MOV TAKEY, #0AAh
MOV TAKEY, #5Ah     ; enable ISPE write attribute
ANL IFCON, #0FEH    ; disable SM39R16A6 ISP function
```

Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VDD	Supply voltage	1.8		5.5	V	
Vref	Internal reference voltage	1.1	1.2	1.3	V	

DC Characteristics

TA = -40℃ to 85℃, VCC = 5.0V

Symbol	Parameter	Valid	Min	Typical	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0,1,2,3	-0.5	-	0.8	V	Vcc=5V
VIL2	Input Low-voltage	RES, XTAL1	0	-	0.8	V	-
VIH1	Input High-voltage	Port 0,1,2,3	2.0	-	VCC + 0.5	V	-
VIH2	Input High-voltage	RES, XTAL1	70%Vcc	-	VCC + 0.5	V	-
VOL	Output Low-voltage	Port 0 (3.)	-	-	0.45	V	IOL=40mA Vcc=5V
		Port 1,2,3 (4.)	-	-	0.45	V	IOL=20mA Vcc=5V
VOH1	Output High-voltage using Strong Pull-up(1)	Port 0	4.6	-	-	V	IOH= -12mA
		Port 1,2,3	4.6	-	-	V	IOH= -7mA
VOH2	Output High-voltage using Weak Pull-up(2)	Port 0,1,2,3	2.6	-	-	V	IOH= -350uA
IIL	Logic 0 Input Current	Port 0,1,2,3	-	-	-75	uA	Vin= 0.45V
ITL	Logical Transition Current	Port 0,1,2,3	-	-	-650	uA	Vin= 2.0V
ILI	Input Leakage Current	Port 0,1,2,3	-	-	±10	uA	0.45V<Vin<Vcc
RRST	Reset Pull-down Resistor	RES	50	-	300	kΩ	-
CIO	Pin Capacitance	-	-	-	10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	VDD	-	3.19	4.78	mA	Active mode ,IRC=22.1184MHz
			-	5.5	8.25	mA	Active mode, 12MHz VCC=5V 25 ℃
			-	4.5	7.25	mA	Idle mode, 12MHz VCC =5V 25 ℃
			-	3	7	uA	Power down mode VCC =5V 25 ℃

Notes:

(1) Port in Push-Pull Output Mode
(2) Port in Quasi-Bidirectional Mode
(3) Maximum IOL per port0 pin : 40mA
(4) Maximum IOL per port1,2,3 pin : 20mA

TA = -40℃ to 85℃, VCC = 3.0V

Symbol	Parameter	Valid	Min	Typical	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0,1,2,3	-0.5	-	0.8	V	Vcc=3.0V
VIL2	Input Low-voltage	RES, XTAL1	0	-	0.8	V	-
VIH1	Input High-voltage	Port 0,1,2,3	2.0	-	VCC + 0.5	V	-
VIH2	Input High-voltage	RES, XTAL1	70%Vcc	-	VCC + 0.5	V	-
VOL	Output Low-voltage	Port 0 (3.)	-	-	0.45	V	IOL=20mA Vcc=3V
		Port 1,2,3 (4.)	-	-	0.45	V	IOL=12mA Vcc=3V
VOH1	Output High-voltage using Strong Pull-up(1)	Port 0	2.6	-	-	V	IOH=- 9mA
		Port 1,2,3	2.6	-	-	V	IOH= -5mA
VOH2	Output High-voltage using Weak Pull-up(2)	Port 0,1,2,3	2.4	-	-	V	IOH= -70uA
IIL	Logic 0 Input Current	Port 0,1,2,3	-	-	-75	uA	Vin= 0.45V
ITL	Logical Transition Current	Port 0,1,2,3	-	-	-650	uA	Vin=1.5V
ILI	Input Leakage Current	Port 0,1,2,3	-	-	±10	uA	0.45V<Vin<Vcc
RRST	Reset Pull-down Resistor	RES	50	-	300	kΩ	-
CIO	Pin Capacitance		-	-	10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	VDD	-	3.15	4.73	mA	Active mode ,IRC=22.1184MHz
			-	2.77	4.16	mA	Active mode ,12MHz VCC = 3.0 V 25 ℃
			-	1.77	3.16	mA	Idle mode, 12MHz VCC =3.0V 25 ℃
			-	1	5	uA	Power down mode VCC=3.0V 25 ℃

Notes:
(1) Port in Push-Pull Output Mode
(2) Port in Quasi-Bidirectional Mode
(3) Maximum IOL per port0 pin : 20mA
(4) Maximum IOL per port1,2,3 pin : 12mA

Absolute Maximum Ratings

SYMBOL	PARAMETER	MAX	UNIT
Maximum sourced current	An I/O pin	N/A	mA
	Total I/O pins	150	mA
Maximum sink current	An I/O pin	N/A	mA
	Total I/O pins	150	mA
Tj	Max. Junction Temperature	150	℃

LVI& LVR Characteristics

	LVR		
	Min	**Typical**	**Max**
1.8V ~ 5.5V	VIL=1.42V (VIH=1.62V)	VIL=1.50V (VIH=1.70V)	VIL=1.57V (VIH=1.77V)

	LVI		
	Min	**Typical**	**Max**
LVIS[1:0] = 00	VIL=1.57V (VIH=1.77V)	VIL=1.65V (VIH=1.85V)	VIL=1.73V (VIH=1.93V)
LVIS[1:0] = 01	VIL=2.47V (VIH=2.67V)	VIL=2.60V (VIH=2.80V)	VIL=2.73V (VIH=2.93V)
LVIS[1:0] = 10	VIL=3.04V (VIH=3.24V)	VIL=3.20V (VIH=3.40V)	VIL=3.36V (VIH=3.56V)
LVIS[1:0] = 11	VIL=3.80V (VIH=4.00V)	VIL=4.00V (VIH=4.20V)	VIL=4.20V (VIH=4.40V)