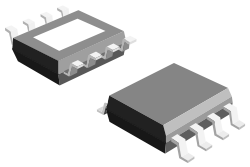
DDR Termination Regulator TJ2998

FEATURES

- Source and Sink Current
- Low Output Voltage Offset
- No External Resistors required
- Linear Topology
- Suspend to RAM (STR) functionality
- Low External Component Count
- Thermal Shutdown
- Under Voltage Lockout and Over Current Limit
- Available in SOP8, SOP8-PP Packages

SOP8 / SOP8-PP PKG



APPLICATIONS

- DDR 2/3/3L/4 Termination Voltage
- SSTL Termination
- HSTL Termination

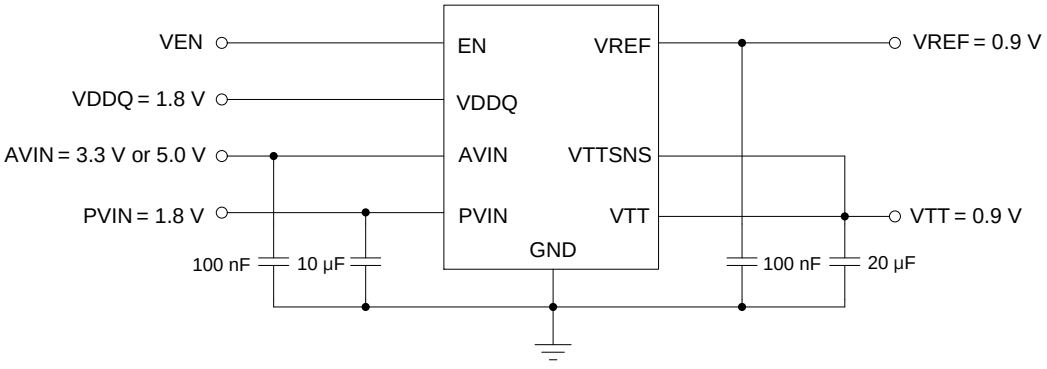
ORDERING INFORMATION

Device	Package
TJ2998GD	SOP8
TJ2998GDP	SOP8-PP

DESCRIPTION

The TJ2998 linear regulator is designed to meet the JEDEC SSTL specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering up to 2A continuous current and transient peaks up to 3A with respect to PVIN operating condition in the application as required for DDR-SDRAM termination. The TJ2998 also incorporates a VTTSNS pin to provide superior load regulation and a VREF output as a reference for the chipset and DIMMs. An additional feature found on the TJ2998 is an active high enable (EN) pin that provides Suspend To RAM (STR) functionality. When EN is pulled low the VTT output will tri-state providing a high impedance output, but, VREF will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Analog Bias Input Voltage (Survival)	AV_{IN}	-0.3	6.0	V
Power Input Voltage (Survival)	PV_{IN}	-0.3	6.0	V
Enable Input Voltage (Survival)	V_{EN}	-0.3	AV_{IN} + 0.3	V
VDDQ Input Voltage (Survival)	V_{DDQ}	-0.3	6.0	V
Lead Temperature (Soldering, 10 sec)	T_{SOL}		260	℃
Storage Temperature Range	T_{STG}	-65	150	℃
Operating Junction Temperature Range	T_{JOPR}	-40	125	℃

RECOMMENDED OPERATION RANGE

CHARACTERISTIC	SYMBOL	MIN.	MAX.	UNIT
Analog Bias Input Voltage	AV_{IN}	3.0	5.5	V
Power Input Voltage	PV_{IN}	0	2.0	V
Enable Input Voltage	V_{EN}	0	AV_{IN}	V
VDDQ Input Voltage	V_{DDQ}	0.5	1.8	V
Operating Temperature Range	T_{OPR}	-40	85	℃

THERMAL INFORMATION

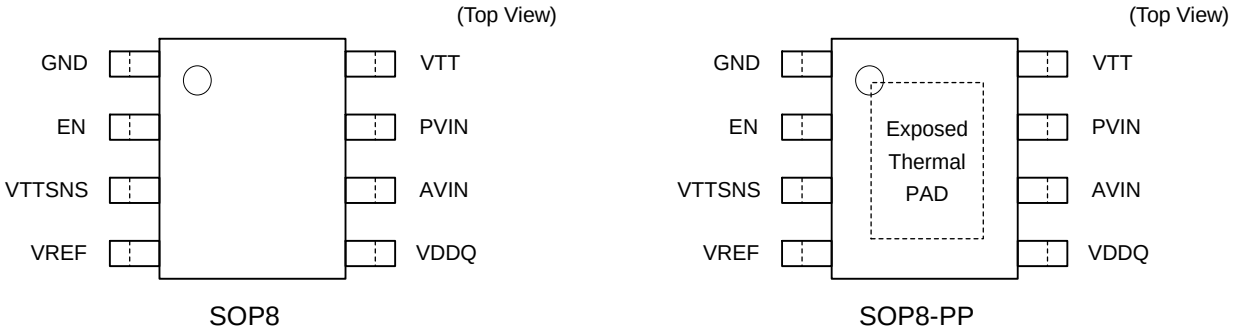
THERMAL METRIC	θ_{JA}	UNIT
Thermal Resistance (SOP8) *	130	ºC/W
Thermal Resistance (SOP8-PP) *	68	ºC/W

* Calculated from package in still air, mounted to minimum foot print PCB (1 oz., 2-layer).

ORDERING INFORMATION

Package	Order No.	Description	Package Marking	Supplied As
SOP8	TJ2998GD	DDR Termination Regulator	TJ2998G	Reel
SOP8-PP	TJ2998GDP	DDR Termination Regulator	TJ2998G	Reel

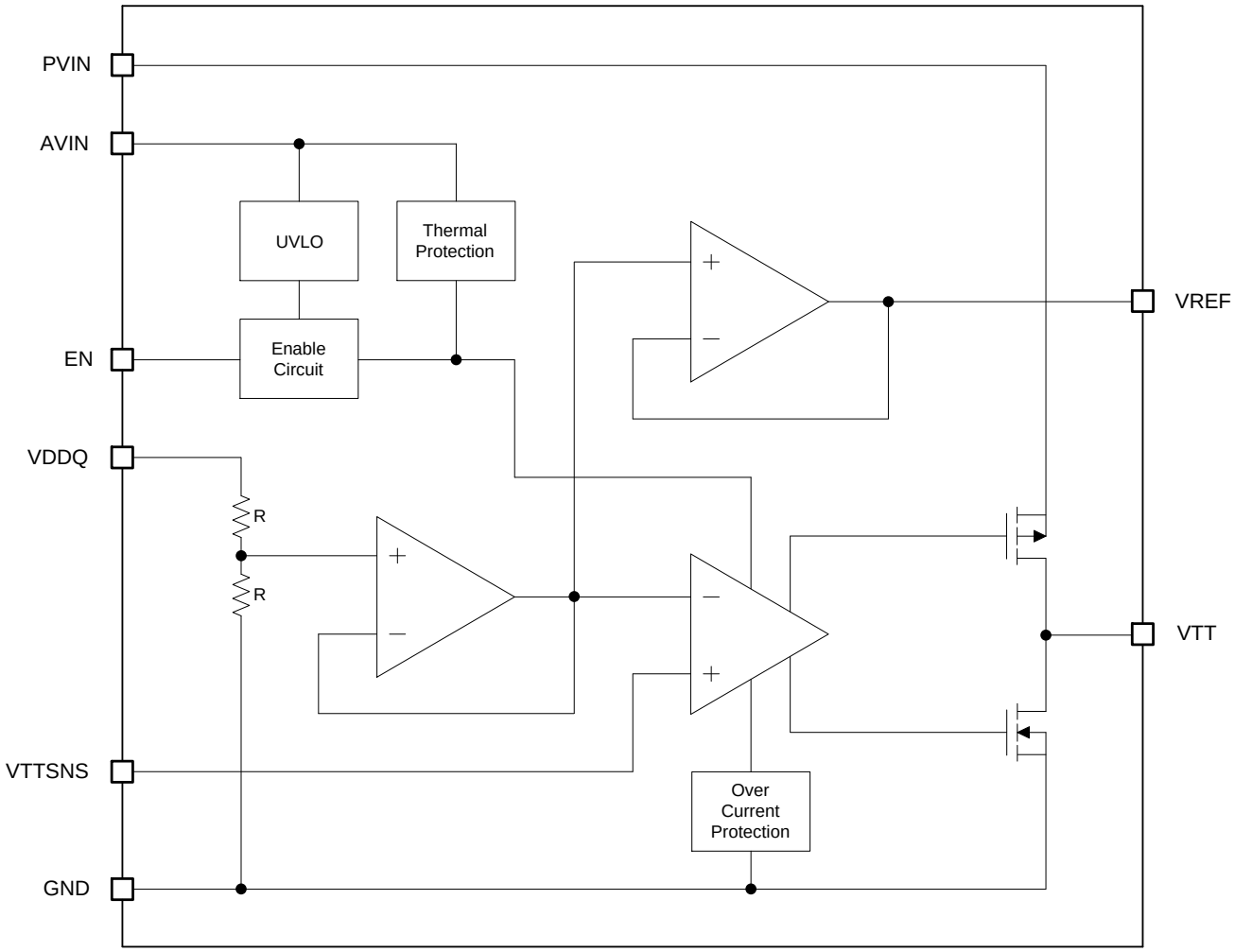
PIN CONFIGURATION



PIN DESCRIPTION

Pin No.		Pin Name	Pin Function
SOP8	SOP8-PP		
1	1	GND	Ground.
2	2	EN	Enable.
3	3	VTTSNS	Feedback Pin for Regulating $V_{TT.}$
4	4	VREF	Buffered Internal Reference Voltage of $V_{DDQ}/2$.
5	5	VDDQ	Input for Internal Reference Equal to $V_{DDQ}/2$.
6	6	AVIN	Analog Bias Input Pin.
7	7	PVIN	Power Input Pin.
8	8	VTT	Output Voltage for Connection to Termination Resistors.
-	PAD	Exposed Thermal PAD	Connect to Ground. (SOP8-PP Only)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

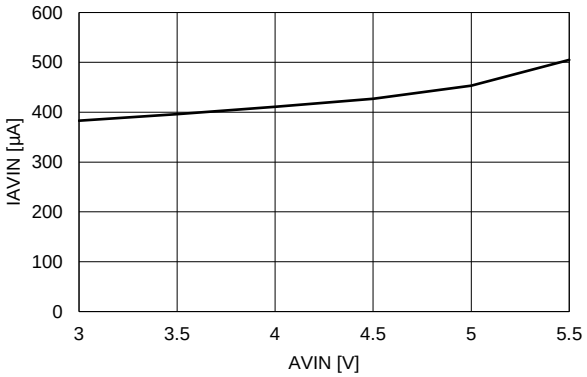
Specifications with standard typeface are for T_J=25˚C. Unless otherwise specified, AVIN=VEN=5.0V, PVIN=VDDQ=1.8V.

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{REF} Voltage	V_{REF}	PVIN = VDDQ = 1.8 V I_{VREF} = 0 A I_{VREF} = ± 10 mA (1)	 0.882 0.882	 0.900 0.900	 0.918 0.918	V
		PVIN = VDDQ = 1.5 V I_{VREF} = 0 A I_{VREF} = ± 10 mA (1)	 0.735 0.732	 0.750 0.750	 0.765 0.768	
		PVIN = VDDQ = 1.2 V I_{VREF} = 0 A I_{VREF} = ± 5 mA (1)	 0.585 0.582	 0.600 0.600	 0.615 0.618	
V_{TT} Voltage	V_{TT}	PVIN = VDDQ = 1.8 V I_{VTT} = 0 A I_{VTT} = ± 2 A (2)	 0.880 0.870	 0.900 0.900	 0.920 0.930	V
		PVIN = VDDQ = 1.5 V I_{VTT} = 0 A I_{VTT} = ± 1.5 A (2)	 0.730 0.720	 0.750 0.750	 0.770 0.780	
		PVIN = VDDQ = 1.2 V I_{VTT} = 0 A I_{VTT} = ± 0.5 A (2)	 0.580 0.570	 0.600 0.600	 0.620 0.630	
V_{TT} Output Voltage Offset	V_{OS}	PVIN = VDDQ = 1.8 V I_{VTT} = 0 A, ± 2 A (2)	 -20	 0	 20	mV
		PVIN = VDDQ = 1.5 V I_{VTT} = 0 A, ± 1.5 A (2)	 -20	 0	 20	
		PVIN = VDDQ = 1.2 V I_{VTT} = 0 A, ± 0.5 A (2)	 -20	 0	 20	
Quiescent Current	I_{AVIN}	I_{VREF} = I_{VTT} = 0 A		450		µA
VDDQ Input Impedance	Z_{VDDQ}			100		kΩ
Quiescent Current in Shutdown	I_{AVIN_SD}	VEN = 0 V		150	300	µA
Enable Threshold	V_{ENH}		1.8			V
	V_{ENL}				0.6	V
Enable Input Current	I_{EN}				0.5	µA
V_{TT} Leakage Current in Shutdown	I_{VTT}	VEN = 0 V, V_{TT} = 0.9 V			10	µA
VTTSNS Input Current	I_{VTTSNS}				0.1	µA
V_{TT} Current Limit	I_{CL_SRC}	Sourcing, 90 % x V_{TT}		2.9		A
	I_{CL_SINK}	Sinking, 110 % x V_{TT}		3.6		A
AVIN UVLO Threshold Voltage	V_{UVLOH_AVIN}		2.85			V
	V_{UVLOL_AVIN}				2.42	V
VDDQ UVLO Threshold Voltage	V_{UVLOH_VDDQ}		0.49			V
	V_{UVLOL_VDDQ}				0.41	V
Thermal Shutdown Temperature	T_{SD}			155		℃
Thermal Shutdown Hysteresis	ΔT_{SD}			20		℃

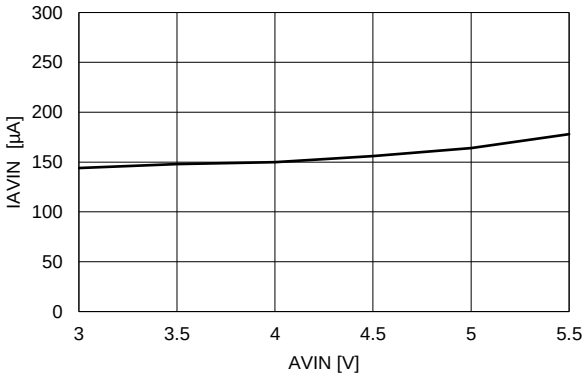
Note 1. V_{REF} load regulation is tested by using a 10 ms current pulse and measuring V_{REF}.

Note 2. V_{TT} load regulation is tested by using a 10 ms current pulse and measuring V_{TT}.

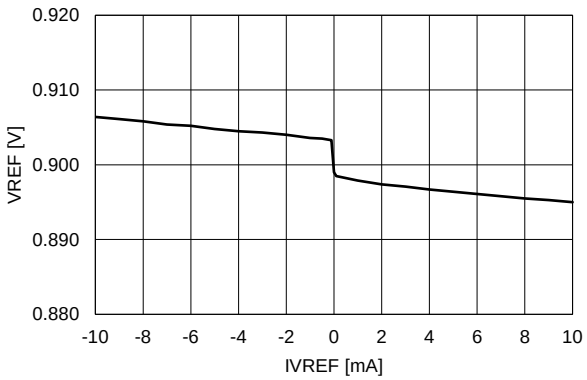
TYPICAL OPERATING CHARACTERISTICS



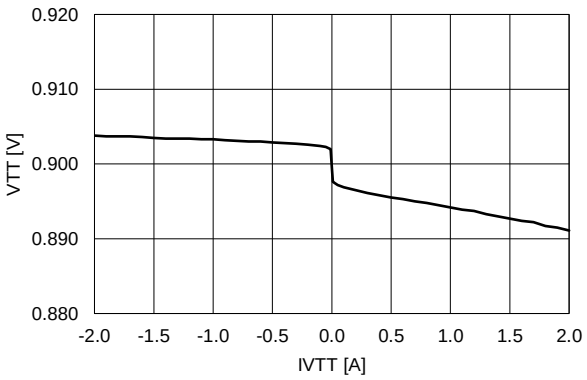
Quiescent Current



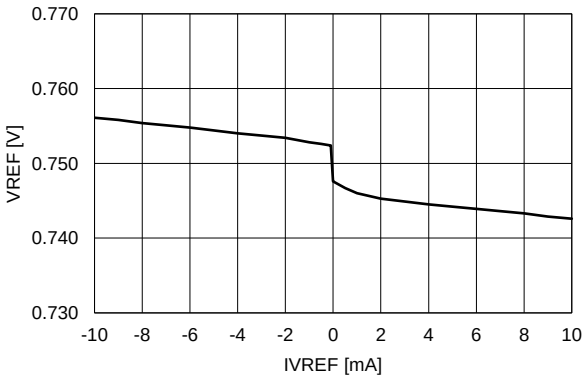
Quiescent Current in Shutdown



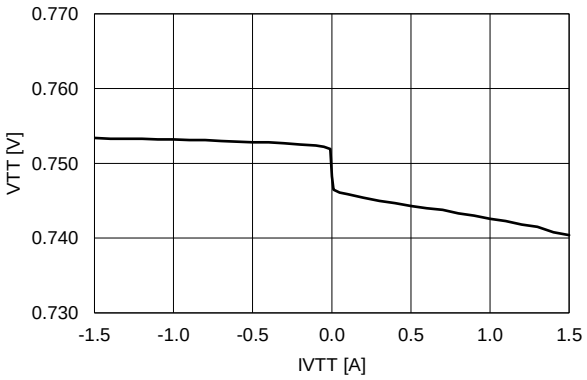
VREF Load Regulation
(AVIN = 5.0 V, PVIN = 1.8 V, VDDQ = 1.8 V)



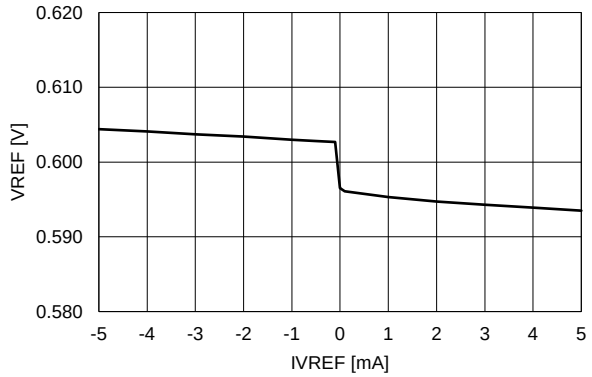
VTT Load Regulation
(AVIN = 5.0 V, PVIN = 1.8 V, VDDQ = 1.8 V)



VREF Load Regulation
(AVIN = 5.0 V, PVIN = 1.5 V, VDDQ = 1.5 V)

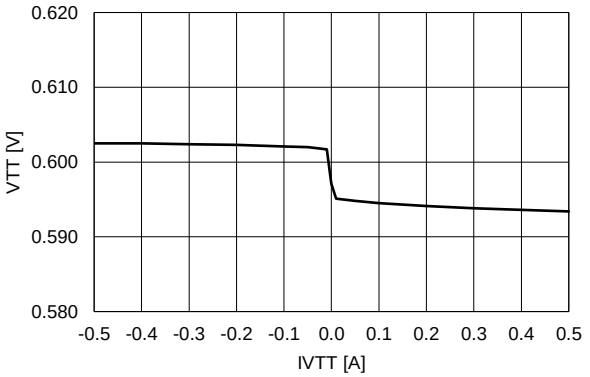


VTT Load Regulation
(AVIN = 5.0 V, PVIN = 1.5 V, VDDQ = 1.5 V)



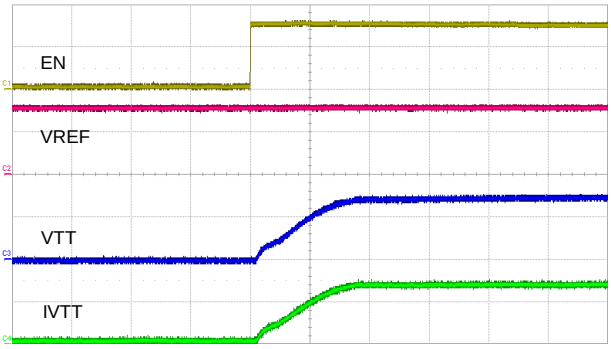
VREF Load Regulation

(AVIN = 5.0 V, PVIN = 1.2 V, VDDQ = 1.2 V)



VTT Load Regulation

(AVIN = 5.0 V, PVIN = 1.2 V, VDDQ = 1.2 V)

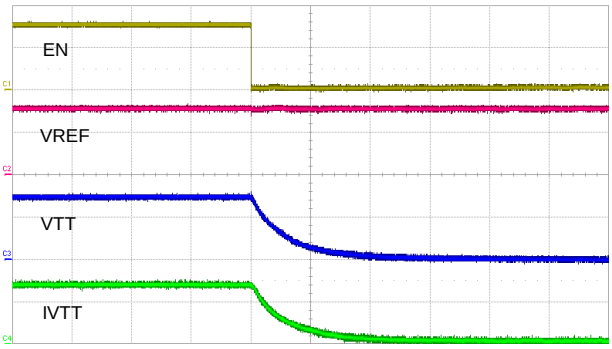


TIME: 20.0 µs/div

EN: 2.0 V/div, VREF: 500 mV/div, VTT: 500 mV/div, IVTT: 1.0 A/div

Start-Up by EN with Load

(AVIN = 3.3 V, PVIN = 1.5 V, VDDQ = 1.5 V, IVTT = 1.5 A (Source))

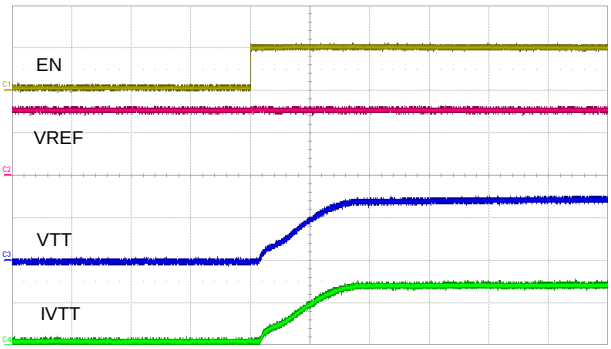


TIME: 20.0 µs/div

EN: 2.0 V/div, VREF: 500 mV/div, VTT: 500 mV/div, IVTT: 1.0 A/div

Shutdown by EN with Load

(AVIN = 3.3 V, PVIN = 1.5 V, VDDQ = 1.5 V, IVTT = 1.5 A (Source))

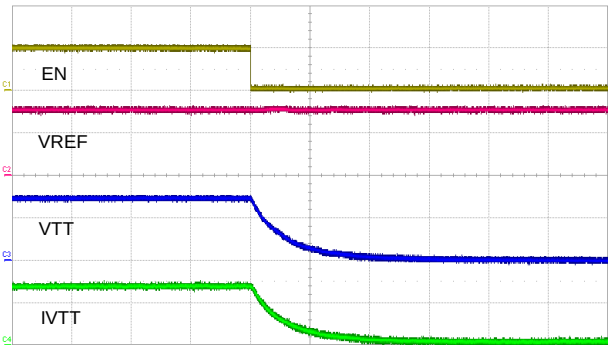


TIME: 20.0 µs/div

EN: 5.0 V/div, VREF: 500 mV/div, VTT: 500 mV/div, IVTT: 1.0 A/div

Start-Up by EN with Load

(AVIN = 5.0 V, PVIN = 1.5 V, VDDQ = 1.5 V, IVTT = 1.5 A (Source))

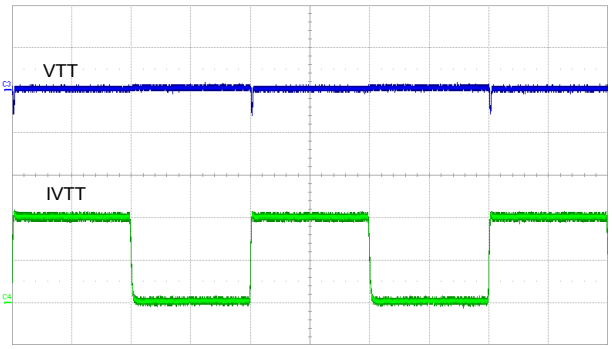


TIME: 20.0 µs/div

EN: 5.0 V/div, VREF: 500 mV/div, VTT: 500 mV/div, IVTT: 1.0 A/div

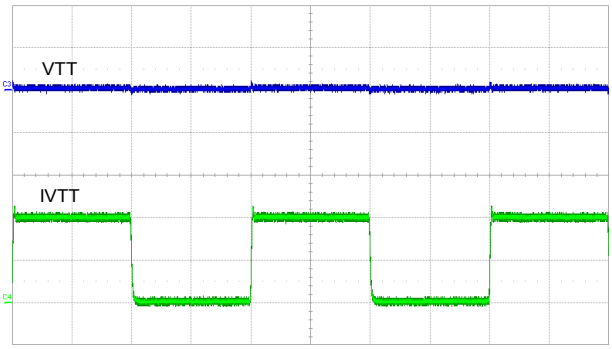
Shutdown by EN with Load

(AVIN = 5.0 V, PVIN = 1.5 V, VDDQ = 1.5 V, IVTT = 1.5 A (Source))



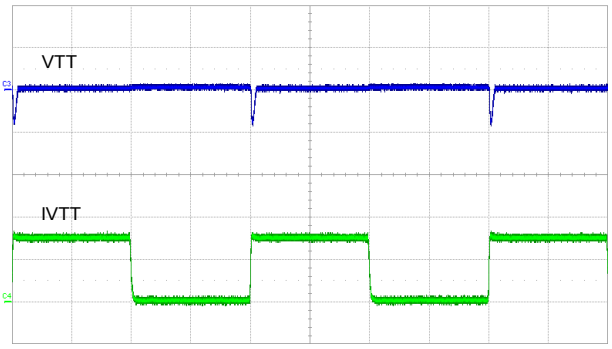
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 1.0 A/div

Load Transient Response
(AVIN = 3.3 V, PVIN = 1.8 V, VDDQ = 1.8 V, IVTT = 0 A to 2.0 A (Source))



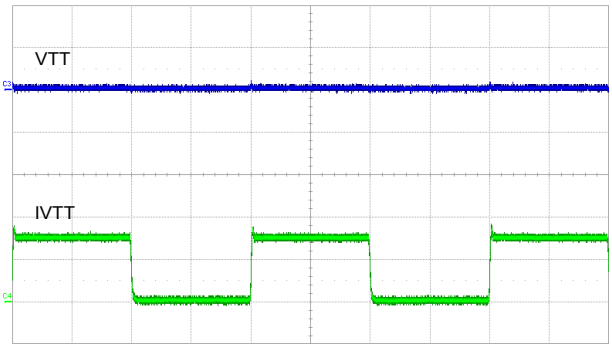
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 1.0 A/div

Load Transient Response
(AVIN = 3.3 V, PVIN = 1.8 V, VDDQ = 1.8 V, IVTT = 0 A to 2.0 A (Sink))



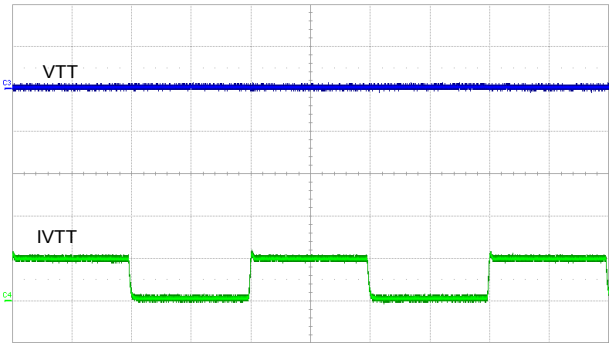
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 1.0 A/div

Load Transient Response
(AVIN = 3.3 V, PVIN = 1.5 V, VDDQ = 1.5 V, IVTT = 0 A to 1.5 A (Source))



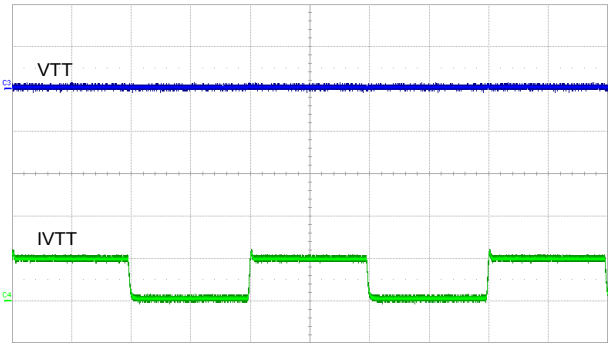
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 1.0 A/div

Load Transient Response
(AVIN = 3.3 V, PVIN = 1.5 V, VDDQ = 1.5 V, IVTT = 0 A to 1.5 A (Sink))



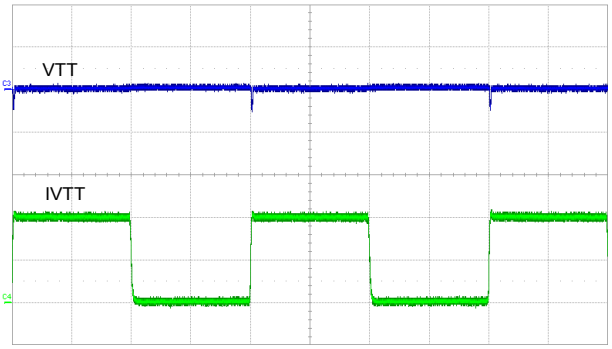
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 500 mA/div

Load Transient Response
(AVIN = 3.3 V, PVIN = 1.2 V, VDDQ = 1.2 V, IVTT = 0 A to 0.5 A (Source))



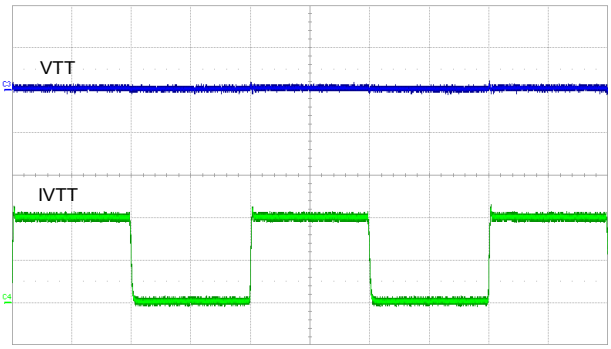
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 500 mA/div

Load Transient Response
(AVIN = 3.3 V, PVIN = 1.2 V, VDDQ = 1.2 V, IVTT = 0 A to 0.5 A (Sink))



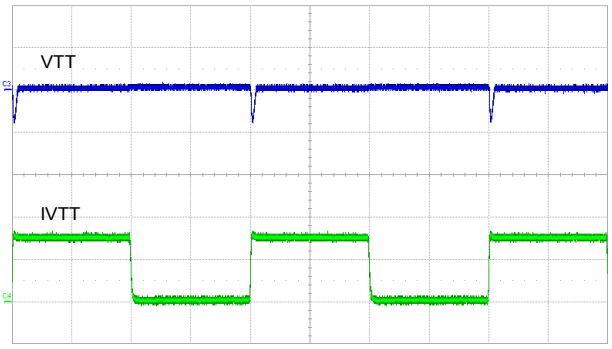
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 1.0 A/div

Load Transient Response
(AVIN = 5.0 V, PVIN = 1.8 V, VDDQ = 1.8 V, IVTT = 0 A to 2.0 A (Source))



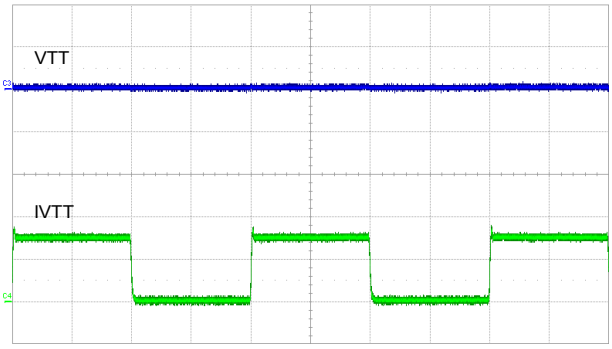
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 1.0 A/div

Load Transient Response
(AVIN = 5.0 V, PVIN = 1.8 V, VDDQ = 1.8 V, IVTT = 0 A to 2.0 A (Sink))



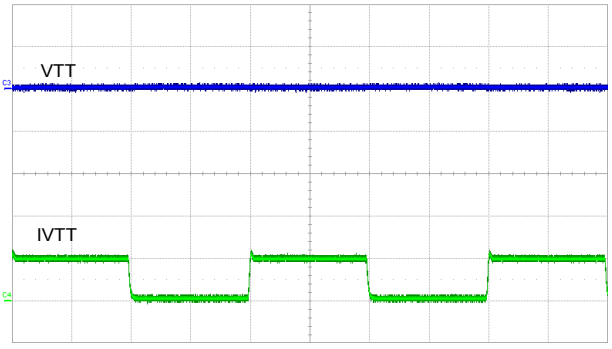
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 1.0 A/div

Load Transient Response
(AVIN = 5.0 V, PVIN = 1.5 V, VDDQ = 1.5 V, IVTT = 0 A to 1.5 A (Source))



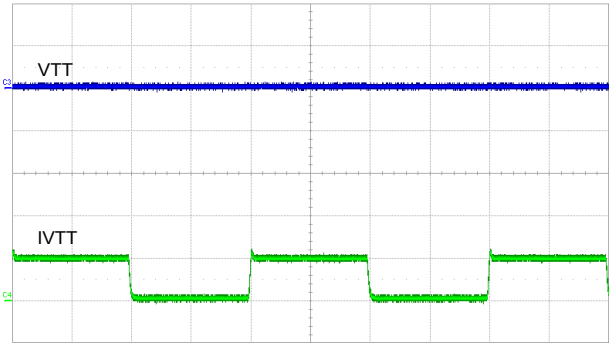
TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 1.0 A/div

Load Transient Response
(AVIN = 5.0 V, PVIN = 1.5 V, VDDQ = 1.5 V, IVTT = 0 A to 1.5 A (Sink))



TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 500 mA/div

Load Transient Response
(AVIN = 5.0 V, PVIN = 1.2 V, VDDQ = 1.2 V, IVTT = 0 A to 0.5 A (Source))



TIME: 500 µs/div
VTT: 20 mV/div (AC), IVTT: 500 mA/div

Load Transient Response
(AVIN = 5.0 V, PVIN = 1.2 V, VDDQ = 1.2 V, IVTT = 0 A to 0.5 A (Sink))

DESCRIPTION

The TJ2998 is a linear bus termination regulator designed for DDR2, DDR3, DDR3L and DDR4 memories. The output, VTT is capable of sinking and sourcing current while regulating the output voltage equal to VDDQ / 2. The output stage has been designed to maintain excellent load regulation while preventing shoot through. The TJ2998 also incorporates two distinct power rails that separate the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the TJ2998 to provide a termination solution for the next generation of DDR-SDRAM memory.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR-SDRAM. The most common form of termination is Class II single parallel termination. This involves one R_S series resistor from the chipset to the memory and one R_T termination resistor. Typical values for R_S and R_T are 25 Ohms, although these can be changed to scale the current requirements from the TJ2998. This implementation can be seen below in Figure 1.

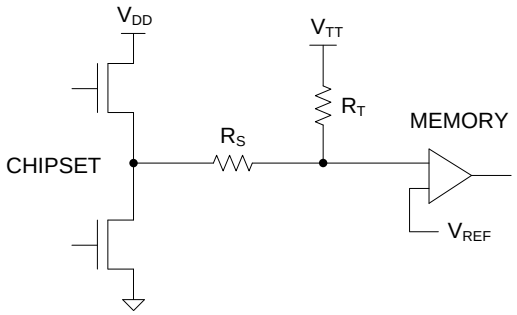


Fig. 1. SSTL-Termination Scheme

PIN DESCRIPTION

AVIN and PVIN

AVIN and PVIN are the input supply pins for the TJ2998. AVIN is used to supply all the internal control circuitry. PVIN, however, is used exclusively to provide the rail voltage for the output stage used to create VTT. These pins have the capability to work off separate supplies depending on the application.

Higher voltages on PVIN will increase the maximum continuous output current because of output R_{DSON} limitations at voltages close to VTT. The disadvantage of high values of PVIN is that the internal power loss will also increase, thermally limiting the design.

The limitation on input voltage selection is that PVIN must be equal to or lower than AVIN. It is recommended to connect PVIN to voltage rails equal to or less than 1.8V to prevent the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown then the part will enter a shutdown state where both VTT and VREF are tri-stated.

VDDQ

VDDQ is the input used to create the internal reference voltage for regulating VTT. The reference voltage

is generated from a resistor divider of two internal 50kΩ resistors. This guarantees that VTT will track VDDQ / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 1.8V rail at the DIMM instead of PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines.

VTTSNS

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to VTT in a long plane. If the output voltage was regulated only at the output of the TJ2998 then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The VTTSNS pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the VTTSNS pin must still be connected to VTT. Care should be taken when a long VTTSNS trace is implemented in close proximity to the memory. Noise pickup in the VTTSNS trace can cause problems with precise regulation of VTT. A small 0.1µF ceramic capacitor placed next to the VTTSNS pin can help filter any high frequency signals and preventing errors.

EN

The TJ2998 contains an active high enable pin that can be used to tri-state VTT. During shutdown VTT should not be exposed to voltages that exceed AVIN. With the enable pin asserted low the quiescent current of the TJ2998 will drop, however, VDDQ will always maintain its constant impedance of 100kΩ for generating the internal reference. Therefore to calculate the total power loss in shutdown both currents need to be considered. For more information refer to the Thermal Dissipation section.

VREF

VREF provides the buffered output of the internal reference voltage VDDQ / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically extremely high impedance, there should be little current drawn from VREF. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A low ESR ceramic capacitor in the range of 0.1µF to 0.01µF is recommended. This output remains active during the shutdown state for the suspend to RAM functionality.

VTT

VTT is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VDDQ / 2. The TJ2998 is designed to handle peak transient currents of up to ± 3A with a fast transient response at a certain operating condition. If a transient is expected to last above the maximum continuous current rating for a significant amount of time then the output capacitor should be sized large enough to prevent an excessive voltage drop. Despite the fact that the TJ2998 is designed to handle large transient output currents it is not capable of handling these for long durations, under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal derating should always be used (please refer to the Thermal Dissipation section). If the junction

temperature exceeds the thermal shutdown point than VTT will tri-state until the part returns below the hysteretic trip-point. In order to maintain stability, it is recommended to use low ESR ceramic capacitors. High ESR capacitors should not be used in the design. For stable operation, the total capacitance of the VTT output pin must be greater than 20 µF. Attach multiple 10 µF ceramic capacitors in parallel to minimize the effect of equivalent series resistance (ESR). X7R or X5R dielectrics are recommended to maintain sufficient capacitance over its full operating temperature.

THERMAL DISSIPATION

Since the TJ2998 is a linear regulator any current flow from VTT will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise, T_{Rmax} can be calculated given the maximum ambient temperature, T_{Amax} of the application and the maximum allowable junction temperature, T_{Jmax}.

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

From this equation, the maximum allowable power dissipation, P_{Dmax} of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA}$$

The maximum allowable value for junction-to-ambient thermal resistance, θ_{JA}, can be calculated using the formula:

$$\theta_{JA} = T_{Rmax} / P_D = (T_{Jmax} - T_{Amax}) / P_D$$

The θ_{JA} of the TJ2998 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow.
Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout it is possible to reduce the θ_{JA} further than the nominal values. Additional improvements in lowering the θ_{JA} can also be achieved with a constant airflow across the package.
Optimizing the θ_{JA} and placing the TJ2998 in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at VTT, either sinking or sourcing, and quiescent current at AVIN and VDDQ. During the active state (when enable is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT}$$

Where, $P_{AVIN} = I_{AVIN} \times V_{AVIN}$

$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$

To calculate the maximum power dissipation at VTT both conditions at VTT need to be examined, sinking and sourcing current. Although only one equation will add into the total, VTT cannot source and sink current simultaneously.

$P_{VTT} = V_{VTT} \times I_{LOAD}$ (Sinking) or $P_{VTT} = (V_{PVIN} - V_{VTT}) \times I_{LOAD}$ (Sourcing)

The power dissipation of the TJ2998 can also be calculated during the shutdown state. During this condition the output VTT will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AVIN and the constant impedance that is seen at the VDDQ pin.

$P_D = P_{AVIN} + P_{VDDQ}$,

Where, $P_{AVIN} = I_{AVIN} \times V_{AVIN}$

$P_{VDDQ} = V_{VDDQ} \times I_{VDDQ} = V_{VDDQ2} \times R_{VDDQ}$

TYPICAL APPLICATION INFORMATION

Several different application circuits have been shown in Figure 2 through Figure 6 to illustrate some of the options that are possible in configuring the TJ2998.

DDR2 APPLICATIONS

With the separate VDDQ pin and an internal resistor divider it is possible to use the TJ2998 in applications utilizing DDR2 memory. Figure 2 shows the recommended circuit configuration for DDR2 applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 3.3V or 5.0V rail.

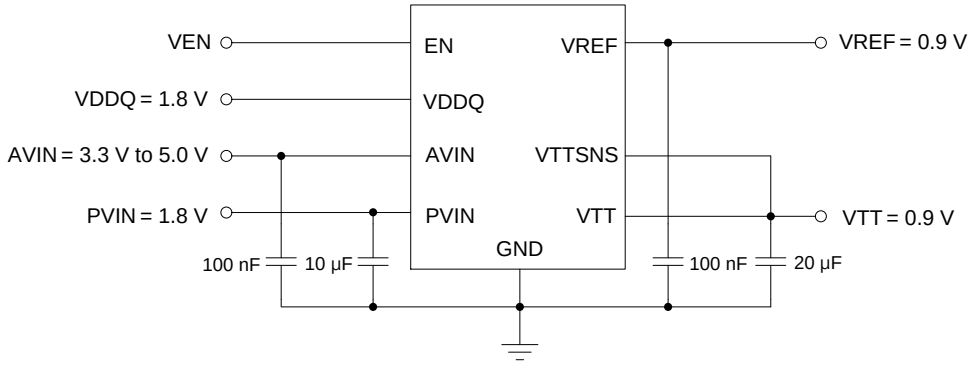


Fig. 2. Recommended DDR2 Termination

If it is not desirable to use the 1.8V rail it is possible to connect the output stage to higher than a 1.8V rail. Care should be taken to do not exceed the maximum junction temperature as the thermal dissipation increases with lower VTT output voltages. The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

LEVEL SHIFTING

If standards other than SSTL-18 are required, such as SSTL-2, it may be necessary to use a different scaling factor than 0.5 times VDDQ for regulating the output voltage. Several options are available to scale the output to any voltage required. One method is to level shift the output by using feedback resistors from VTT to the VTTSNS pin. This has been illustrated in Figures 3 and 4. Figure 3 shows how to use two resistors to level shift VTT above the internal reference voltage of VDDQ / 2. To calculate the exact voltage at VTT the following equation can be used

$$V_{TT} = V_{DDQ} / 2 (1 + R1 / R2)$$

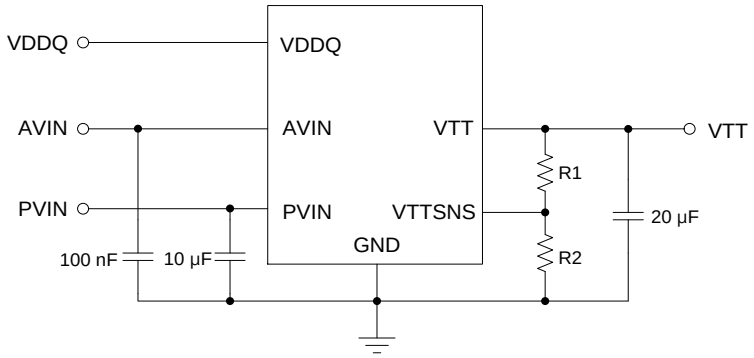


Fig. 3. Increasing VTT by Level Shifting

Conversely, the R2 resistor can be placed between VTTSNS and VDDQ to shift the VTT output lower than the internal reference voltage of VDDQ / 2. The equations relating VTT and the resistors can be seen below:

$$V_{TT} = V_{DDQ} / 2 (1 - R1 / R2)$$

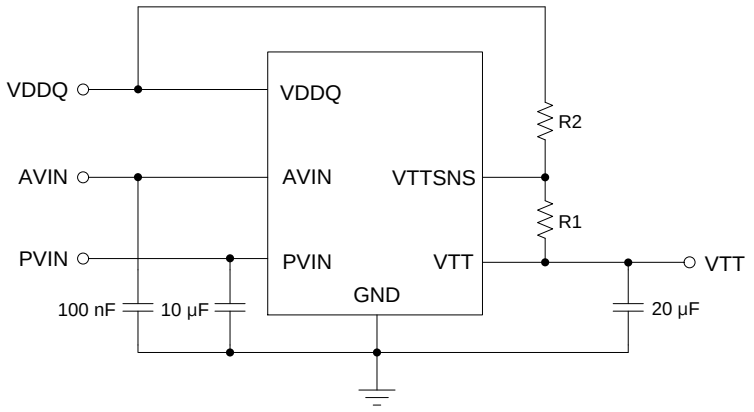


Fig. 4. Decreasing VTT by Level Shifting

HSTL APPLICATIONS

The TJ2998 can be easily adapted for HSTL applications by connecting VDDQ to the 1.5V rail. This will produce a VTT and VREF voltage of approximately 0.75V for the termination resistors. It is possible to connect PVIN to higher than a 1.5V rail for higher source/sink current. Care should be taken to do not exceed the maximum junction temperature as the thermal dissipation increases with lower VTT output voltages (For more information, refer to the Thermal Dissipation section). The advantage of this configuration is that it has the ability to source and sink a higher maximum continuous current.

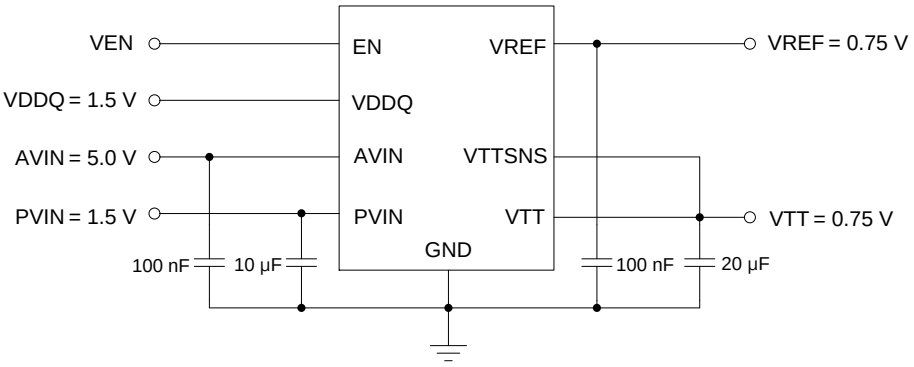


Fig. 5. HSTL Application

QDR APPLICATIONS

Quad data rate (QDR) applications utilize multiple channels for improved memory performance. However, this increase in bus lines has the effect of increasing the current levels required for termination. The recommended approach in terminating multiple channels is to use a dedicated TJ2998 for each channel. This simplifies layout and reduces the internal power dissipation for each regulator. Separate VREF signals can be used for each DIMM bank from the corresponding regulator with the chipset reference provided by a local resistor divider or one of the TJ2998 signals. Because VREF and VTT are expected to track and the part to part variations are minor, there should be little difference between the reference signals of each TJ2998.

OUTPUT CAPACITOR SELECTION

For applications utilizing the TJ2998 to terminate SSTL-18 I/O signals the typical application circuit shown in Figure 6 can be implemented.

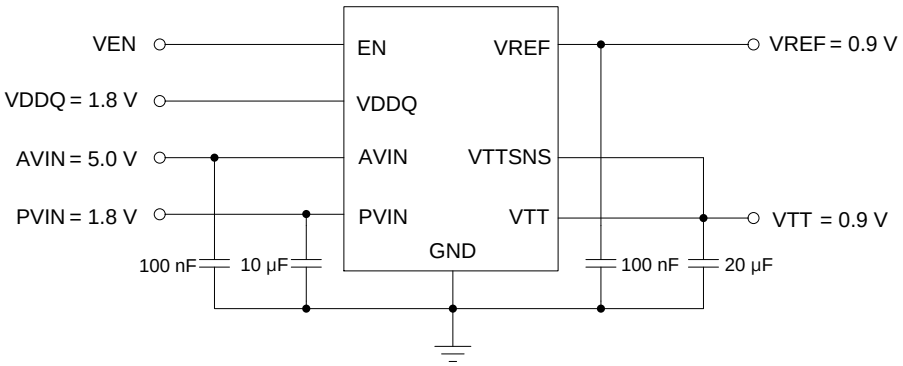


Fig. 6. Typical SSTL-18 Application Circuit

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where VTT is distributed across a long plane it is advisable to use multiple capacitors and addition to high frequency decoupling.

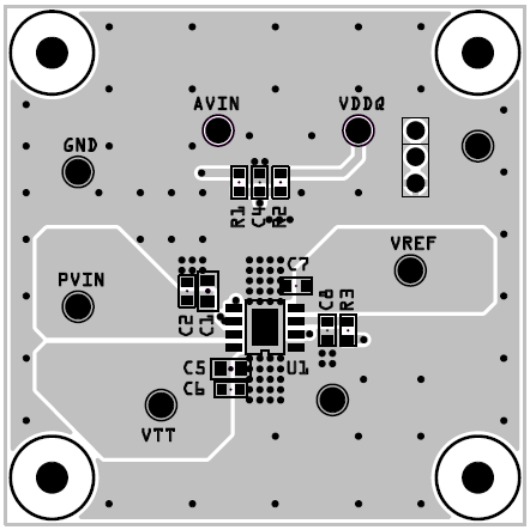
In most PC applications an extensive amount of decoupling is required because of the long interconnects encountered with the DDR-SDRAM DIMMs mounted on modules. As a result low ESR ceramic capacitors in the range of 100µF are typically used.

PCB LAYOUT CONSIDERATIONS

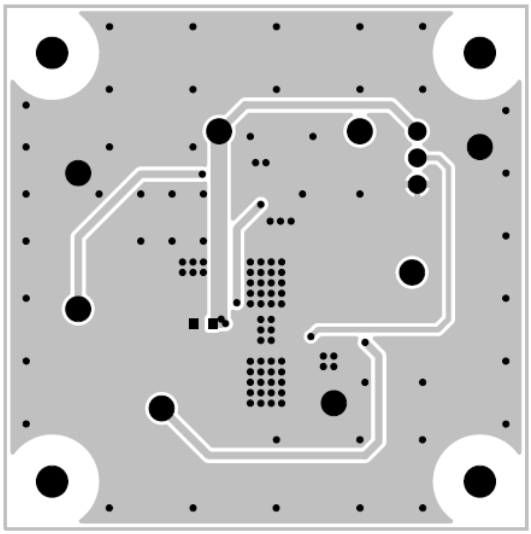
1. The input capacitor for the power rail should be placed as close as possible to the PVIN pin.
2. VTTSNS should be connected to the VTT termination bus at the point where regulation is required. For mother- board applications an ideal location would be at the center of the termination bus.
3. VDDQ can be connected remotely to the VDDQ rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the VTTSNS trace to avoid noise pickup from switching I/O signals. A 0.1µF ceramic capacitor located close to the VTTSNS can also be used to filter any unwanted high frequency signal. This can be an issue especially if long VTTSNS traces are used.
6. VREF should be bypassed with a 0.01 µF or 0.1 µF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the VREF pin.
7. VTT requires a 20 µF (or greater) ceramic capacitor to maintain stability. This capacitor should be located as close as possible to the VTT pin.

Evaluation Board Layout Example

TOP



BOTTOM



REVISION NOTICE

The description in this datasheet is subject to change without notice to describe its electrical characteristics properly. Please contact us to get the latest version of datasheet.