EM9203: 1Volt, 2Mbps, 2.4GHz GFSK Transceiver

Description

The EM9203 is a 1Mbps or 2Mbps low-power, low-voltage, completely-integrated 2.4GHz ISM band RF transceiver ideal for battery operated wireless applications such as wireless sensors and control, audio streaming, human interface devices, and security networks.

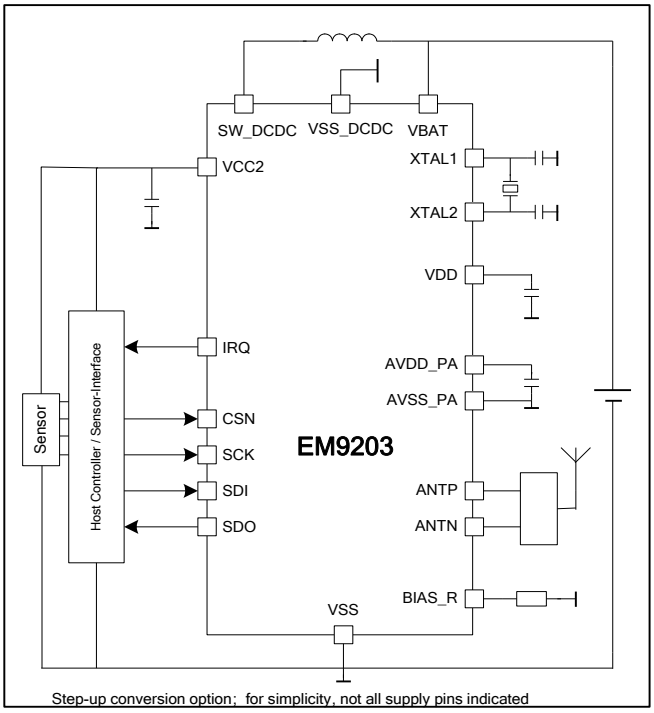
The EM9203's built-in baseband processor (with link-layer) permits implementation of optimized proprietary wireless protocol links in the license-free 2.4000GHz to 2.4835GHz ISM band. It includes a low-IF receiver architecture and uses GFSK modulation compliant with the emerging Bluetooth Low Energy (4.0) standard. An industry-standard SPI interface provides for simple control of the baseband using an external host controller.

The EM9203 Version 11 features an integrated step-up (boost) DC/DC converter that allows operation with supply voltages as low as 0.8V with an external coil. This converter is designed to support an additional load such as a low-power microcontroller (host) and interface circuits with a dedicated application profile. The EM9203 Version 12 can be supplied by a 3V battery or other voltage source.

Available chip versions:

- Version 11: with DC/DC converter for use with 1.5V battery (down to 0.8V)
- Version 12: without DC/DC converter for use with any voltage from 1.9V to 3.6V

Simplified Application Schematic



Step-up conversion option; for simplicity, not all supply pins indicated

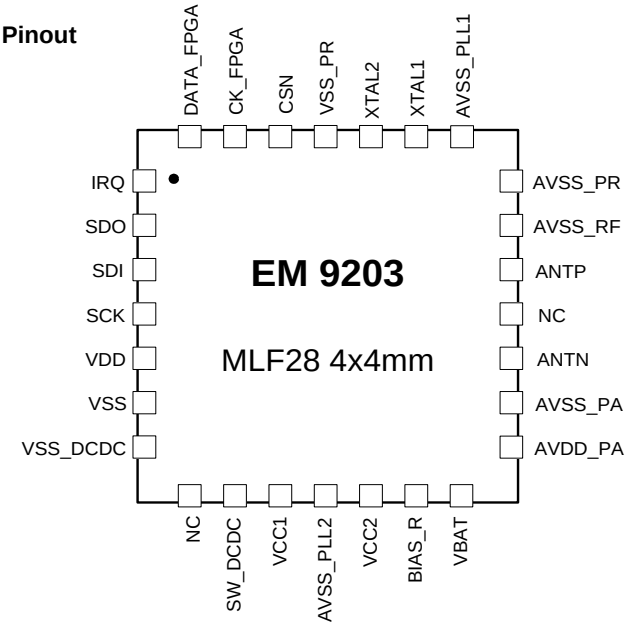
Features

- Low Voltage:
  - Single-cell, 1.5V battery operation (down to 0.8V); or
  - 3V battery operation (1.9V to 3.6V)
- Low Power:
  - 14mA in RX Mode (2Mbps)
  - 14mA in TX Mode (0 dBm output power, 2Mbps)
  - <3µA in Xtreme Mode (Version 11)
  - <1µA in Power-Down Mode (Version 12)
- High Performance:
  - -85dBm sensitivity at 2Mbps
  - Programmable output power from -18dBm to +3dBm
- Compact radio design with low BOM cost:
  - MLF28 4mm x 4mm package
  - Operating Temperature: -40°C to +85°C
  - Direct antenna interface
  - Integrated DC/DC converter (Version 11)
  - Supply Voltage Level Detector (SVLD)
  - 26MHz crystal oscillator, frequency tolerance ±50ppm
- Flexible interface:
  - Microcontroller compatible SPI interface
  - FPGA access to modulator and demodulator
  - External PA control signal available

Typical Applications

- Remote sensing and control
- Wireless audio streaming
- Wireless mice, keyboards, toys etc.
- Wireless watch sensors, sports equipment

Pinout



A COMPANY OF THE SWATCH GROUP

Table of Contents

Table of Figures

Table of Tables

Writing Conventions

This product specification follows a set of typographic conventions that make the document consistent and easy to read. The following writing conventions are used:

Commands, bit state conditions, and register names are written in **`Courier New bold`**.

Pin names and pin signal conditions are written in `Courier New`.

Cross references are underlined and highlighted in blue.

1. Introduction

1.1 Overview

The EM9203 is a low-power, low-voltage, fully integrated 2.4GHz RF transceiver with complete power management ideal for battery operated wireless applications such as wireless sensors or control, audio streaming, human interface devices, and security networks.

The EM9203 employs a GFSK modulation scheme which is directly applied to the 2.4GHz transmitter power amplifier. RF output power is digitally tuned over a wide range (-18dBm to +3dBm) to optimize current consumption and transmitted power for the application. The on-air transmission rate is digitally programmed to 1Mbps or 2Mbps.

The EM9203 features a fully integrated low-noise, high-sensitivity 2.4GHz front end (-90dBm at 1Mbps; -85dBm at 2Mbps) with a high maximum input power at either data rate. Due to its robust low-IF receiver architecture, the EM9203 does not require expensive external filters to block undesired RF signals. Additionally, the integration of an agile frequency synthesizer makes the EM9203 well suited for frequency hopping applications.

The EM9203 may be directly connected to a properly designed 200-Ohm PCB loop antenna. Other antenna impedances may be accommodated through the use of a balun or simple matching network.

The EM9203 Version 11 incorporates a sophisticated DC/DC converter and power management system, enabling full operation with a single 1.5V coin cell. The DC/DC step-up converter powers the entire baseband and RF circuitry typically with 2.2V (configurable) and is also powerful enough to supply up to 100mA to an external load such as a microcontroller, an external sensor, or other user interface components. Furthermore, the DC/DC converter has an extreme low-power mode, Xtreme Mode, which is capable of providing 2V with very little intrinsic current consumption (<3μA), resulting in extremely power-efficient 1.5V applications with low RF duty cycle. Version 12 is available without the DC/DC converter for use with a 3V battery supply and also has very-low-power modes. Both versions have supply voltage level detection (SVLD) and battery protection mode (BPM) for safe end-of-battery-life control.

The EM9203 is an attractive choice for a broad range of wireless applications where power-efficient, single battery operation is desired. In addition, the low bill-of-materials (BOM) required implementing a complete solution with the EM9203 results in minimal overall system cost.

1.2 Applications schematic and block diagram

A simplified applications schematic and block diagram of Version 11 of the EM9203 is shown in Figure 1. Required external components include only a coil for the DC/DC converter, a crystal for the frequency synthesizer, a precision resistor for bias circuitry, and capacitors for supply decoupling. The major blocks that make up the EM9203 are the RF transceiver, baseband processor, power management circuitry, and digital interface. An overview of each of these blocks is provided in this section.

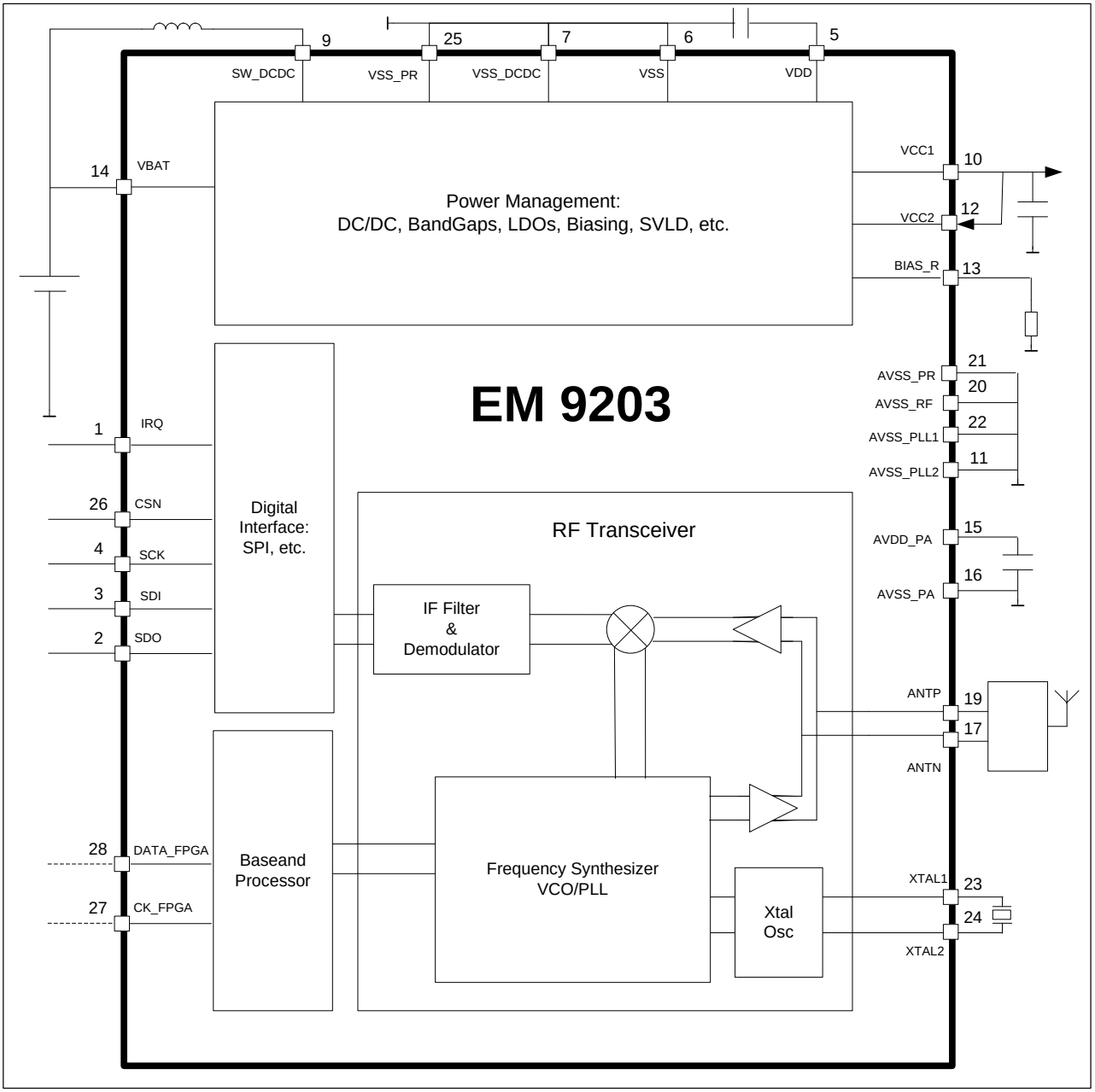


Figure 1: Simplified block diagram (DC/DC configuration)

1.3 RF transceiver

The highly integrated multi-channel RF transceiver is ideal for wireless applications in the world-wide, license-free, ISM frequency band at 2.4000GHz to 2.4835GHz. Its robust low-IF architecture and direct GFSK modulation scheme are designed not only for proprietary communication protocols, but also to be compatible with the emerging Bluetooth Low Energy Wireless standard. The EM9203 supports data transmission rates of 1Mbps or 2Mbps for up to 40 channels. The digital GFSK-modulation and demodulation is performed using a bit-bandwidth product (BT) of 0.5 and a data rate dependent modulation index of 0.5 for 1Mbps and 0.32 for 2Mbps.

The RF transceiver can be programmed to one of two primary modes:

- Transmit Mode: the entire transmit-chain is active and the digital baseband data can be up-converted to a 2.4GHz GFSK modulated signal
- Receive Mode: the frequency synthesizer and the entire receive-chain are active and ready to receive a packet.

The RF transceiver consists of three major subsystems: the frequency synthesizer/phase-locked loop (PLL), the receiver, and the transmitter. Each of these is described below.

1.3.1 Frequency synthesizer / Phase-Locked Loop (PLL)

The frequency synthesizer provides an accurate, low jitter 2.4GHz RF signal used for both up-conversion (in Transmit Mode) and down-conversion (in Receive Mode). Up to 40 different frequencies can be synthesized. Additionally, the PLL supports two-point GFSK modulation for use in the Transmit Mode. The benefit of two-point modulation is there is no frequency drift during packet transmission.

An auto-calibration mechanism is included in the PLL (see Section 5.2.6) for proper centering of the VCO control voltage.

1.3.2 Receiver

The receiver achieves both high sensitivity (-90dBm for 1Mbps and -85dBm for 2Mbps) and high maximum input power RF-reception at 2.4GHz. It is comprised of a low noise amplifier (LNA), followed by a down-conversion mixer and an IF-filter. The output of the IF-filter is fed to a limit-amplifier, and then the digital GFSK demodulator. The received clock and data are available at the demodulator output, and processed by the digital baseband circuitry.

The receiver also features a Received Signal Strength Indicator (RSSI), which can measure the down-converted RF power after the IF filter. The average power on the channel or burst power of a packet can be read via the SPI after the single-shot RSSI measurement has been completed (see Section 5.2.17).

1.3.3 Transmitter

The transmitter consists of a dual-rate (1Mbps and 2Mbps) two-point GFSK modulator which is included in the frequency synthesizer (see Section 1.3.1) and a programmable Power Amplifier (PA) output stage. Eight power levels are available from +3dBm down to -18dBm for range/power consumption optimization. A control signal is also provided for an external PA.

1.4 Baseband processor

The baseband processor is the central digital control system of the EM9203. It manages all modes of the EM9203 and controls the RF transceiver. Furthermore, it configures digital data for transmission and processes packets received from the demodulator (what is commonly referred to as the link layer).

The primary operational modes of the EM9203 are Receive (RX) Mode, Transmit (TX) Mode, and Standby Mode. An EM9203 configured for auto-acknowledge will send a packet in Transmit Mode, wait for the auto-acknowledge packet from the receiving device, and then go to Standby Mode. The EM9203 will automatically retransmit if the auto-acknowledgment indicates an error occurred or in the absence of an auto-acknowledgment. An EM9203 not configured for auto-acknowledge will send a packet in Transmit Mode, and then go directly to Standby Mode. The EM9203 can also be programmed to transmit several packets in succession.

In Receive Mode the EM9203 will wait for any packet on the selected channel at the selected data rate. When a packet is received, the EM9203 verifies the address, examines the packet information flags, and compares the transmitted data check value with the calculated check value. If the auto-acknowledge is enabled, the EM9203 sends the auto-acknowledge packet and returns to Receive Mode. The device will remain in Receive Mode until the host controller places it in Standby Mode. From Standby Mode, the host controller may access the other operational modes.

The EM9203 has several low power modes:

- Standby Mode consumes 140µA, typically
- Standby Low-Power Mode consumes 85µA
- Xtreme Mode (Version 11 only) consumes 2.8µA
- Power-Down Mode (Version 12) consumes 0.8µA

Each of these modes can be entered from Standby Mode quickly, but the lowest power modes will require more time to return to Standby Mode. See Section 3.4 for timing details.

1.5 Power management

The power management system of the EM9203 provides the necessary supplies, voltage and current references for reliable operation in all modes. This includes low drop-out voltage regulators (LDO) for the RF transceiver and all digital circuitry, a low noise bandgap, and a bias-generator using a precision external resistor. These circuits are powered through the VCC2 pin, either using the DC/DC converter (Version 11) or by direct supply connections (Version 12).

1.5.1 RF transceiver supply

Two on-chip regulators, for the receiver and the PLL, supply all analog circuits in the RF transceiver. There is also a dedicated regulator for the power amplifier which requires an external 22nF decoupling capacitor. The voltage reference for these regulators is derived from a low noise bandgap circuit. In order to optimize the current consumption in any mode of operation, the regulators as well as the bandgap/bias are enabled individually when needed.

1.5.2 Digital supply

A low power regulator with a dedicated bandgap reference for noise isolation generates the supply (VDD) for all digital parts in the system (base-band, frequency synthesizer and demodulator). This ensures that the digital logic circuitry is properly powered not only in RF modes, but also in the power-down modes described in Section 4.2.3. This regulator requires an external decoupling capacitor of 1μF.

1.5.3 Bias generator

In order to create a stable and temperature-independent current reference for the RF transceiver, the EM9203 features a bias generator that utilizes an on-chip bandgap reference and an external 27kΩ resistor. Variance in current consumption during operation is dependent on this resistance value. The maximum tolerance for this resistor is ±2%.

1.6 Digital interface

The digital interface includes an industry standard 4-pin Serial Peripheral Interface (SPI) and an interrupt pin. The SPI can operate at up to 10MHz for reading and writing to the register space. The interrupt pin can be programmed to indicate the status of the EM9203 (e.g., that a packet has been received or auto-calibration has finished). This functionality allows the host controller to complete other operations or even enter its own low power mode. Additionally, two pins are provided for interfacing to an FPGA for applications that, for example, require a custom link-layer. Additional details regarding the FPGA pins can be provided upon special request.

2. Pin information

Table 1: EM9203 pinout for all versions

Bond Pad #	MLF Pin #	Name	Notes	I/O	Pin Function	Description
8	1	IRQ		O	Digital Output	Interrupt output for external host controller
7	2	SDO		O	Digital Output	SPI data output
6	3	SDI		I	Digital Input	SPI data input
5	4	SCK		I	Digital Input	SPI clock input
4	5	VDD			Power	Regulated digital supply provided for external decoupling; not to be loaded by any external circuitry
3	6	VSS	1		Ground	Digital ground
2		VSS_PR	1		Ground	Pad-ring ground
1	7	VSS_DCDC	1		Ground	Version 11: DC/DC converter ground Version 12: Power management ground
	8	NC				No connection
27	9	SW_DCDC			Analog	DC/DC converter coil switch
26	10	VCC1		O	Power Output	Version 11: DC/DC output connect to VCC2 and peripherals; Version 12: connect to ground
25	11	AVSS_PLL2	1		Ground	PLL ground
24	12	VCC2		I	Power Input	Version 11: Radio supply, connect to VCC1 Version 12: Radio supply, connect to 3V battery
23	13	BIAS_R			Analog	Terminal for bias-setting resistor
22	14	VBAT		I	Power Input	Version 11: Connect to battery supply Version 12: Connect to ground
21	15	AVDD_PA			Power	Regulated PA supply provided for external decoupling; not to be loaded by any external circuitry
20	16	AVSS_PA	1		Ground	PA ground
19	17	ANTN		I/O	RF	Negative antenna terminal
	18	NC				No connection
18	19	ANTP		I/O	RF	Positive antenna terminal
17	20	AVSS_RF	1		Ground	RF ground
16	21	AVSS_PR	1		Ground	Pad-ring ground
15	22	AVSS_PLL1	1		Ground	PLL ground
14	23	XTAL1		I	Analog Input	Crystal oscillator input
13	24	XTAL2		O	Analog Output	Crystal oscillator output
12	25	VSS_PR	1		Ground	Pad-ring ground
11	26	CSN		I	Digital Input	SPI Chip Select
10	27	CK_FPGA	2	O	Digital output	No connect for normal operation Clock out for optional FPGA
9	28	DATA_FPGA	2	I/O	Digital I/O	No connect for normal operation Data terminal for optional FPGA
	Center	VSS_DIE	1		Ground	Die ground

Note 1: For a proper operation of the chip, this terminal shall be connected to a common ground plane.

Note 2: For typical operation of the chip, these terminals shall be floating.

3. Electrical specifications

Typical values are generally stated at room temperature (T=25ºC) with a supply voltage of VCC2=2.5V, for both Version 11 and Version 12.

3.1 Handling procedures and absolute maximum ratings

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as with any CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the specified voltage range.

Table 2: Absolute maximum ratings

Parameter	Min	Max	Unit
Supply Voltage VCC2 - VSS	-0.3	3.8	V
Input Voltage	VSS - 0.2	VCC2 + 0.2	V
Electrostatic discharge to Mil-Std-883 method 3015.7 with ref. to VSS	-2000	+2000	V
Maximum soldering conditions	As per Jedec J-STD-020		

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction

3.2 General operating conditions

Table 3: General operating conditions

Parameter	Min	Typ	Max	Unit
Supply voltage Version 11 (applied on pin VBAT)	0.8	1.5	1.8	V
Supply voltage Version 12 (applied on pin VCC2)	1.9	2.5	3.6	V
Temperature range	-40		+85	°C

3.3 Electrical characteristics

The electrical characteristics of all versions of the EM9203 are summarized in this section. The primary difference between the two versions is the use of the general supply VCC2 (Version 11 with the DC/DC converter, Version 12 without the DC/DC converter). The electrical characteristics for both versions are summarized in the following tables. A version summary is given in Section 7.

Table 4: Supply currents on VCC2 (all versions)

Operating Mode		Notes	Symbol	Conditions	Min	Typ	Max	Unit
Power-Down			I_{CC_PD}	Version 12 (no DC/DC), no oscillators running, register values maintained		0.8		µA
Xtreme			I_{CC_XTR}	Version 11 (DC/DC), RC oscillator running, crystal-oscillator off DC/DC in Xtreme Mode		2.8		µA
Standby		1	I_{CC_STDBY}	26MHz crystal oscillator active		140		µA
Standby Low Power		1	$I_{CC\_STDBY\_LP}$	Crystal Low Power Mode activated		85		µA
Autocalibration	1Mbps	2	I_{CC_AUTO1}	Channel 19		5.9		mA
	2Mbps		I_{CC_AUTO2}	Channel 19		6.5		mA
Transmit	1Mbps	2	I_{CC_TX1}	P_{OUT} = 0dBm, channel 19		12.6		mA

Operating Mode		Notes	Symbol	Conditions	Min	Typ	Max	Unit
	2Mbps		I_{CC_TX2}	P_{OUT} = 0dBm, channel 19		13.5		mA
Receive	1Mbps	2	I_{CC_RX1}	Channel 19		12.2		mA
	2Mbps		I_{CC_RX2}	Channel 19		14.0		mA

Conditions: No external DC/DC load.

Note 1: Standby current depends on the type of crystal used; typical values given are for ABM10 with 12pF load capacitors.

Note 2: For 1Mbps mode, additional current savings is obtained by modifying the VCO current register. See Section 5.2.19 for details.

Table 5: VBAT supply and DC/DC step-up converter (Version 11)

Parameter	Notes	Symbol	Conditions	Min	Typ	Max	Unit
Battery Voltage Range		V_{BAT}	I_{Lext} < 30mA	0.80	1.50	1.80	V
Minimum start-up voltage		V_{BAT_START}	I_{Lext} < 20mA			1.00	V
Battery-Low Detection Threshold Levels		V_{BAT_MIN} V_{BAT_MINW} V_{BAT_LO} V_{BAT_LOW}	Battery Protection Battery Protection, Early Warning Battery Low Indication Battery Low, Early Warning	 1.00	0.82 0.92 1.12 1.25	 1.22	V
Programmable Output Voltages	1	V_{CC1_OUT}	Code = '00' Code = '01' Code = '10' Code = '11'	1.90 2.00 2.55 2.70	2.10 2.20 2.75 2.90	2.30 2.40 2.95 3.10	V
Xtreme Mode output voltage		V_{CC1_XTR}	No external load		2.00		V
Output Voltage Ripple	2	V_{CC1_RIPPLE}	Active (RF mode),I_{Lext} < 30mA Xtreme mode, I_{Lext} < 0.5mA		10	 160	mV_{PP}
Converter Efficiency	3,4	DC/DC_Eff	Active (RF mode), I_{Lext} = 30mA Xtreme Mode, I_{Lext} = 30µA		90 53		%
External load on VCC1		$I_{VCC1\_EXT\_RX}$	VBAT > 1.2V			100	mA
		$I_{VCC1\_EXT\_XTR}$	Xtreme Mode			500	µA
Current drawn from battery in Battery Protection Mode		I_{BAT_BPM}	VBAT = 1.0V			75	µA

Conditions: VBAT = 1.4V, I_{Lext} = 10mA, EM9203 in RX Mode (unless otherwise specified)

Note 1: Refer to Section 5.4.21 for information about programming the DC/DC Control Register, **RegDCDC**

Note 2: For C = 22µF, ESR_C = 100mΩ and L = 10µH, ESR_L = 120mΩ

Note 3: Depends on external components (ESR_C, ESR_L, Ri_bat) – typical values are for C, L and ESR as in Note 1

Note 4: See Section 10.1 for detailed information

Table 6: VCC2 supply for Version 12

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Battery Voltage Range	V_{BAT_NODC}		1.9	2.5	3.6	V
Battery-Low Detection Threshold levels	V_{BATLO_NODC} $V_{BATLO\_W\_NODC}$	Battery Protection Battery Low, Early warning	2.10	2.24 2.49	2.45	V

Table 7: DC characteristics

Parameter	Symbol	Min	Typ	Max	Unit
HIGH level input voltage	V_{IH}	0.75 * VCC2		VCC2	V
LOW level input voltage	V_{IL}	0		0.25 * VCC2	V
HIGH level output voltage	V_{OH}	VCC2-0.3		VCC2	V
LOW level output voltage	V_{OL}	0		0.3	V

Conditions: 1mA maximum load for V_{OH}, V_{OL}

Table 8: RF characteristics

Parameter		Notes	Symbol	Min	Typ	Max	Unit
General RF conditions							
Operating frequency			f_{OP}	2400		2484	MHz
Differential antenna impedance					200		ohm
Data rate	1Mbps		DR_1		1.0		Mbps
	2Mbps		DR_2		2.0		Mbps
Channel spacing			F_{CHW}		2		MHz
Crystal frequency			f_{XTAL}		26		MHz
Crystal frequency accuracy		1				±50	ppm
Transmitter Operation							
Output Power	Power Level = 7		P_{RF7}		+3		dBm
	Power Level = 6		P_{RF6}		0		dBm
	Power Level = 5		P_{RF5}		-3		dBm
	Power Level = 4		P_{RF4}		-6		dBm
	Power Level = 3		P_{RF3}		-9		dBm
	Power Level = 2		P_{RF2}		-12		dBm
	Power Level = 1		P_{RF1}		-15		dBm
	Power Level = 0		P_{RF0}		-18		dBm
RF power accuracy			P_{RFAC}		+/-3		dB
Frequency deviation for 00001111 repeating sequence	1Mbps	2	Δf_{M1}		±250		kHz
	2Mbps	2	Δf_{M2}		±320		kHz
Power transmitted at freq offset $\lvert f_{offs} \rvert$ = 2MHz	1Mbps	3	P_{RF12}			-35	dBm
Power transmitted at freq offset $\lvert f_{offs} \rvert$ = 3MHz	1Mbps	3	P_{RF13}			-45	dBm
Power transmitted at freq offset $\lvert f_{offs} \rvert$ = 2MHz	2Mbps	3	P_{RF22}			-20	dBm
Power transmitted at freq offset $\lvert f_{offs} \rvert$ = 4MHz	2Mbps	3	P_{RF24}			-45	dBm

Parameter		Notes	Symbol	Min	Typ	Max	Unit
Power transmitted at freq offset $\lvert f_{offs} \rvert \geq$ 6MHz	2Mbps	3	P_{RF26}			-50	dBm
Receiver Operation							
Sensitivity for 0.1% BER at room temperature	1Mbps	4,5	RX_{SE1}		-90		dBm
	2Mbps	4,5	RX_{SE2}		-85		dBm

Note 1: Frequency accuracy includes initial tolerance, stability over temperature range, and aging of the quartz, as well as the effect of the tolerance of the required tuning capacitors.

Note 2: Positive frequency deviations are represented by a logic level '1', and negative frequency deviations are represented by a logic level '0'.

Note 3: Mask measurements tested with continuous wave output as described in Section 5.5. PN9 data is applied to DATA_FPGA pin.

Note 4: BER (Bit Error Rate) is specified based on the PER (Packet Error Rate) equivalent measurement of a packet with a 32 byte payload (PN9 data), and with the public address 12345B (reset). PER equivalent is 26.8% since the packet length is 312 bits.

Note 5: A small degradation in sensitivity and minimum PER is noticed on channels with an integer multiple of the crystal frequency (channels 8, 21, and 34).

Spurious emissions were measured on process corner parts over all temperature and voltage specifications. Figure 2 shows the maximum spurious emissions into a 50ohm load in Transmit Mode. Figure 3 shows the maximum spurious emissions into a 50ohm load in Receive Mode. To meet regulatory requirements for a specific application, proper filtering of the second harmonic is required on the application board PCB and antenna. Spurious emissions at twice the channel frequency are highly dependant on the external circuitry interfaced to the antenna, and including the antenna design. Recommended external circuits and performance of the EM9203 with these circuits can be obtained from EM.

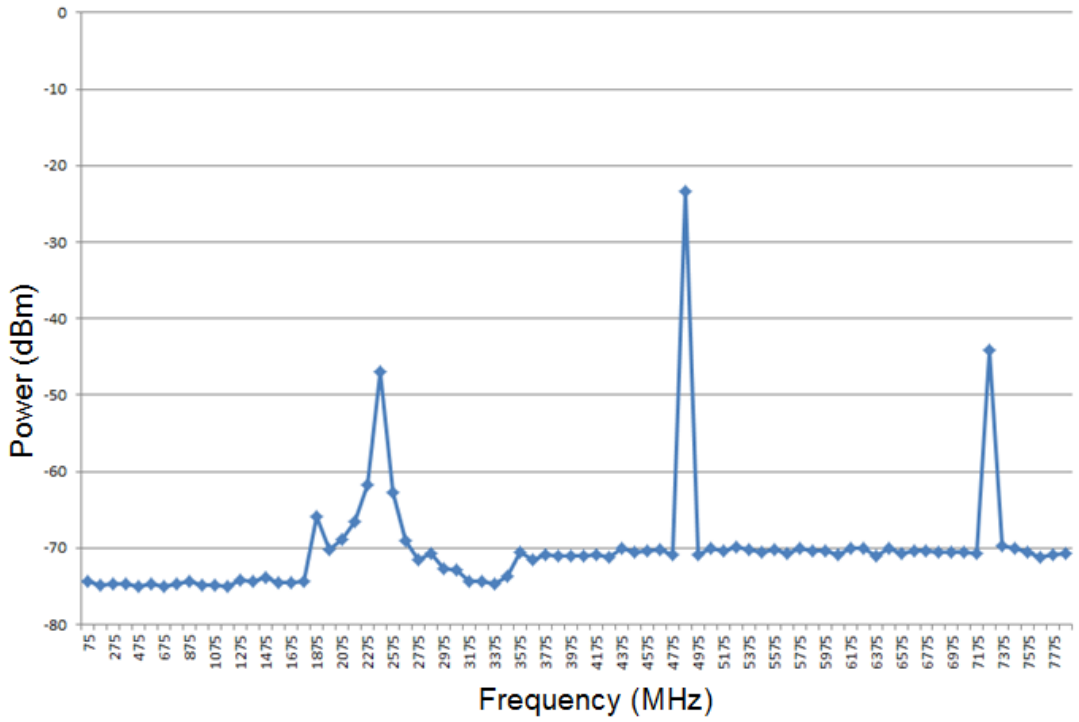


Figure 2: Maximum measured transmit mode spurious emissions into 50ohm load over all operating conditions

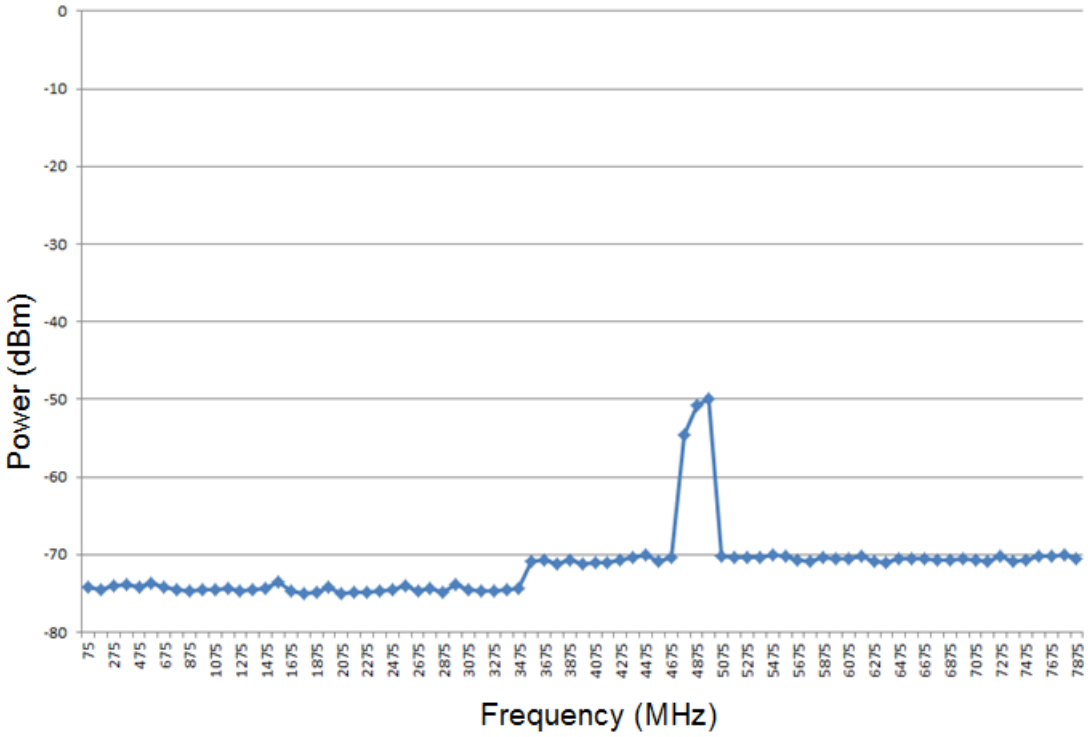


Figure 3: Maximum measured receive mode spurious emissions into 50ohm load over all operating conditions

3.4 Timing characteristics

Table 9: Timing Characteristics

Parameter	Notes	Symbol	Conditions	Min	Typ	Max	Unit
Startup	1	$t_{STARTUP}$	Version 11: VBAT=1.4V, I_{Lext}=10mA		7.5	12	ms
			Version 12: VBAT=2.5V, I_{Lext}=10mA		1.5	2.5	ms
RX↔TX in same channel	2	t_{RX_TX}			100		µs
Standby Mode → TX/RX Mode	2	t_{STDBY_RF}			100		µs
Power-down → Standby Mode	1	t_{PD_STDBY}	No external load		0.8	10	ms
Standby Low-Power → Standby Mode		$t_{STDBYLP\_STDBY}$			1		ms
Xtreme Mode → Standby Mode	1	t_{XTR_STDBY}	Output settled to within ripple spec; no external load		2.5	10	ms
DC/DC converter start-up	3	t_{STDBY_DCDC}	Version 11 only. Output settled to within ripple spec		10	30	ms
Auto-calibration		$t_{AUTOCAL}$			500		µs

Conditions: VBAT = 1.4V, I_{Lext} = 10mA (unless otherwise specified)

Note 1: Startup time is highly dependent on the crystal oscillator quality-factor. Typical values are measured with the ABM10 crystal as specified in Table 39. Maximum start time is specified for ABM10 with significant margin for Q-factor spreading.

Note 2: Optimum RX performance can take up to 200us to achieve at cold temperatures (e.g. below -20°C).

Note 3: Initial start-up upon battery insertion, includes crystal start-up and RC cold-start. Depends on Q-factor (see note 1).

4. Functional Modes

4.1 Start-up Mode

The start-up procedure is described below and differs only slightly for each of the two versions of the EM9203. This description is intended to be informational only as it is independent of any external controls.

4.1.1 Start-up with DC/DC up-converter (Version 11)

When a battery is inserted, an RC oscillator starts up and provides a clock to the DC/DC converter in order to generate VCC1. The VCC1 voltage ramps up with soft-start circuitry, including current and voltage limitation to avoid damage to any circuitry. During start-up, the RF transceiver circuitry is disabled; only the power management and required bias circuitry is enabled.

The VCC2 voltage is monitored by the SVLD circuit. When a sufficient voltage level is detected, the crystal oscillator is powered up and used as the main timing reference for the DC/DC converter and RF transceiver circuitry. When the crystal oscillator has sufficient amplitude, the full regulation circuitry of the DC/DC converter is switched on.

The interrupt (IRQ) pin is then set to logic '1' to indicate to the application (e.g., attached host controller) that the start-up sequence has completed. The DC/DC converter can then be externally loaded (e.g., peripherals / microcontroller) and the chip is ready to communicate via SPI. The DC/DC converter is designed to support external loads of 100mA. For efficiency versus load current see Section 10.1.1. Noise from the external load should be minimized when the EM9203 is in Transmit or Receive Mode for best RF performance.

4.1.2 Start-up without DC/DC (Version 12)

For applications not requiring the DC/DC converter, the EM9203 Version 12 is used. The start-up sequence is slightly different than described above. Upon connecting a battery to the VCC2 pin, the regulated digital supply ramps up quickly and the RC oscillator is turned on, providing a clock to the SVLD circuit. The crystal oscillator is then enabled and the interrupt (IRQ) pin is set to logic '1' after a crystal-dependent start-up time. (Some crystals may start up faster than other crystals depending on the quality factor.) The RC oscillator is then stopped.

4.2 Operational Modes

This section describes the operational modes of the EM9203. A simplified state diagram is given in Figure 4 , and each mode is described below. The EM9203 is fully functional at the end of the start-up procedure. The SPI interface is used to set or change the mode. In the event of a one-shot transmission, the EM9203 automatically enters Standby Mode when completed.

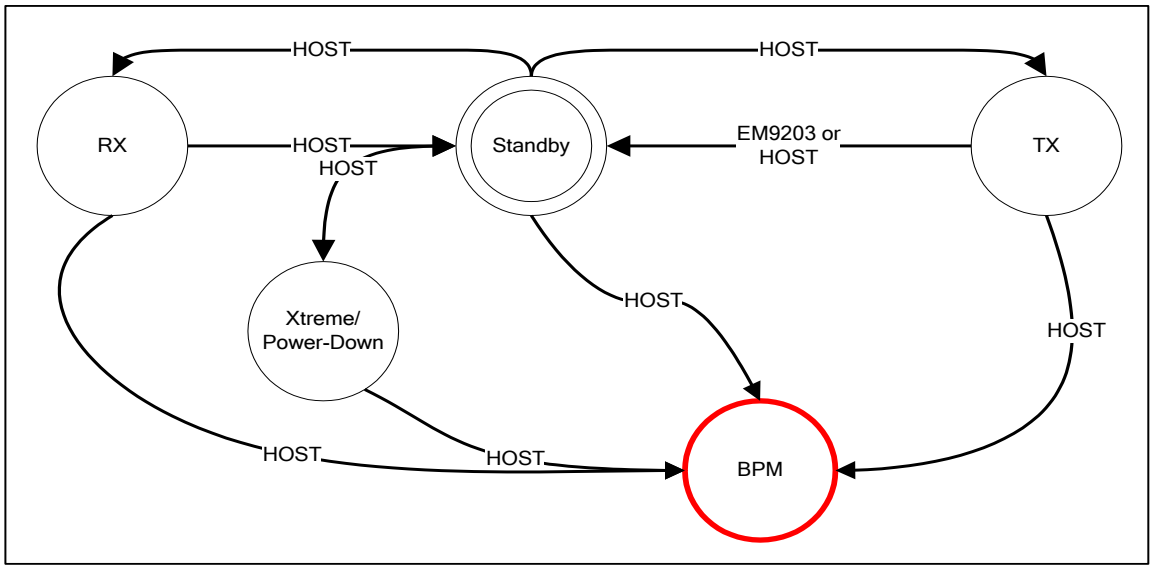


Figure 4: Simplified state diagram of EM9203 Modes

4.2.1 Standby Mode

Standby Mode is the default mode for the EM9203 following reset, and the starting point for any RF operation (transmission / reception) or activation of the power management modes (Xtreme / Power-Down Mode, etc.). The host can program the EM9203 for any operational mode only while it is in Standby Mode, as shown in the state diagram. In Standby Mode, only the crystal oscillator is running and, if a Version 11 chip is used, the DC/DC converter is also running.

4.2.2 Battery Protection Mode (BPM)

For single-cell battery applications using the DC/DC step-up converter, the EM9203 features a Battery Protection Mode. It protects weak batteries from leaking by limiting the amount of long-term constant current when the device is not used. BPM is a state in which all electronics, except a resistive load, are switched off. *It is important to note that the EM9203 will remain in Battery Protection Mode until a fresh battery is inserted.*

The BPM feature is of particular significance at the start-up of the system, since it can prevent excessive steady-state current due to an improperly started DC/DC converter if a weak battery is inserted. After the start-up sequence is finished (IRQ goes high; see Section 4.1.1), a supply voltage level detection (SVLD) function should be executed by the host. See Section 5.2.18. If there is insufficient battery voltage, the chip should be placed in BPM by the host. BPM may be programmed from any mode, or Standby Mode.

4.2.3 Xtreme / Power-Down Mode

The EM9203 features a mode that draws very little current to minimize power consumption while idle. This host activates this mode from Standby Mode. In Version 11 it is called 'Xtreme Mode'; in Version 12 it is called 'Power-Down Mode'.

4.2.3.1 Xtreme Mode (Version 11 only)

When the EM9203 is in Xtreme Mode (Version 11 only) VDD is decreased from +1.8V to approximately +1.4V to reduce leakage current but retain all register values. In this configuration, the DC/DC converter will support external loads up to 500µA, and so the external host controller should also be configured for minimum power consumption. An increased ripple of approximately 100mV$_{PP}$ is present on VCC1, with a period dependent upon the external load.

4.2.3.2 Power-Down Mode (Version 12 only)

When the EM9203 is in Power-Down Mode (Version 12 only) VDD is decreased from +1.8V to approximately +1.2V to reduce leakage current but retain all register values.

4.2.4 Standby Low-Power Mode

The EM9203 also provides a Standby Low-Power Mode, which is shown as the inner circle of standby mode in Figure 4. In this mode the current consumption of the crystal oscillator is reduced and the main system clock is set to 400kHz. This mode is complementary to the above mentioned Xtreme / Power-Down Mode in that the crystal oscillator continues to run, but at a lower accuracy. This mode returns to Standby Mode more quickly than Xtreme / Power-Down Mode, and can be used to optimize system efficiency.

Standby Low-Power Mode can be activated only from Standby Mode.

4.2.5 Transmit (TX) Mode

In TX Mode, the EM9203 outputs a GFSK-modulated packet to the antenna pins, returns to Standby Mode and sets the interrupt if the interrupt is configured. If auto-acknowledge is turned-on the EM9203 is first set to RX Mode, awaits the auto-acknowledge packet, and then returns to Standby Mode and sets the interrupt. If no auto-acknowledge is received or the auto-acknowledge indicates an error occurred, and then the packet is retransmitted. Several packets can be automatically transmitted sequentially if desired.

TX Mode can be activated only from Standby Mode.

4.2.6 Receive (RX) Mode

In RX Mode, the EM9203 is ready to receive a GFSK-modulated packet from the antenna. After receiving a packet, the interrupt pin is set if the interrupt is configured. If auto-acknowledge is turned on, the EM9203 is set to TX Mode, sends the auto-acknowledge packet, and then returns to RX Mode. Otherwise, it remains in RX Mode.

RX Mode can be activated only from Standby Mode.

4.3 Auto-calibration Mode

The EM9203 frequency synthesizer has an Auto-calibration Mode that must be run before the first RF operation and then periodically by the host. This keeps the channel frequency and GFSK modulator operating within specification. Analog components in this block are sensitive to temperature variation, therefore performance may degrade or the link may fail if not run periodically. Auto-calibration Mode must be entered from channel 19 in Standby Mode. See Section 5.2.6 for programming details.

5. User interface

This section describes information the user needs for programming and interfacing to the EM9203. The major subsections include the digital interface, the programming interface, and register descriptions.

5.1 Digital interface

The EM9203 can be controlled with a 4-wire serial peripheral interface (SPI). The four wires are:

CSN: Chip select (negated)

SCK: Serial clock

SDI: Serial data in to EM9203

SDO: Serial data out of EM9203

Details of the SPI interface are provided in Section 5.1.1.

The EM9203 has a programmable interrupt pin (IRQ). The IRQ pin is activated by selected status flags in the mask registers. The polarity of the IRQ is also programmable. See Section 5.2.2 for programming details.

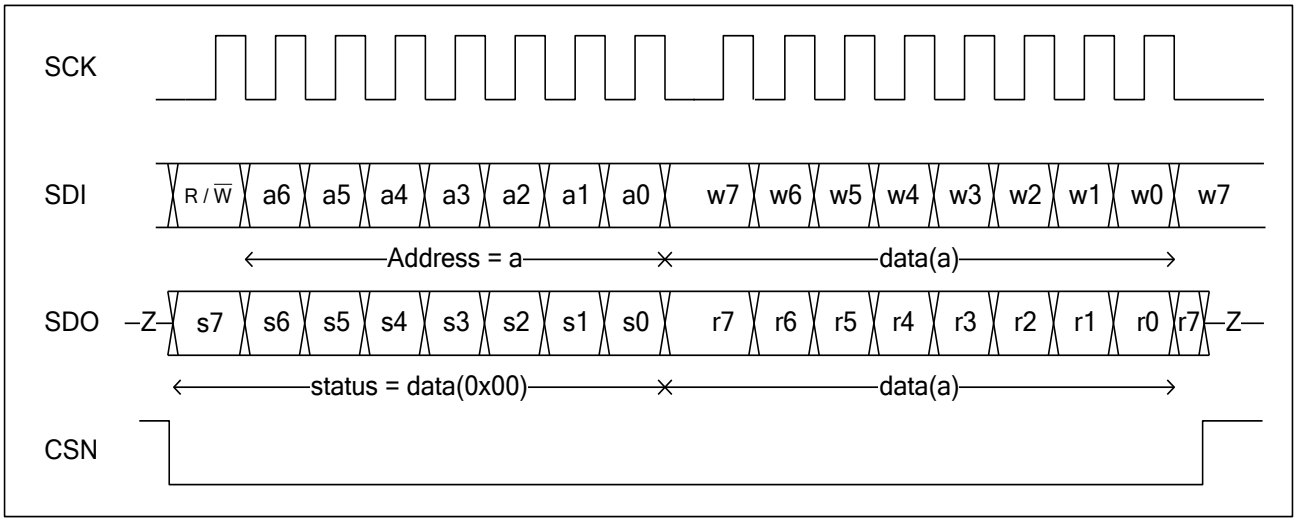
The EM9203 also has pins for direct access to the clock (CK_FPGA pin) and data (DATA_FPGA pin) of the RF transceiver. These pins are useful for implementing, for example, a custom link layer on an external component (e.g., MCU, FPGA, or ASIC) while utilizing the EM9203 GFSK modem and/or the power management features. A more detailed description of using the FPGA pins is available upon special request.

5.1.1 SPI interface

The SPI interface is used to read and write from all of the registers on the EM9203.

A SPI transaction is defined as all of the activity on SCK, SDI and SDO that occurs between one falling edge of CSN and its next rising edge (see Figure 5 below). The first bit of SDI identifies the transaction as a register read (‘1’) or write (‘0’). This is followed by seven address bits and eight data bits. Simultaneously the SDO returns the 8 status bits from **RegInt1Sts**, followed by eight data bits from the requested register. Over this physical interface, the protocol is byte-based. Each byte shall be sent most-significant bit (MSb) first.

Figure 5: SPI transaction structure



Note: The register 0x00 is also directly visible as the status information for each SPI transaction.

A complete transaction requires a multiple of 8 SCK pulses (complete bytes). In the event of incomplete transactions, only the completed bytes will be used to perform the desired action.

The possible actions are:

- Read one or more consecutive register(s) and the status byte (register 0x00). See Figure 6 below.
  This action requires at least two bytes: one byte for address and read order, and at least one byte for reading the desired address.
- Write one or more consecutive register(s) and read the status byte (register 0x00). See Figure 7 below.
  This action requires at least two bytes: one byte for address and write order, and at least one byte for writing at the desired address.
- Read the status byte.
  This action requires one byte.

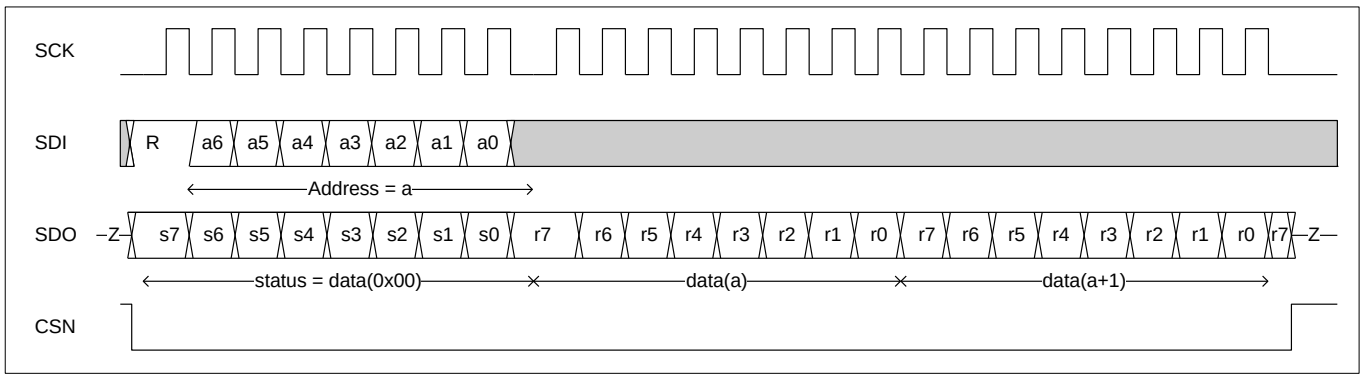


Figure 6: Multi-read SPI transaction

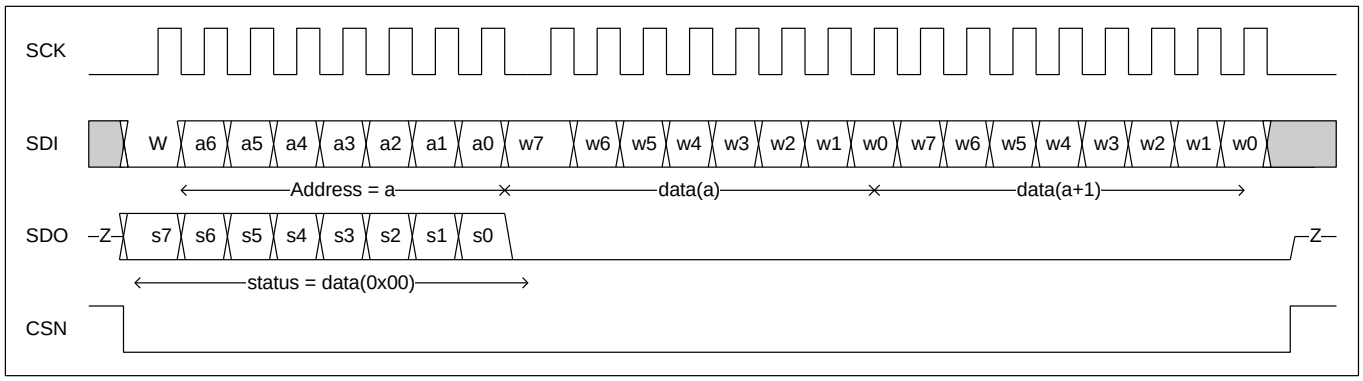


Figure 7: Multi-write SPI transaction

Each change to SDI is latched on the rising edge of SCK, and each change to SDO is available on the falling edge of SCK. A timing diagram is shown in Figure 8. Complete timing specifications are given in Table 10.

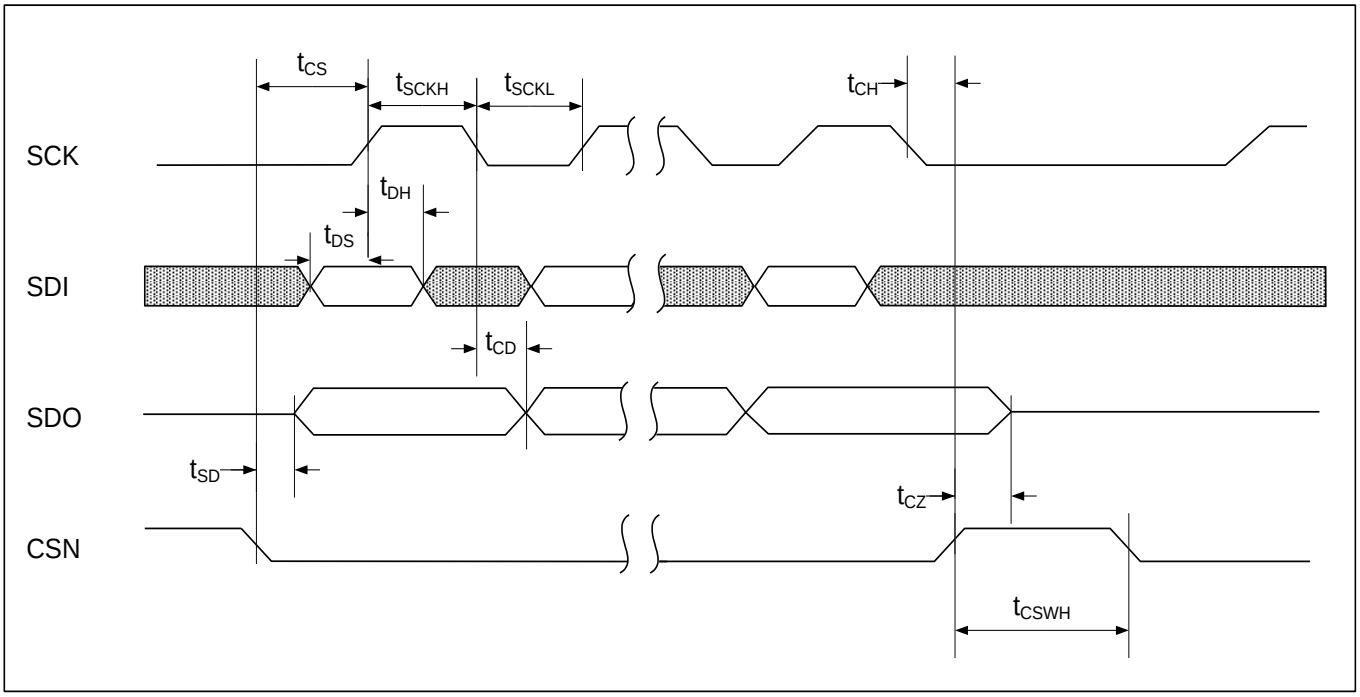


Figure 8: SPI timing diagram

Table 10: SPI timing values, maximum load 15pF

Symbol	Parameters	Min	Max	Units
t_{DS}	SDI to SCK Setup	5		ns
t_{DH}	SCK to SDI Hold	5		ns
t_{SD}	CSN to SDO Valid		30	ns
t_{CD}	SCK to SDO Valid		30	ns
t_{SCKL}	SCK Low Time	40		ns
t_{SCKH} Tsckh	SCK High Time	40		ns
f_{SCK}	SCK Frequency		8	MHz
f_{SCK_LP}	SCK Frequency in Low Power / Xtreme Mode		1	MHz
t_{CS}	CSN to SCK Setup	125		ns
t_{CH}	SCK to CSN Hold	125		ns
t_{CSWH}	CSN Inactive Time	125		ns
t_{CZ}	CSN to SDO High Z		30	ns

Note: It is recommended to minimize SPI activity during RF communications. SPI activity during RF communications (RX or TX Mode) can decrease the quality of communication resulting in a higher packet-error rate.

5.2 Programming interface

The Programming interface section describes how to program the EM9203 by writing to the EM9203 registers. Complete register descriptions can be found in Section 5.4.

5.2.1 POR/Software reset

A power-on-reset (POR) is executed when power is first applied to the EM9203. A software-reset can be executed by consecutively writing '0xB3' and '0x5E' to the **RegSPIReset** register.

After power-up, interrupt **IntStsRstFlg** should be cleared.

After **any** reset, all RF communication setup parameters (RF channel, address, etc.) must be reconfigured, and the PLL auto-calibration cycle must be repeated.

No further initialization sequence is required after reset at this time. Contact EM for the latest required initialization sequence.

5.2.2 Status registers and interrupt control

The EM9203 status bits are stored in the **RegInt1Sts** and **RegInt2Sts** registers. Some status bits indicate completion of an operation, such as changing modes and sending or receiving data. Other status bits indicate that certain error conditions have occurred. The status bits can be polled continuously through the SPI.

Status bits can also trigger an interrupt when the host has properly set the mask registers, **RegInt1Msk** and **RegInt2Msk.** Each status bit has a corresponding mask bit. The IRQ pin will be activated by a status bit if the corresponding mask bit is '1'. If the corresponding mask bit is a '0' then the status bit will not trigger an interrupt. After an interrupt has occurred, the interrupt can be cleared by writing '1' to the status bits to be cleared, and writing '0' to the bits to keep.

The polarity of the IRQ pin can be programmed by writing to the **RegConfig.IRQNeg** bit. After reset, the pin is defined as an active high.

5.2.3 Power management Modes

The power management modes can be accessed through the **RegPower** register:

- Battery Protection Mode can be activated by writing '0x3F' to the **RegPower.BPM** bits
- Xtreme or Power-Down Mode can be activated by writing a '1' to the **RegPower.Xtreme** bit
- Standby Low-Power Mode can be activated by writing a '1' to the **RegPower.LowPwrStdby** bit

Once placed in a power management mode, the EM9203 must be returned to Standby Mode before it can receive or transmit data. This is accomplished by writing '0x00' to the **RegPower** register. Status and interrupt bits are available to signal the end of Xtreme / Power-Down or Standby Low-Power Mode.

5.2.4 Data rate

The EM9203 has a programmable data rate of 1Mbps or 2Mbps for transmission and reception. The 2Mbps data rate not only yields a lower probability of on-air collision due to shorter transmission time, but also lowers the average power consumption when using high TX output power.

The RF data rate is set by **RegRFSetup.RFDR** bit.

To establish communication, both linked devices must be set to the same data rate.

5.2.5 Channel

The channel register sets the center frequency of the transmission channel used by the EM9203. The channel is set by the **RegRFChannel** register. **RFChannel** may be a value between 0 and 39. For programmed values greater than 39, the channel defaults to 39.

The center frequency is defined as:

F_C = 2402 + **RFChannel***2 (MHz)

To establish communication, both linked devices must be set to the same channel. The host can program a channel change, which is effective on a Standby → RX transition.

The spectral width of the channel depends on the data rate. For a data rate of 1Mbps, the channel width is 1MHz. The channel width increases to 2MHz for 2Mbps.

5.2.6 Auto-calibration

Auto-calibration is used to calibrate the analog circuits of the PLL. For correct transmission and reception, the PLL should be calibrated at the desired data rate before the link is used. Auto-calibration must be run on channel 19 in Standby Mode by the host after any chip reset; following auto-calibration, the RF transceiver can be set to any channel.

To request the auto-calibration, set the **RegRFSetup.RFAutoCalib** bit to '1'. This bit is reset to '0' at the end of the auto-calibration. If requested, an IRQ can be generated to signal the end of auto-calibration. The auto-calibration end information is on **RegInt2Sts.IntStsAutoCalEnd** bit and can be masked by **RegInt2Msk.IntMskAutoCalEnd** bit.
The calibration of the PLL may vary if the external conditions change (e.g., temperature), therefore calibration should be repeated periodically. It is recommended to rerun auto-calibration for any change in temperature greater than 5 degrees C.

Due to excessive noise in the calibration procedure, it is recommended to average 4 auto-calibration values. Here is the procedure in pseudo-code:

Step 1) Enter Standby Mode, and set the variable autocal=0

Step 2) Repeat the following instructions 4 times:

Step 2a) Run auto-calibration

Step 2b) Write 0x01 into register 0x3F

Step 2c) autocal+=read(0x3A) & 0x3F

Step 2d) Write 0x00 into register 0x3F

Step 3) autocal = (autocal>>2)

Step 4) Write 0x01 into register 0x3F

Step 5) Write autocal variable into register 0x3A

Step 6) Write 0x00 into register 0x3F

Step 7) Enter RX Mode

Since auto-calibration needs to be run periodically, a running average can be maintained.

Note: The interrupt for the end of auto-calibration also appears during a normal transmit or receive operation to indicate that the PLL has completed its set-up procedure.

5.2.7 Address registers

Each device can have a unique three byte address. For proper communication between two devices the receiving device must set the **RegRxAddr** register to match the transmitting device's **RegTxAddr** register. The **RegRxAddr** and **RegTxAddr** registers can be set to the same value. Although it is possible to set the addresses to any value, optimal operation is achieved when following these two selection rules:

6 < Hamming Weight < 18

3 address bytes must be different

An application note is available upon request which describes this selection process in detail.

5.2.8 Data whitening

The data in the payload can be “whitened” by setting the **RegConfig.WhitDis** bit to ‘0’. Whitening encodes the payload data such that more transitions between ‘0’ and ‘1’ occur in the packet. Whitening is recommended for higher probability of packet reception in the demodulator when a long series of ‘0’s or ‘1’s is present in the payload.

To establish communication, both linked devices must have the same whitening setting.

5.2.9 Auto-acknowledge

Auto-acknowledge functionality is controlled with the **RegACKSetup** register. When the auto-acknowledge capability is enabled (**RegACKSetup.ACKDis**=’0’) an acknowledgement packet is generated based on the result of the data error check. In the event that the data check value is correct, an ACK packet is generated, otherwise a NACK packet is generated. (Refer to Section 6.2 for more information about the data check value.) The amount of time that the transmitter waits for an auto-acknowledgement from the receiver is configured in the **RegACKSetup.ACKTimeout** register.

For proper communication with auto-acknowledge packets, both linked devices should enable the auto-acknowledge feature. For proper communication without auto-acknowledge packets, both linked devices should disable the auto-acknowledge feature.

An auto-acknowledge timing example is shown in Figure 9. The RX unit timing is shown in the bottom three traces, and is enabled before the TX unit, which is shown on the top three traces. The TX sends a packet, which is not received by the RX as indicated by the first red “X”. In this case the TX waits the predefined timeout period as set in the **RegACKSetup.ACKTimeout** register and retransmits the packet. This time the RX receives the packet, transmits and ACK packet, and issues an interrupt indicating a received packet. In this example the ACK packet is not received by the TX as indicated by the second red “X”. After the predefined timeout period, the TX again sends the packet. This packet is received by the RX and it sends an ACK packet, but this time it does not issue an interrupt because the packet has been previously received. This time the ACK packet is received by the TX which issues an interrupt indicating successful transmission of the packet.

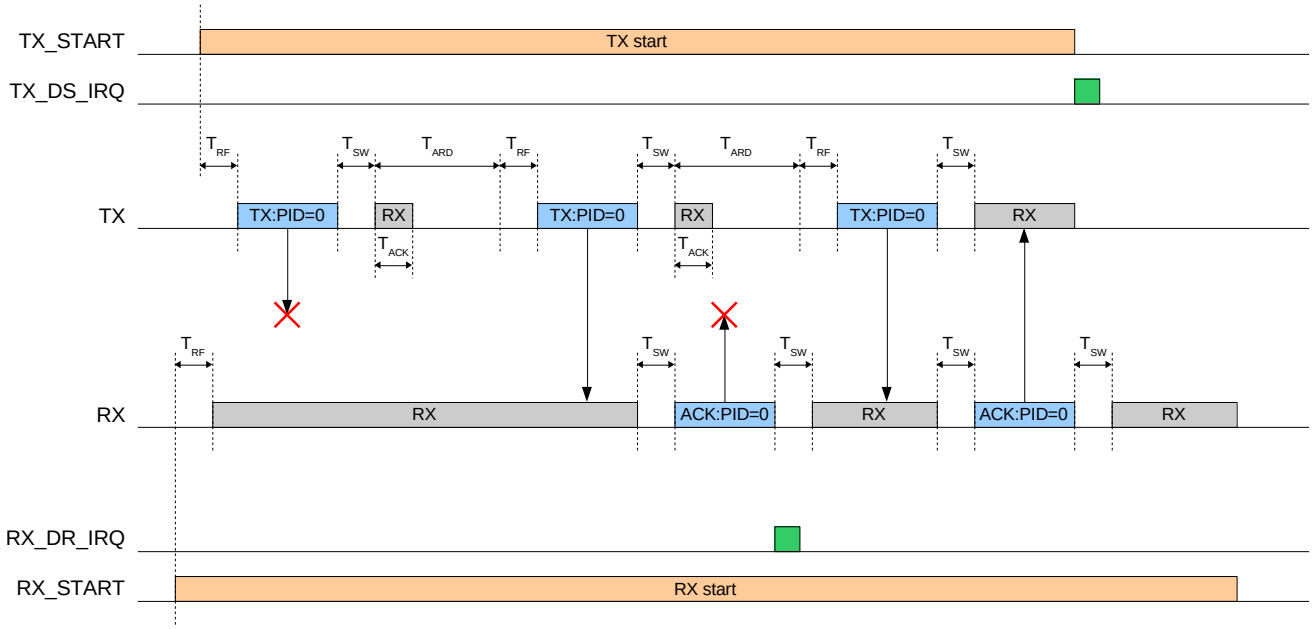


Figure 9: Auto-acknowledge procedure

5.2.10 Auto-retransmit

Auto-retransmit functionality is controlled with the **RegRetrSetup** register. Packets are retransmitted when a NACK packet is received or no auto-acknowledgement packet is received. The auto-retransmit delay is set in the **RegRetrSetup.ARDly** register, and the maximum number of retransmissions is set in the **RegRetrSetup.ARCntMax** register.

The number of packets that are determined lost because an auto-acknowledge was not received may be read from the **RegRetrStatus.LstPckCnt** register. This register can be reset by writing to the **RegRFChannel** register. The number of packets resent because an ACK was not received may be read from the **RegRetrStatus.RsntPckCnt** register. This register is reset when a new transmission begins.

5.2.11 TX power level

The PA output power can be adjusted to one of eight levels as shown in Table 11. These levels are set by **RegRFSetup.RFPwr** register bits. Typical current consumption for each of these power levels is also shown.

Table 11: RF power settings for the EM9203

RF Power Control Bits (**RFPwr[2:0]**)	Output Power	DC Current 1Mbps (mA)	DC Current 2Mbps (mA)
'111'	+3	16.8	17.7
'110'	0	12.6	13.5
'101'	-3	11.4	12.2
'100'	-6	10.4	11.1
'011'	-9	9.6	10.2
'010'	-12	9.2	9.8
'001'	-15	8.8	9.4
'000'	-18	8.6	9.2

Measuring conditions: VCC2 = 2.5V, T=25 °C, load impedance = 200Ω.

5.2.12 External PA control

A control signal for an external Power Amplifier is available if a higher transmit output power is required than the EM9203 can output. This is configured with the **RegRFSetup.ExtPA** register bit and is available on the CK_FPGA pin. When using an external Power Amplifier, the user is required to comply with all ISM band regulations.

5.2.13 TX and RX payload

The transmit payload can be up to 32 bytes and must be written to the **RegTXBuff** register, starting with byte 0. '*PayloadLength*-1', the length in bytes of the transmit payload *minus one,* must be written to the **RegTxPldLen** register.

The receive payload can be up to 32 bytes and can be read from the **RegRXBuff** register, starting with byte 0. '*PayloadLength*-1', the length in bytes of the receive payload *minus one,* can be read from the **RegRxPldLen** register.

5.2.14 TX and RX FIFO

The receiver and transmitter each have a two-element FIFO. Each FIFO element is up to 32 bytes long to contain a complete payload. The transmit FIFO can be accessed by writing to the **RegTXBuff** register. The receive FIFO can be accessed by reading from the **RegRXBuff** register.

The transmit FIFO can have one or both elements loaded prior to transmission. The payloads can be sent with single or separate commands depending on **RegConfig.TxCont** as described in Section 5.2.15. The FIFO can be loaded while simultaneously transmitting another packet. The FIFO pointer must be incremented after each payload is written (**RegFIFOCtrl.TxPtrInc** = '1'). The TX FIFO can be flushed by setting **RegFIFOCtrl.TxFlush** = '1'. The 'full' or 'empty' status of the TX FIFO can be read in the **RegFIFOStatus** register.

The receive FIFO can be read after a packet has been received and the **RegInt1Sts.StsRxDR** (RX data ready) flag is '1'. The RX FIFO pointer must be incremented after reading the payload (**RegFIFOCtrl.RxPtrInc** = '1'). A packet can be read while simultaneously receiving another packet. The RX FIFO can be flushed by setting **RegFIFOCtrl.RxFlush** = '1'. The 'full' or 'empty' status of the RX FIFO can be read in the **RegFIFOStatus** register.

Note: TX FIFO Empty flag is not updated after writing TxPtrInc. RX FIFO Full flag is not updated after writing RxPtrInc. Flags are updated as soon as RF is active.

5.2.15 Transmission flow

This section describes the entire flow for transmitting a packet with the EM9203.

1. Match **RegTxAddr** to the address of the receiver's **RegRxAddr**.
2. Match **RegRxAddr** to the address of the transmitter's **RegTxAddr**.
3. Configure the data rate (**RegRFSetup.RFDR**) and output power (**RegRFSetup.RFPwr**).
4. Configure the channel used (0-39) on **RegRFChannel** register.

5. Set the desired auto-acknowledge behavior:
   a. Enable auto-acknowledge: (**RegACKSetup.ACKDis** = '0').
6. -or-
   a. Disable auto-acknowledge: (**RegACKSetup.ACKDis** = '1').
7. Set the mask for the desired interrupts (on **RegInt1Msk** and **RegInt2Msk**).
8. Write the *PayloadLength*-1 to **RegTxPldLen.TxPldLen**. (*PayloadLength*-1 is the number of payload bytes minus one.)
9. Write 0x40 to **RegFIFOCtrl** to flush the TX FIFO
10. Write the payload data to **RegTxBuf[0:PayloadLength-1]**.
11. Increment the TX FIFO pointer by writing '1' to **RegFIFOCtrl.TxPtrInc**.
12. If the EM9203 is in Xtreme / Power-Down Mode, set **RegPower.Xtreme** to '0' to exit the Xtreme / Power-Down Mode. Poll the interrupt bit (**RegInt1Sts.IntStsXmEnd** = '1') or wait for IRQ to verify that the EM9203 is in Standby Mode.
13. Set the **RegConfig.TxRxN** and **RegConfig.Start** bits to '1' and set the desired whitening behavior (**RegConfig.WhitDis**).
14. The EM9203 will:
    a. Power up the RF transceiver system in the Transmit Mode on the specified frequency.
    b. Send the packet in one burst at the given data rate.
15. If auto-acknowledge is enabled, the EM9203 will set the RF transceiver to Receive Mode and wait for an acknowledgement packet.
16. Once communication is initiated, the host is allowed to send other data.
17. When auto-acknowledge is enabled:
    a. If the EM9203 receives an ACK packet, it generates the **RegInt1Sts.StsTxDS** interrupt.
    b. If the EM9203 doesn't receive an ACK packet, or it receives a NACK packet, it increments the auto-retransmission counter. If the counter is less than the number of maximum allowed retransmissions, then the EM9203 retransmits, otherwise it generates the **RegInt1Sts.StsMaxRT** interrupt.
18. When auto-acknowledge is disabled:
    a. The EM9203 immediately generates the **RegInt1Sts.StsTxDS** interrupt after sending the packet.
19. If the bit **RegConfig.TxCont** = '0', the system sets the **RegConfig.Start** bit to '0' and goes to Standby Mode. If the bit **RegConfig.TxCont** = '1' and the TX FIFO is not empty the system transmits the next packet stored in the TX FIFO.

5.2.16 Reception flow

This section describes the entire flow for receiving data on the EM9203.

1. Match **RegTxAddr** to the address of the receiver's **RegRxAddr**.
2. Match **RegRxAddr** to the address of the transmitter's **RegTxAddr**.
3. Configure the data rate (**RegRFSetup.RFDR**).
4. Configure the channel used (0-39) on **RegRFChannel** register.
5. Set the desired auto-acknowledge behavior:
   a. Enable auto-acknowledge: (**RegACKSetup.ACKDis** = '0').
6. -or-
   a. Disable auto-acknowledge: (**RegACKSetup.ACKDis** = '1').
7. Set the mask for the desired interrupts (on **RegInt1Msk** and **RegInt2Msk**).
8. If the EM9203 is in Xtreme / Power-Down Mode, set **RegPower.Xtreme** to '0' to exit the Xtreme / Power-Down Mode. Poll the interrupt bit (**RegInt1Sts.IntStsXmEnd** = '1') or wait for IRQ to verify that the EM9203 is in Standby Mode.
9. Set the **RegConfig.TxRxN** bit to '0' and the **RegConfig.Start** bit to '1'.
10. Set the desired whitening behavior (**RegConfig.WhitDis**).
11. The EM9203 will:
    a. Power up the RF transceiver system in Receive Mode on the specified frequency.
    b. Listen for incoming communication.

12. When auto-acknowledge is enabled:
    a. If a packet with matching address has been received, the EM9203 will go into Transmit Mode to send an ACK or NACK, depending on the result of the data error check, then return to Receive Mode.
13. If the packet received was valid (correct address and no errors detected):
    a. The payload data is stored in the RX FIFO.
    b. The payload length *minus one* is written to the **RegRxPldLen** register.
    c. **RegInt1Sts.StsRxDR** is set to '1'.
    d. The IRQ pin is set if **RegInt1Msk.IntMskRxDR** = '1'.
14. The host microcontroller can stop the reception by setting the **RegConfig.Start** bit to '0'.
15. After a valid packet has been received, read the *PayloadLength-1* of the received packet from the **RegRxPldLen** register. (*PayloadLength-1* is the number of payload bytes minus one)
16. Read the received packet from the **RegRxBuf[0:*PayloadLength-1*]**.
17. Increment the RX FIFO pointer by setting **RegFIFOCtrl.RxPtrInc** to '1'. Note RX stops if RX FIFO is full.

5.2.17 Received Signal Strength Indicator (RSSI)

A received signal strength indicator (RSSI) is available through the **RegRFRSSI** register.

The average power on the channel can be measured if **RegRFRSSI.RFRSSIMode** is set to '0'. This is useful for determining if there is other RF activity on the channel (e.g., WiFi).

First enable the RSSI circuit:

Step 1) Write 0x00 to register **0x3F**

Step 2) Write 0xB4 to register 0x1B

Step 3) Write 0x5D to register 0x1B

This only needs to be done once at power up.

Then measurement is triggered with a special sequence:

Step 4) Write 0x01 to register **0x3F**

Step 5) Write 0x48 to register **0x22**

Step 6) Write 0x00 to register **0x3F**

Step 7) Write 0x10 to register **RegRFRSSI**

Step 8) Write 0x80 to register 0x1C

Step 9) Wait 12us

Step 10) Read **RegRFRSSI.RFRSSIOut**

Step 11) Write 0x00 to register **RegRFRSSI.RFRSSIEn**

Step 12) Write 0x00 to register 0x1C

First, set **RegRFRSSI.RFRSSIMode** to '0' and set **RegRFRSSI.RFRSSIEn** to '1'. Trigger the one-shot measurement. The measurement then takes 12us. Then read the 4-bit result of the RSSI power measurement from **RegRFRSSI.RFRSSIOut.** Finally, reset the RSSI and one-shot. Repeat the procedure for subsequent measurements.

The burst power of a received packet can be measured if **RegRFRSSI.RFRSSIMode** is set to '1'. The 4-bit result of the RSSI power measurement is available on **RegRFRSSI.RFRSSIOut** after a packet is received.

The relationship between the applied RF power, P_{IN} at the antenna pins and the value given by the RSSI can be expressed as:

P_{IN} [dBm] = -110dBm + **RFRSSIOut** * 6dB, for P_{IN} < -50 dBm.

The accuracy of the RSSI is not guaranteed.

5.2.18 Supply Voltage Level Detection (SVLD)

The EM9203 features the capability of supply monitoring on several nodes in the system (VBAT, VCC2, and VDD). The host controller can initiate a measurement by sending a SPI command, which compares the actual node voltage with a predefined level. After the measurement is completed, the result can be read back from the corresponding SPI register. The **RegInt1Sts.IntStsPwrLow** flag can indicate either the completion of the measurement, or that the measurement was below the selected level. The levels are indicated in Table 12. The levels have an accuracy of +/-10%.

Table 12: Nodes available for SVLD monitoring

EM9203 Version	Supply	Level [V]	Function
(11) DC/DC	VBAT	0.82	BPM battery monitoring (see Section 4.2.2)
	VBAT	0.92	BPM early warning
	VBAT	1.12	Battery low detection (1.5V batteries)
	VBAT	1.25	Battery low detection, early warning (1.5V batteries)
(11) and (12)	VDD	1.43	N/A (used for power-check at start-up)
(12) no DC/DC	VCC2	2.00	N/A (used for chip internal monitoring)
	VCC2	2.24	Battery low detection (3V batteries)
	VCC2	2.49	Battery low early warning (3V batteries)

To utilize the SVLD feature:

1. Select the supply to monitor:
   a. Set **RegSVLD.SVLDSelSrc**
      '00' – VDD Voltage
      '01' – VCC2 Voltage
      '10' – VBAT Voltage
2. Select the measurement threshold level:
   a. Set **RegSVLD.SVLDSelLvl**
3. '000' – 0.82V
   '001' – 0.92V
   '010' – 1.12V
   '011' – 1.25V
   '100' – 1.43V
   '101' – 2.00V
   '110' – 2.24V
   '111' – 2.49V
4. Select the low power interrupt status flag (**RegInt1Sts.IntStsPwrLow**) behavior:
   a. **RegSVLD.SVLDIntOnFail** = '0' – flag indicates measurement completed

-or-

   b. **RegSVLD.SVLDIntOnFail** = '1' – flag indicates measurement completed and is below selected level
5. Initiate the measurement:
   a. Set **RegSVLD.SVLDStart** = '1'
6. If **RegSVLD.SVLDIntOnFail** = '0', wait for measurement to be completed:
   a. Monitor **RegInt1Sts.IntStsPwrLow** until it equals '1' , or use interrupt by setting **RegInt1Msk.IntMskPwrLow**
   b. Read the result from the register **RegSVLD.SVLDResult**, if needed
7. If **RegSVLD.SVLDIntOnFail** = '1':
   a. Monitor **RegInt1Sts.IntStsPwrLow** and if it equals '1' take appropriate action (e.g., enter BPM, etc.)

Several measurements should be taken to minimize any inaccuracy due to noise.

5.2.19 VCO Bias Control

The VCO bias current can be reduced in 1Mbps for lower overall RX and TX power consumption. In order to do this a special sequence is required:

Step 1) Write 0x01 to register **0x3F**

Step 2) Write 0x66 to register **RegTstRFCtatCtrl**

Step 3) Write 0x00 to register **0x3F**

In order to return the VCO bias to the correct current for 2Mbps operation, the following sequence can be used:

Step 1) Write 0x01 to register **0x3F**

Step 2) Write 0x76 to register **RegTstRFCtatCtrl**

Step 3) Write 0x00 to register **0x3F**

Alternately, the correct value is placed in the register on software reset.

5.3 DC/DC converter

The external host controller and sensor interface may require a higher voltage for some measurements and signal processing prior to sending data to the EM9203; therefore the DC/DC output voltage can be set by the host temporarily to a higher value by changing **RegDCDC.DCDCLvl**.

Note: It is not recommended to externally draw a large amount of current from the DC/DC converter at the same time that the on-air link is running.

5.4 Register descriptions

In this section all basic functionality and reset values for relevant registers of the EM9203 are described. Any register not specifically mentioned here is reserved and its contents are set to '0x00'. In the event that an application must write to a reserved register, it is mandatory to write '0x00'.

5.4.1 Status Register 1

Table 13: **RegInt1Sts** (0x00)

Mnemonic	Bit	Type	Reset Value	Description
IntStsRxDR	7	R/W	0	RX data received
IntStsTxDS	6	R/W	0	TX data sent
IntStsMaxRT	5	R/W	0	Maximum number of TX retransmission exceeded
IntStsPLLNoLock	4	R/W	0	PLL not locked after entering RX or TX Mode
IntStsPckError	3	R/W	0	Packet error during reception
IntStsPwrLow	2	R/W	0	SVLD measurement end
IntStsXTALHiPwr	1	R/W	0	Exit from Standby Low-Power Mode completed
IntStsXmEnd	0	R/W	0	Exit from Xtreme / Power-Down Mode completed

5.4.2 Status Register 2

Table 14: **RegInt2Sts** (0x01)

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7:2	-	0x00	Only 0x00 allowed
IntStsRstFlg	1	R/W	0	Power-up procedure completed
IntStsAutoCalEnd	0	R/W	0	Auto-calibration procedure completed, also indicates that the PLL has completed its set-up procedure prior to transmission or reception

5.4.3 Interrupt Mask Register 1

This register allows the host to choose which status bits trigger an interrupt in the IRQ pin. A '1' value in the mask register bit enables the interrupt due to the corresponding status bit in **RegInt1Sts** register. A '0' value masks the interrupt.

Table 15: **RegInt1Msk** (0x02)

Mnemonic	Bit	Type	Reset Value	Description
IntMskRxDR	7	R/W	0	Interrupt mask – RX data ready
IntMskTxDS	6	R/W	0	Interrupt mask – TX data sent
IntMskMaxRT	5	R/W	0	Interrupt mask – Maximum retransmissions exceeded
IntMskPLLNoLock	4	R/W	0	Interrupt mask – PLL not in lock
IntMskPckError	3	R/W	0	Interrupt mask – Packet error
IntMskPwrLow	2	R/W	0	Interrupt mask – Power check measurement ended
IntMskXTALHiPwr	1	R/W	0	Interrupt mask – End of Standby Low-Power Mode
IntMskXmEnd	0	R/W	0	Interrupt mask – End of Xtreme / Power-Down Mode

5.4.4 Interrupt Mask Register 2

This register allows the host to choose which status bits trigger an interrupt in the IRQ pin. A '1' value in the mask register bit enables the interrupt due to the corresponding status bit in **RegInt2Sts** register. A '0' value masks the interrupt.

Table 16: **RegInt2Msk** (0x03)

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7:1	-	0x00	Only 0x00 allowed.
IntMskAutoCalEnd	0	R/W	0	Interrupt mask – End of auto-calibration

5.4.5 Configuration Register

Table 17: **RegConfig** (0x04)

Mnemonic	Bit	Type	Reset Value	Description
IRQNeg	7	R/W	0	IRQ active level definition ('0' means active high)
Reserved	6	-	0x00	Only 0x00 allowed
WhitDis	5	R/W	0	Disable the RX Whitener
Reserved	4	-	0	Only 0x00 allowed
Reserved	3	R/W	0	Only 0x00 allowed
TxCont	2	R/W	0	Transmit entire FIFO in continuous mode
Start	1	R/W	0	RF Transceiver start
TxRxN	0	R/W	1	RF Transceiver mode: '0' – RX Mode '1' – TX Mode

5.4.6 Power Management Register

Table 18: **RegPower** (0x05)

Mnemonic	Bit	Type	Reset Value	Description
BPM	7:2	R/W	0	Battery Protection Mode Write '0x3F' to activate BPM. Read always returns '0x00'
Xtreme	1	R/W	0	Xtreme Mode on/off
LowPwrStdby	0	R/W	0	Standby Low-Power Mode on/off

5.4.7 RF Setup Register

Table 19: **RegRFSetup** (0x06)

Mnemonic	Bit	Type	Reset Value	Description
ExtPA	7	R/W	0	Enable external PA control signal on CK_FPGA
Reserved	6	-	0	Only '0' allowed
RFAutoCalib	5	R/W	0	Start PLL auto-calibration procedure
Reserved	4	R/W	1	Only '1' allowed
RFDR	3	R/W	1	Data rate: '0' – 1Mbps '1' – 2Mbps
RFPwr	2:0	R/W	'110'	Set RF output power in TX Mode: '000' – -18dBm '001' – -15dBm '010' – -12dBm '011' – -9dBm '100' – -6dBm '101' – -3dBm '110' – 0dBm '111' – +3dBm

5.4.8 RF Channel Register

Table 20: **RegRFChannel** (0x07)

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7:6	-	0x00	Only '0x00' allowed
RFChannel	5:0	R/W	0x00	Device channel (maximum 39)

5.4.9 RF Timing Register

Table 21: **RegRFTiming** (0x08)

Mnemonic	Bit	Type	Reset Value	Description
RFStUpTim	7:4	R/W	0xA	RF start-up time. (150µs)
RFSwTim	3:0	R/W	0xD	RF RX ↔ TX switching time. (150µs)

5.4.10 RF RSSI Register

Table 22: **RegRFRSSI** (0x09)

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7:6	-	0x00	Only '0x00' allowed
RFRSSIMode	5	R/W	0	'0' for average power, '1' for packet burst power
RFRSSIEn	4	R/W	0	Received signal strength indicator (RSSI) enable
RFRSSIOut	3:0	R	0x0	Result of RSSI power measurement

5.4.11 Auto-Acknowledgement Setup Register

Table 23: **RegACKSetup** (0x0B)

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7:5	-	0x00	Only 0x00 allowed
ACKDis	4	R/W	0	Auto-acknowledge disable
ACKTimeout	3:0	R/W	0xD	Timeout for waiting for auto-acknowledge: '0111' – 100µs '1000' – 110µs '1001' – 120µs '1010' – 130µs '1011' – 140µs '1100' – 150µs '1101' – 160µs (reset value) '1110' – 170µs '1111' – 180µs

5.4.12 Auto-Retransmit Register

Table 24: **RegRetrSetup** (0x0C)

Mnemonic	Bit	Type	Reset Value	Description
ARDly	7:4	R/W	0x7	Auto-retransmit delay: '0x0' – Wait for 250µs '0x1' – Wait for 500µs '0x2' – Wait for 750µs ..... '0x7' – Wait for 2000µs (reset value) ..... '0xF' – Wait for 4000µs (Delay from end of transmission to start of the next transmission)
ARCntMax	3:0	R/W	0x3	Maximum number of allowed auto-retransmit attempts: '0x0' – Retransmit disabled '0x1' – Up to 1 retransmit ..... '0xF' – Up to 15 retransmits

5.4.13 Auto-Retransmit Status Register

Table 25: **RegRetrStatus** (0x0D)

Mnemonic	Bit	Type	Reset Value	Description
LstPckCnt	7:4	R	0x0	Count of lost packets (ACK was not received). The counter is overflow protected to 15, and holds at max until reset. The counter is reset by writing **RegRFChannel.RFChannel**
RsntPckCnt	3:0	R	0x0	Count of packets resent because ACK was not received; the counter is reset when transmission of a new packet starts

5.4.14 RX Address Register

The Receive Mode address register is three bytes wide.

Table 26: **RegRxAddr** (0x0E to 0x010)

Address	Mnemonic	Bit	Type	Reset Value	Description
0x0E	**RxAddrB0**	7:0	R/W	0x5B	Address of this device (Byte 0)
0x0F	**RxAddrB1**	7:0	R/W	0x34	Address of this device (Byte 1)
0x10	**RxAddrB2**	7:0	R/W	0x12	Address of this device (Byte 2)

5.4.15 TX Address Register

The peer address in transmit mode is set by this register and is three bytes wide.

Table 27: **RegTxAddr** (0x11 to 0x13)

Address	Mnemonic	Bit	Type	Reset Value	Description
0x11	**TxAddrB0**	7:0	R/W	0x5B	Address of the peer device (Byte 0)
0x12	**TxAddrB1**	7:0	R/W	0x34	Address of the peer device (Byte 1)
0x13	**TxAddrB2**	7:0	R/W	0x12	Address of the peer device (Byte 2)

5.4.16 TX Payload Length Register

Table 28: **RegTxPldLen** (0x14)

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7:5	-	0x0	Only '0x0' allowed
TxPldLen	4:0	R/W	0x00	*PayloadLength-1*: Number of bytes to be transmitted minus one

5.4.17 RX Payload Length

Table 29: **RegRxPldLen** (0x15)

Mnemonic	Bit	type	Reset Value	Description
Reserved	7:5	-	0x0	Only '0x0' allowed
RxPldLen	4:0	R/W	0x00	*PayloadLength-1*: Number of bytes received minus one

5.4.18 FIFO Control Register

Table 30: **RegFIFOCtrl** (0x16)

Mnemonic	Bit	Type	Reset Value	Description
TxPtrInc	7	W	0	Increment pointer in TX FIFO
TxFlush	6	W	0	Flush TX FIFO
RxPtrInc	5	W	0	Increment pointer in RX FIFO
RxFlush	4	W	0	Flush RX FIFO
Reserved	3:0	-	0x0	Only '0x0' allowed

5.4.19 FIFO Status Register

Table 31: **RegFIFOStatus** (0x17)

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7:4	-	0x0	Only '0x0' allowed
RxFull	3	R	0	RX FIFO full
RxEmpty	2	R	1	RX FIFO empty
TxFull	1	R	0	TX FIFO full
TxEmpty	0	R	1	TX FIFO empty

5.4.20 SVLD Register

Table 32: **RegSVLD** (0x18)

Mnemonic	Bit	Type	Reset Value	Description
SVLDResult	7	R	0	SVLD result
SVLDStart	6	R/W	0	Start SVLD measurement
SVLDIntOnFail	5	R/W	0	Defines the meaning of **RegInt1Sts.IntStsPwrLow**: '0' - measurement completed '1' – measurement completed and below selected level
SVLDSelSrc	4:3	R/W	0x0	Select the source measured: '00' – VDD Voltage '01' – VCC2 Voltage '10' – VBAT Voltage '11' – VDD Voltage
SVLDSelLvl	2:0	R/W	0x0	Select SVLD level: '000' – 0.82V '001' – 0.92V '010' – 1.12V '011' – 1.25V '100' – 1.43V '101' – 2.00V '110' – 2.24V '111' – 2.49V

5.4.21 DC/DC Control Register

Table 33: **RegDCDC** (0x19)

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7:2	-	0x00	Only 0x00 allowed
DCDCLvl	1:0	R/W	0x1	DC/DC converter output level: '00' – 2.10V '01' – 2.20V (reset value) '10' – 2.75V '11' – 2.90V

5.4.22 SPI Reset Register

Table 34: **RegSPIReset** (0x1A)

Mnemonic	Bit	Type	Reset Value	Description
SPIReset	7:0	R/W	0x00	Consecutively write value '0xB3' then value '0x5E' to generate a SPI reset. All registers return to reset values.

5.4.23 Transmit Payload Register: RegTxBuf (0x40 to 0x5F)

The address range 0x40 to 0x5F is the TX payload register (32 bytes). Each value can be read or written independently or in a sequence (multi-read or multi-write transaction). Each register is eight bits wide with read/write access. There is no reset value, thus the initial values are undetermined.

5.4.24 Receive Payload Register: RegRxBuf (0x60 to 0x7F)

The address range 0x60 to 0x7F is the RX payload register (32 bytes). Each value can be read independently or in a sequence (multi-read transaction). Each register is eight bits wide with read-only access. There is no reset value, thus the value is undetermined prior to initial packet reception.

5.4.25 VCO Bias Register

Table 35: **RegTstRFCtatCtrl** (0x2C)*

Mnemonic	Bit	Type	Reset Value	Description
Reserved	7	-	0	Only 0 allowed
TstRFCtatCtrl	6:0	R/W	0x76	VCO Bias Level: 2 Mbps – 0x76 (reset value) 1 Mbps* – 0x66 – must be programmed

*Note: A special sequence is required to write to **RegTstRFCtatCtrl.** See Section 5.2.19.

5.5 TX CW Mode

For ETSI / FCC testing it is necessary to put the transmitter in CW mode. To enter TX CW mode execute the following sequence:

Step 1) Run auto-calibration, setup channel, data-rate, etc.

Step 2) Write 0xB4 to register 0x1B

Step 3) Write 0x5D to register 0x1B

Step 4) Write 0x01 to register 0x3F

Step 5) Write 0x58 to register 0x22

After this sequence data can be applied on DATA_FPGA pin at the configured data-rate. No clock is needed as the data is resynchronised on-chip.

To exit TX CW Mode issue the following sequence:

Step 1) Write 0x00 to register 0x3F

Step 2) Execute software reset as in Section 5.2.1.

6. Packet information

The following details on the packet are provided for informational purposes only. Knowledge of the information contained here is not necessary for proper usage of the EM9203.

6.1 Packet format

Each packet contains the following information:

Preamble	Address	Flags	Payload 1-32 bytes	CRC

Table 36: Packet format

Packet Information	Length	Description
Preamble	1 byte	The preamble defines the start of the packet The preamble is “01010101” if the address LSB is 0 The preamble is “10101010” if the address LSB is 1 The preamble is removed from the data stream
Address	3 bytes	The address field contains the address of the receiver The address is 3 bytes long See Section 5.2.7 for details on choosing a proper address.
Flags	1 byte	The flag field contains information about the packet 2 bits for packet identification (PID) 1 bit for packet type: ‘0’ for data packet ‘1’ for ACK packet 5 bits for payload length
Payload	1-32 bytes	Data
CRC result	2 bytes	Cyclic Redundancy Check result The polynomial check is $x^{16} + x^{12}+x^5+1$ (CCITT-X.25)

Multi-byte data (including the address) are always sent with the LSByte first. For each byte, the LSBit is sent first.

The structure of the auto-acknowledge packet is similar to the data packet except that no data is present.

Preamble	Address	Flags	CRC

This packet acts as an ACK or NACK according to the check value. If the check value received is different than the one sent, this packet is a NACK otherwise it is an ACK.

6.2 Cyclic Redundancy Check (CRC)

The EM9203 performs a cyclical redundancy check (CRC) to determine if any errors have occurred during data transmission. The two-byte check value is calculated by the transmitting device and is included at the end of each packet. The receiving device also performs the CRC and compares the transmitted check value to the calculated value. Any difference indicates an error in the packet. The polynomial check is $x^{16}+ x^{12}+x^5+1$ (CCITT-X.25).

6.3 Packet identifier

Each packet contains a two-bit packet identifier (PID) field. The PID and CRC result fields are used by the receiving device to determine whether a packet is re-sent or new. The PID will prevent the receiving device from sending the same payload more than once to the host controller. The scheme for PID generation and detection is depicted in Figure 10.

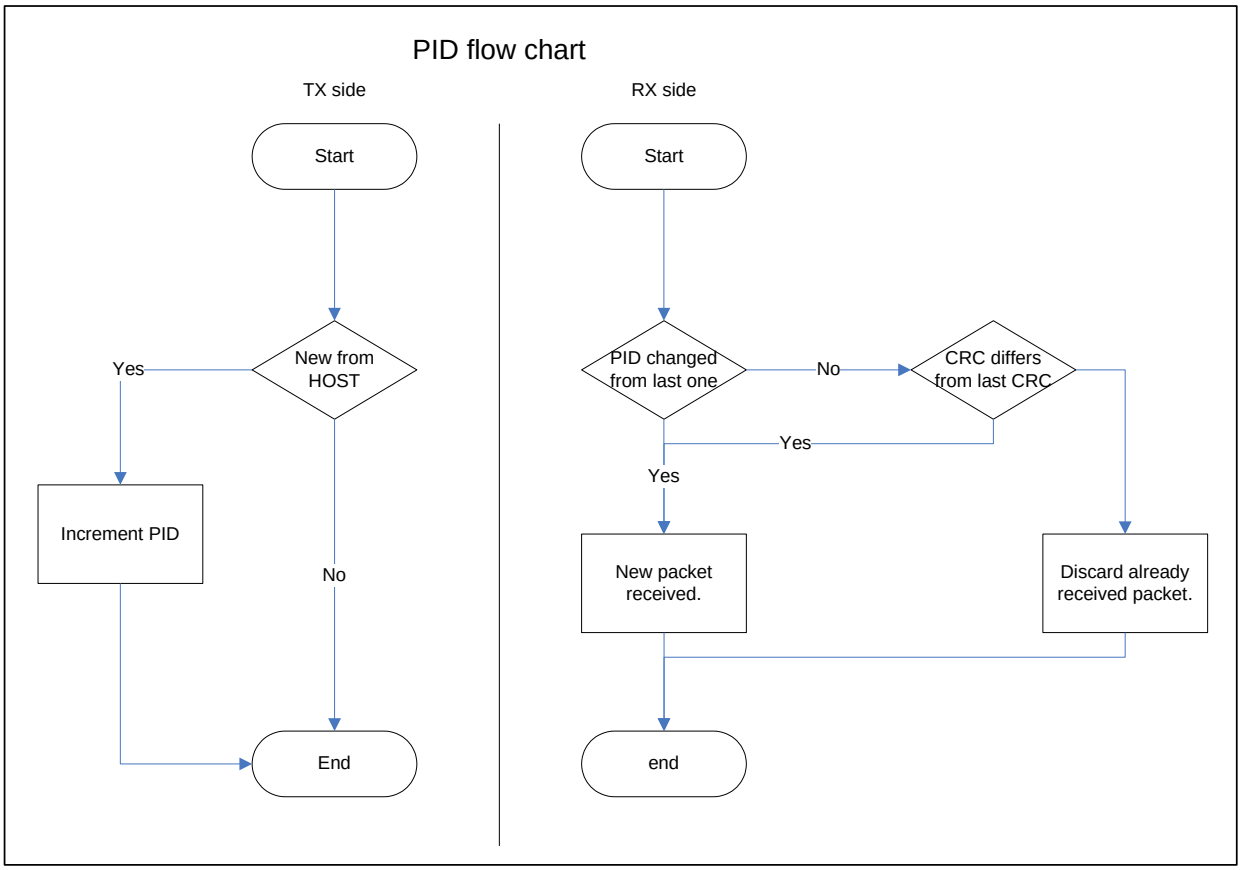


Figure 10: PID generation and detection

7. Versions and ordering information

The EM9203 is available in two different versions as summarized in

Table 37 below. Each version is available in bare die or package format. The two versions have the same pad locations and pin-out.

Table 37: Version information

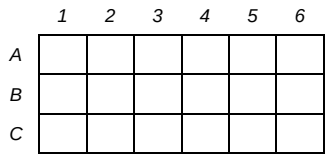
Version	Description	Features	Applications / Comments
11	DC/DC step-up converter	2.4GHz transceiver with on-chip DC/DC step-up converter for 1.5V single batteries - 26MHz crystal required - 1Mbps and 2Mbps on-air data rate - Xtreme Mode for DC/DC - Battery Protection Mode	RF application where only one 1.5V battery is available (e.g., wireless mouse)
12	No DC/DC – direct battery supply	2.4GHz transceiver for direct 3V battery supply (or external regulator) - 26MHz crystal required - 1Mbps and 2Mbps on-air data rate - Power-Down Mode	Wireless applications relying on 3V button cells (e.g., in watches) or where an external regulator is available (e.g., USB dongle)

Table 38: Ordering information

Version	Ordering Code	Description	Packaging	Container
11	EM9203 V11LF28D *	1 / 2Mbps Transceiver with DC/DC	MLF28	Tray
12	EM9203 V12LF28D	1 / 2Mbps Transceiver without DC/DC	MLF28	Tray
11	EM9203 V11LF28B *	1 / 2Mbps Transceiver with DC/DC	MLF28	Tape and Reel
12	EM9203 V12LF28B	1 / 2Mbps Transceiver without DC/DC	MLF28	Tape and Reel
11	EM9203 V11WW7 *	1 / 2Mbps Transceiver with DC/DC	Bare Die	Wafer Container
12	EM9203 V12WW7	1 / 2Mbps Transceiver without DC/DC	Bare Die	Wafer Container

* Note: DC-DC version available upon special request

7.1 Package marking



First Line:

- A1-A6: “EM9203”

Second Line:

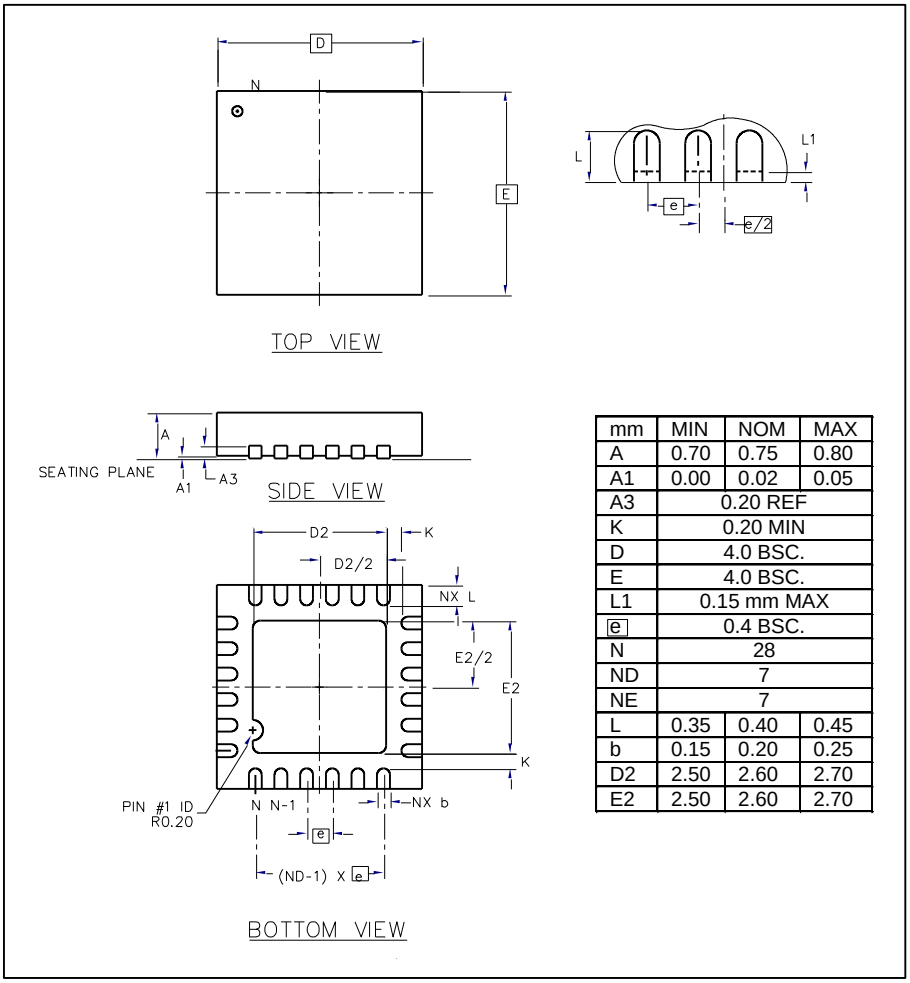
- B1-B3: Version – “011” with DC/DC, “012” without DC/DC
- B4: Year of Assembly
- B5: Assembly House Code
- B6: Blank

Third Line:

- C1-C6: Diffusion Lot Number (without year of diffusion)

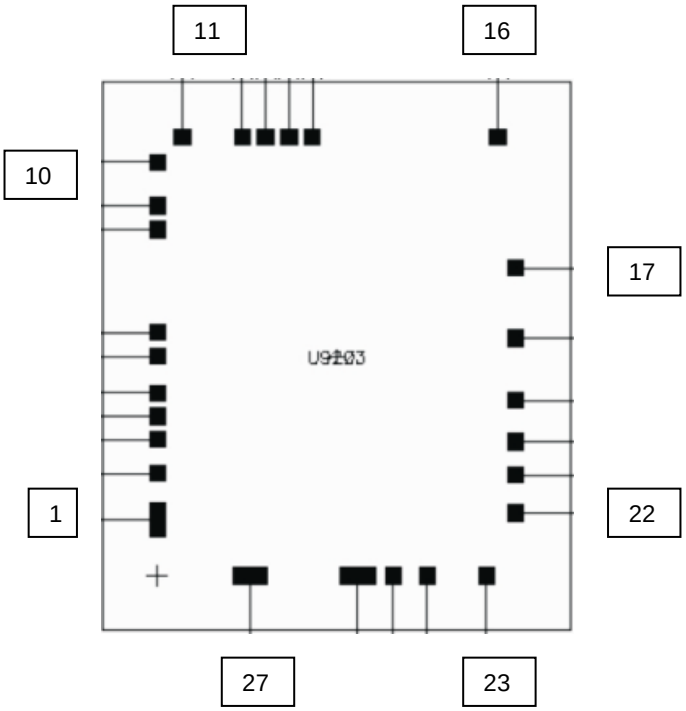
8. Package information

MLF28 4mm x 4mm



mm	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20 REF	
K		0.20 MIN	
D		4.0 BSC.	
E		4.0 BSC.	
L1		0.15 mm MAX	
e		0.4 BSC.	
N		28	
ND		7	
NE		7	
L	0.35	0.40	0.45
b	0.15	0.20	0.25
D2	2.50	2.60	2.70
E2	2.50	2.60	2.70

9. Pad locations



Pin Name	Pad N°	Width [µm]	Length [µm]	X [µm]	Y [µm]
p_vss_dcdc	1	146	68	0	239.56
p_vss_pr	2	68	68	0	438.53
p_vss	3	68	68	0	581.79
p_vdd	4	68	68	0	681.79
p_sck	5	68	68	0	781.79
p_sdi	6	68	68	0	939.19
p_sdo	7	68	68	0	1039.19
p_irq	8	68	68	0	1481.15
p_data_fpga	9	68	68	0	1581.13
p_ck_fpga	10	68	68	0	1767.37
p_cs	11	68	68	106.47	1877.84
p_avss_pr	12	68	68	362.85	1877.84
p_xtal2	13	68	68	462.85	1877.84
p_xtal1	14	68	68	562.84	1877.84
p_avss_pll1	15	68	68	662.84	1877.84
p_avss_pr	16	68	68	1457.22	1877.84
p_avss_rf	17	68	68	1533.84	1316.67
p_antp	18	68	68	1533.84	1016.67
p_antn	19	68	68	1533.84	750.21
p_avss_pa	20	68	68	1533.84	574.04
p_avdd_pa	21	68	68	1533.84	429.44
p_vbat	22	68	68	1533.84	267.69
p_bias_r	23	68	68	1408.31	0
p_vcc2	24	68	68	1154.42	0
p_avss_pll2	25	68	68	1009.85	0
p_vcc1	26	146	68	857.49	0
p_sw_dcdc	27	146	68	396.70	0

10. DC/DC converter typical operating characteristics

This chapter describes the typical operating characteristics of the DC/DC converter available on the EM9203 Version 11.

10.1 DC/DC converter efficiency

The DC/DC converter efficiency is evaluated by loading its output VCC1 with an external current I_{Lext} for a fixed input (battery) voltage applied to VBAT.

The efficiency η is given by:

$\eta := P_{OUT}/P_{IN} = V(VCC1)* I_{Lext} / (V(VBAT)*I_{BAT})$

The efficiency of the DC/DC converter in Standby Mode and Xtreme Mode is plotted in the graphs below.

Note: These measurements include the internal chip current consumption (from VCC2).

Setup: EM9203-Version 11 configured as described in Section 11.1, with L1 = 10µH / ESR=110mΩ, C3=22µF (Ceramic X5R).

10.1.1 Standby Mode efficiency

Figure 11 shows the measured DC/DC converter efficiency versus the fully available external load current (0 to 100mA), when the EM9203 is Standby Mode (internal chip current consumption is approximately 140µA). Measurement data is plotted for VBAT = {0.85V, 1.2V, and 1.4V}.

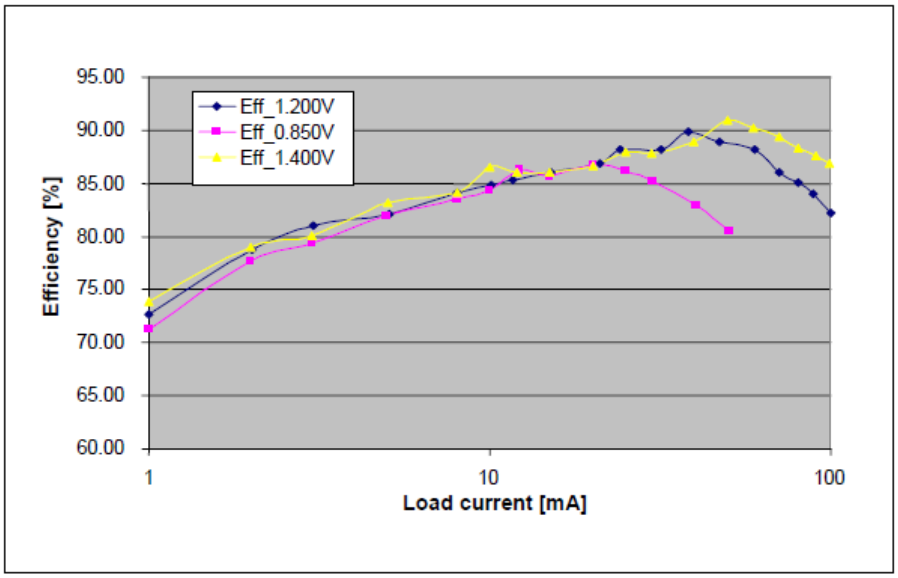


Figure 11: Typical measured DC/DC Efficiency in Standby Mode

In this measurement, an efficiency η >85% is achieved for load currents of 10mA to 30mA and battery supplies (VBAT) greater 0.85V. For battery supplies approximately 1.2V and load currents of 50mA, an efficiency of close to 90% can be obtained.

10.1.2 Xtreme Mode efficiency

Figure 12 shows the efficiency versus load current for Xtreme Mode, when the on-chip VCC2 consumption is approximately 3µA. Measurement traces are plotted for VBAT = {0.85V, 1.20V, and 1.40V}, with loads ranging 0 to 500µA.

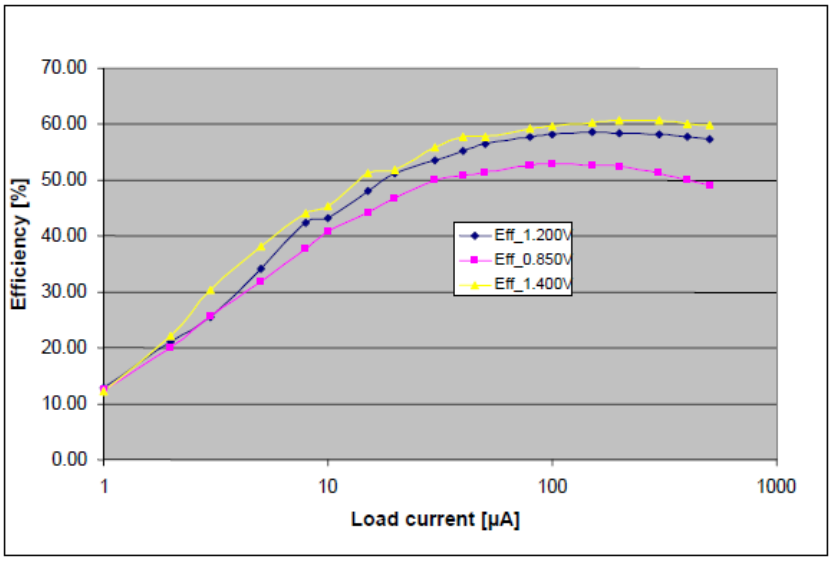


Figure 12: DC/DC converter efficiency in Xtreme Mode

The efficiency in this mode achieves a typical value of η = 55% at a load current of 30µA.

10.2 Xtreme Mode battery current versus load current

Xtreme Mode current is significantly higher than the actual load current and may be useful for battery lifetime calculations. Figure 13 shows the battery current versus the load current for VBAT = {0.85V, 1.20V, and 1.40V}. This is the same data used to derive the efficiency plots shown in Figure 12, but plotted in a different way.

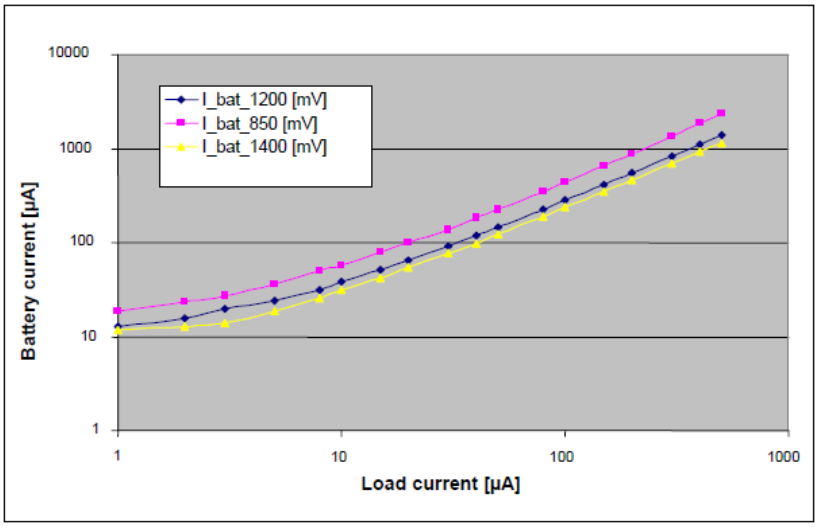


Figure 13: Xtreme Mode - battery current vs. load-current

For a typical supply voltage of 1.2V, the measured battery current is 10µA when there is no external load, and rises to 40µA when an external load of 10µA.

11. Typical Applications

In this chapter, typical application scenarios for the EM9203 are described – both for the DC/DC step-up configuration (Version 11) and for system using a direct battery (or regulator) supply.

11.1 Application schematics

A typical application schematic for Version 11 of the EM9203 is shown in Figure 14. The DC/DC converter requires L1, R1, C1, and C2. Decoupling should be provided for the digital supply (C8), and the PA suppl.y (C7). Additionally a precision (±2%) resistor (R2) is required for the bias circuitry, and a 26MHz crystal (X1) with load capacitors (C5 and C6) are required for the RF and digital clock. A 200-Ohm PCB antenna (A1) can be used for the wireless link, or a 1:4 balun (50Ω : 200Ω) can be used to interface to standard 50-Ohm antennas (e.g., chip antenna) or test equipment. Finally, it is recommended to include an RF shield over the EM9203 package or die for optimum RF performance, eg minimize interference from WiFi, microwave ovens, and other RF interferes in the 2.4 GHz band.

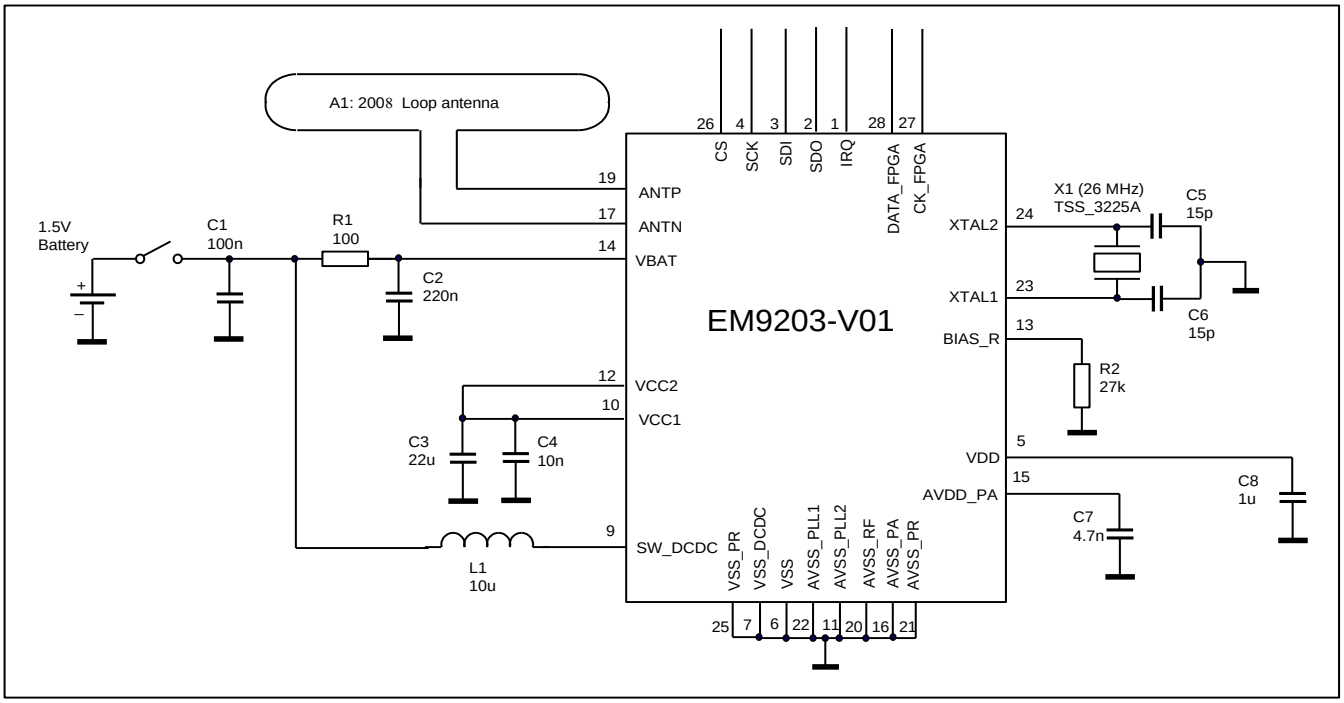


Figure 14: Example application schematic for the EM9203 Version 11 (with DC/DC converter)

A typical application schematic for Version 12 of the EM9203 is shown in Figure 15. The pins VBAT, VCC1 and SW_DCDC are connected to system ground. Decoupling should also be provided for the digital supply (C8), and the PA supply (C7). A precision (±2%) resistor (R2) is required for the bias circuitry, and a 26MHz crystal (X1) with load capacitors (C5 and C6) are required for the RF and digital clock. A 200-Ohm PCB antenna (A1) can be used for the wireless link, or a 1:4 balun (50Ω : 200Ω) can be used to interface to standard 50-Ohm antennas or test equipment. Finally, it is recommended to include an RF shield over the EM9203 package or die for optimum RF performance, eg minimize interference from WiFi, microwave ovens, and other RF interferes in the 2.4 GHz band.

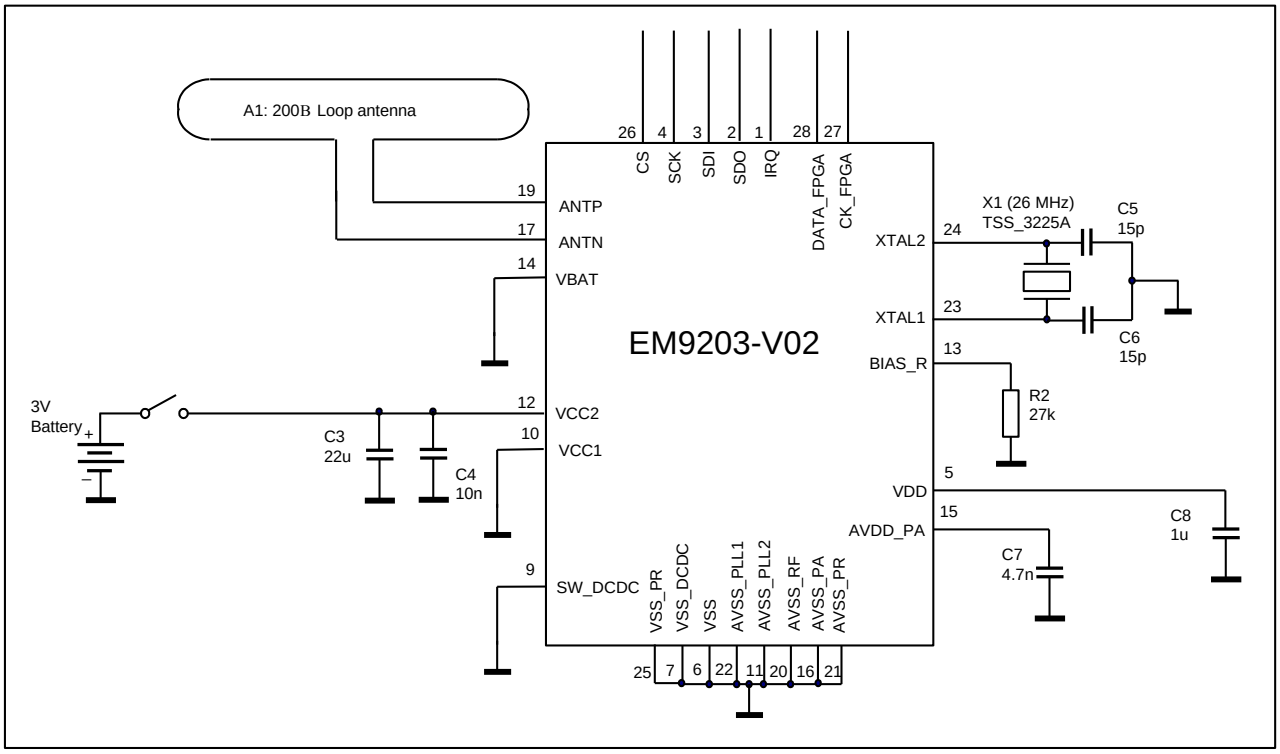


Figure 15: Example application schematic for Version 12 (without DC/DC) of the EM9203

External component values, footprint, tolerance, and other requirements are shown in Table 39 for both of the example applications schematics.

Table 39: EM9203 application schematic external component details

Component	Version	Notes	Value	Footprint	Description
A1	11,12		200Ω	-	Printed loop antenna
C1	11		100nF	0402	VBAT decoupling capacitor, ±10%
C2	11		220nF	0805	VBAT filter capacitor, ±10%
C3	11,12		22µF	0805	DC/DC storage capacitor, X5R ±10%
C4	11,12		10nF	0402	VCC2 decoupling, ±10%
C5	11,12	1	15pF	0402	Crystal load capacitor , ±5%
C6	11,12	1	12pF	0402	Crystal load capacitor, ±5%
C7	11,12		4.7nF	0402	LDO-PA decoupling capacitor, ±10%
C8	11,12		1µF	0805	LDO-Digital decoupling capacitor, ±10%
L1	11		10µH	-	DC/DC coil: recommended ESR < 120 mΩ, ±20%
R1	11		100Ω	0402	VBAT filter resistor, ±10%
R2	11,12		27kΩ	0402	RF-biasing resistor, ±2%
X1	11,12	2	26MHz	-	Crystal, ±50ppm, Example: ABM10-26.000MHZ-D30-T3

Note 1: C5 and C6 must have values that match the crystal load capacitance.

Note 2: Crystal circuit tolerance, temperature, and aging shall not exceed ±50ppm.