Real Time Clock with I2C or SPI, Crystal Temperature Compensation, Battery Switchover and Trickle Charger

Description

The EM3027 is an Ultra Low Power CMOS real-time clock IC with two serial interface modes: I2C or SPI. The interface mode is selected by the chip version (see §12).

The basic clock is obtained from the 32.768 kHz crystal oscillator. A thermal compensation of the frequency is based on the temperature measurement and calculation of the correction value. The temperature can be measured internally or be input by an external application to the register.

The chip provides clock and calendar information in BCD format with alarm possibility. The actual contents are latched at the beginning of a read transmission and afterwards data are read without clock counter data corruption.

An integrated 16-bit timer can run in Zero-Stop or Auto-Reload mode.

An interrupt request signal can be provided through INT/IRQ pin generated from alarm, timer, voltage detector and Self-Recovery system.

An integrated trickle charger allows recharging backup supply V_{Back} from the main supply voltage V_{CC} through internal resistor(s). The internal device supply will switchover to V_{CC} when V_{CC} is higher than V_{Back} and vice versa.

The device operates over a wide 1.4 to 5.5V supply range and requires only 900 nA at 5V. It can detect internally two supply voltage levels.

Applications

- Utility meters
- Battery operated and portable equipment
- Consumer electronics
- White/brown goods
- Pay phones
- Cash registers
- Personal computers
- Programmable controller systems
- Data loggers

Features

- Fully operational from 2.1 to 5.5V
- Supply current typically 600 nA at 1.4V
- Thermal compensated crystal frequency
- Oscillator stability 0.5 ppm / Volt
- Counter for seconds, minutes, hours, day of week, date months, years in BCD format and alarm
- Leap year compensation
- 16-bits timer with 2 working modes
- Two low voltage detection levels V_{Low1}, V_{Low2}
- Automatic supply switchover
- Serial communication via I2C (I^2C-bus specification Rev. 03 compatible – see §10.2) or SPI (3-line SPI-bus with separate combinable data input and output)
- Thermometer readable by the host
- Trickle charger to maintain battery charge
- Integrated oscillator capacitors
- Two EEPROM and 8 RAM data bytes for application
- Digital Self-Recovery system
- No busy states and no risk of corrupted data while accessing
- One hour periodical configuration registers refresh
- Support for standard UL1642 for Lithium batteries
- Standard temperature range: -40°C to +85°C
- Extended temperature range: -40°C to +125°C
- Packages: TSSOP8, TSSOP14, SO8.

Block Diagram

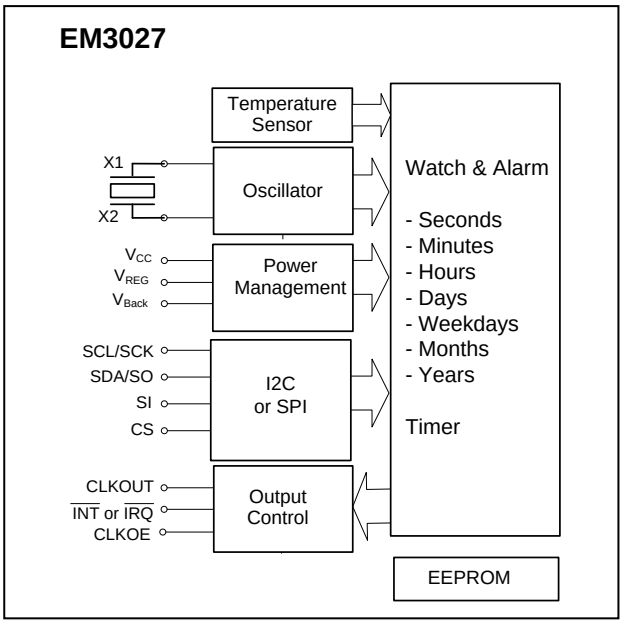
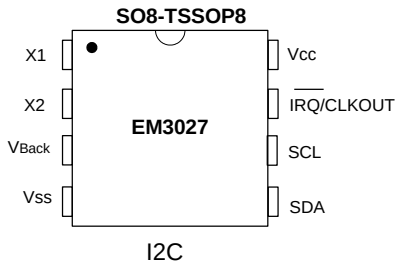


Table of contents

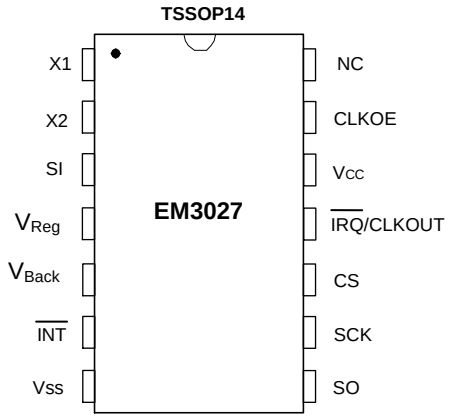
1 Packages / Pin Out Configuration



I2C

Pin	Name	Function
1	X1	32.768 kHz crystal input
2	X2	32.768 kHz crystal output
3	V_{Back}	Backup Supply
4	V_{SS}	Ground Supply
5	SDA	Serial Data
6	SCL	Serial Clock
7	$\overline{IRQ}$/CLKOUT	Interrupt Request/Clock output
8	V_{CC}	Positive Supply

Table 1



SPI

Pin	Name	Function
1	X1	32.768 kHz crystal input
2	X2	32.768 kHz crystal output
3	SI	Serial Data input
4	V_{Reg}	Regulated Voltage – Reserved for test purpose (This output must be left unconnected)
5	V_{Back}	Backup Supply
6	$\overline{INT}$	Interrupt Request output (Open Drain active low)
7	V_{SS}	Ground Supply
8	SO	Serial Data output
9	SCK	Serial Clock input
10	CS	Chip Select input
11	$\overline{IRQ}$/CLKOUT	Interrupt Request/Clock output
12	V_{CC}	Positive Supply
13	CLKOE	Clock Output Enable CLKOE = '0' CLKOUT is low CLKOE = '1' CLKOUT is output
14	NC	Not Connected

Table 2

2 Absolute Maximum Ratings

Parameter	Symbol	Conditions
Maximum voltage at V_{CC}	V_{CCmax}	V_{SS} + 6.0V
Minimum voltage at V_{CC}	V_{CCmin}	V_{SS} – 0.3V
Maximum voltage at any signal pin	V_{max}	V_{CC} + 0.3V
Minimum voltage at any signal pin	V_{min}	V_{SS} – 0.3V
Maximum storage temperature	T_{STOmax}	+150°C
Minimum storage temperature	T_{STOmin}	-65°C
Electrostatic discharge maximum to MIL-STD-883C method 3015.7 with ref. to V_{SS}	V_{Smax}	2000V

Table 3

Stresses above these listed maximum ratings may cause permanent damages to the device.

Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

2.1 Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

2.2 Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temp.	T_A	-40		+125	°C
Supply voltage (Note 1)	V_{CC}, V_{Back}	1.4	5.0	5.5	V
Capacitor at V_{CC}, V_{Back}	C_D		100		nF

Table 4

Note 1: Refer to paragraphs 9.1 and 9.2

2.3 Crystal characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Frequency	f		32.768		kHz
Load capacitance	C_L	7	8.2	12.5	pF
Series resistance	R_S		70	110	kΩ

Table 5

Crystal Reference : Micro Crystal CC5V-T1A
web: www.microcrystal.com

2.4 EEPROM Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Read voltage	V_{Read}	1.4			V
Programming Voltage	V_{Prog}	2.2			V
EEPROM Programming Time	T_{Prog}			30	ms
Write/Erase Cycling		5000			cycles

Table 6

3 Electrical Characteristics

Parameter	Symbol	Test Conditions	V_{CC}	Temp. °C	Min	Typ	Max	Unit
Total supply current with Crystal	I_{CC}	All outputs open, Rs < 70 kΩ, V_{Back} = 0V I2C: SDA, SCL at V_{CC}, Clk/Int='0' SPI: All inputs at V_{SS}	1.4	-40 to 125		0.6	4.6	µA
			3.3	-40 to 125		0.8	5.2	
			5.0	-40 to 125		0.9	5.5	
Total supply current with Crystal	I_{Back}	All outputs open, Rs < 70 kΩ, V_{CC} = 0V, V_{Back} = 3.3V I2C: SDA, SCL at V_{Back}, Clk/Int='0' SPI: All inputs at V_{SS}	0	-40 to 125		0.8	5.2	µA
Dynamic current I2C	I_{DD}	SCL = 100kHz (See Note 1)	1.4	-40 to 125			15	µA
		SCL = 400kHz (See Note 1)	3.3	-40 to 125			40	
		SCL = 400kHz (See note 1)	5.0	-40 to 125			60	

Parameter	Symbol	Test Conditions	V_{CC}	Temp. °C	Min	Typ	Max	Unit
Dynamic current SPI Interface	I_{DD}	SCK = 200 kHz (See Note 2)	1.4	-40 to 125			18	µA
		SCK = 1 MHz (See Note 2)	3.3	-40 to 125			55	
		SCK = 1 MHz (See Note 2)	5.0	-40 to 125			75	
Low supply detection level1	V_{low1}	Relative to V_{CC}		-40 to 125	1.8		2.1	V
Low supply detection level2	V_{low2}	Relative to V_{CC}		-40 to 125	1.0		1.4	V
Switchover hysteresis	V_{hyst}	V_{CC} with respect to V_{Back} = 3.0V		-40 to 125		20		mV
Input Parameters								
Low level input voltage	V_{IL}	CS, CLKOE, SI, SCL/SCK, SDA	1.4 to 5.0	-40 to 125			0.2V_{CC}	V
High level input voltage	V_{IH}			-40 to 125	0.8V_{CC}			
Input Leakage	I_{IN}	0.0 < V_{IN} < V_{CC}	1.4 to 5.0	-40 to 125	-1.5		1.5	µA
Output Parameters								
Low level output voltage	V_{OL}	I_{OL} = 0.4 mA	1.4	-40 to 125			0.2	V
High level output voltage	V_{OH}	I_{OH} = 0.1 mA			1.0			
Low level output voltage	V_{OL}	I_{OL} = 1.5 mA	3.3	-40 to 125			0.25	V
High level output voltage	V_{OH}	I_{OH} = 1.5 mA			2.7			
Low level output voltage	V_{OL}	I_{OL} = 5.0 mA	5.0	-40 to 125			0.8	V
High level output voltage	V_{OH}	I_{OH} = 2.0 mA			4.5			
Output HiZ leakage on $\overline{INT}$	I_{LEAK_OUT}	$\overline{INT}$ not active	1.4 to 5.0	-40 to 125	-1.5		1.5	µA
Oscillator								
Start-up voltage	V_{STA}	T_{STA} < 10s		-40 to 125	1.2			V
Start-up time	T_{STA}		5.0	-40 to 125		1	3	s
Frequency stability over voltage	$\Delta f/(f \Delta V)$	1.8V ≤ V_{CC} ≤ 5.5V, T_A = +25°C		25		0.5	2	ppm/V
Input capacitance on X1	C_{IN}	T_A = +25°C, f = 32.768kHz, V_{meas} = 0.3V (Note 3)		25		16.5		pF
Output capacitance on X2	C_{OUT}	T_A = +25°C, f = 32.768kHz, V_{meas} = 0.3V (Note 3)		25		15.0		
Trickle Charger								
Current limiting Resistors	R80k	V_{CC} =5.0V, V_{Back}=3.0V		25		80		kΩ
	R20k	V_{CC} =5.0V, V_{Back}=3.0V		25		20		
	R5k	V_{CC} =5.0V, V_{Back}=3.0V		25		5.0		
	R1.5k	V_{CC} =5.0V, V_{Back}=3.0V		25		1.5		
Thermometer								
Precision	T_E	V_{low1} < V_{CC} ≤ 5.5V		40		+/- 1	+/- 2	°C
				-40 to 125		+/- 4	+/- 10	

Table 7

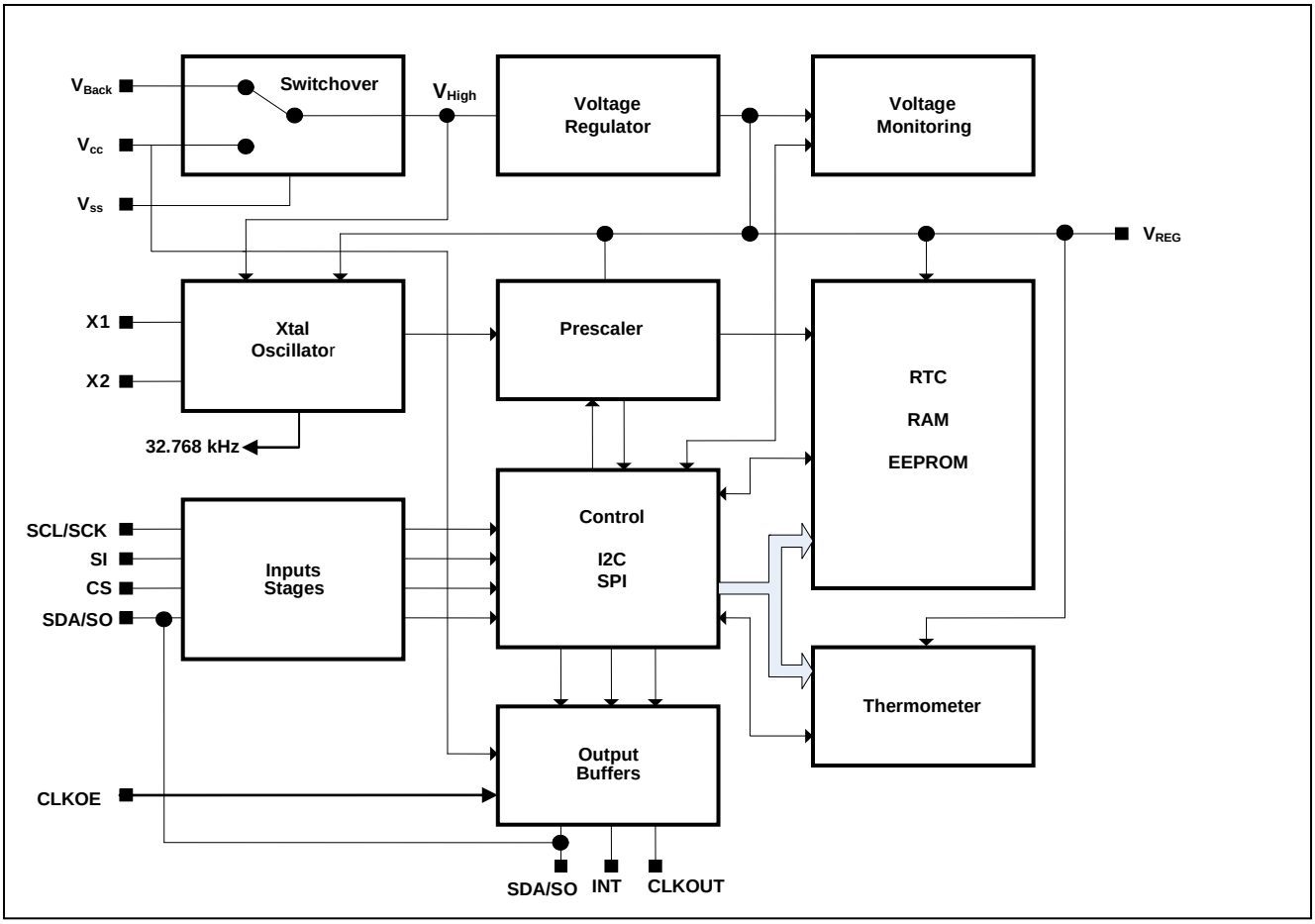
The following parameters are tested during production test: I_{DD}, V_{low1}, V_{low2}, V_{IL}, V_{IH}, V_{OL}, V_{OH}, I_{IN}, I_{LEAK_OUT}
The parameters I_{CC}, V_{hyst}, V_{STA}, T_{STA}, C_{IN}, C_{OUT}, $\Delta f/(f*\Delta V)$, T_E are characterised during the qualification of the IC.

Notes:

1. SDA = V_{SS}, continuous clock applied at SCL (V_{IL_SCL} < 0.05V, V_{IH_SCL} > 0.95V_{CC})
2. CS, SI = V_{CC}, continuous clock applied at SCK, SO not connected. (V_{IL_SCK} < 0.05V_{CC}, V_{IH_SCK} > 0.95V_{CC})
   Note that there is a 100kΩ pull-down resistor on CS.
3. V_{meas} : Peak to peak amplitude during capacitance measurement
4. Below 0°C, a negative slope on Vcc will stop the oscillator during a time which may be as long as 1 second. This is not dependent on slope and occurs with a slew rate as low as 2V/sec.
5. Some chip versions do not support “Trickle Charger” and “Switchover” features.

4 EM3027 Block Diagram and Application Schematic

4.1 Block Diagram



4.2 Application Schematic

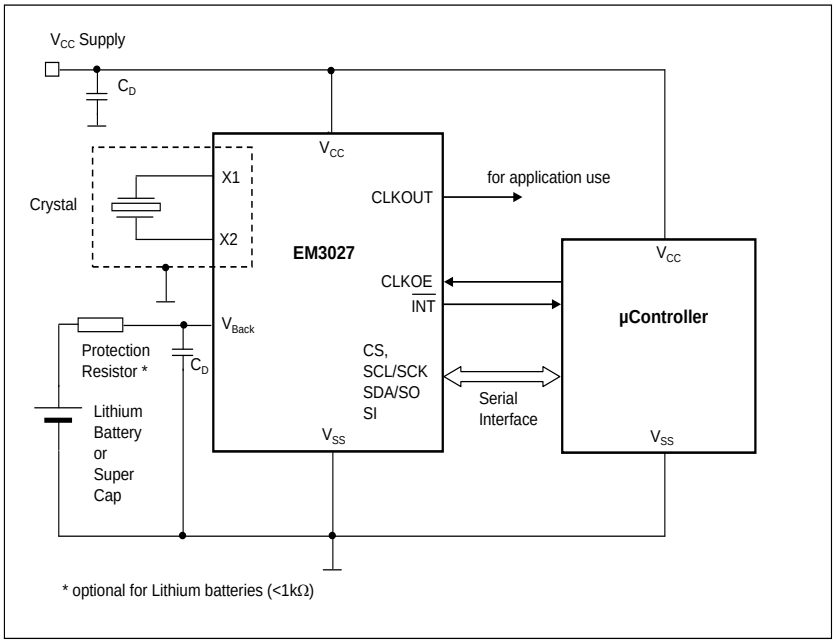
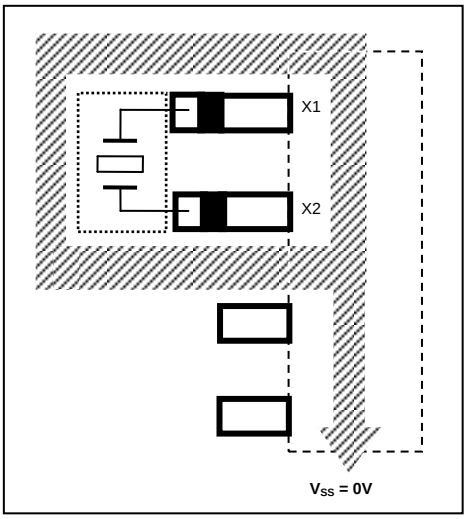


Figure1: Application Schematic

Crystal Layout Example



4.3 Crystal Thermal Behaviour

The frequency of the crystal is dependent on the temperature concurring with the following diagram:

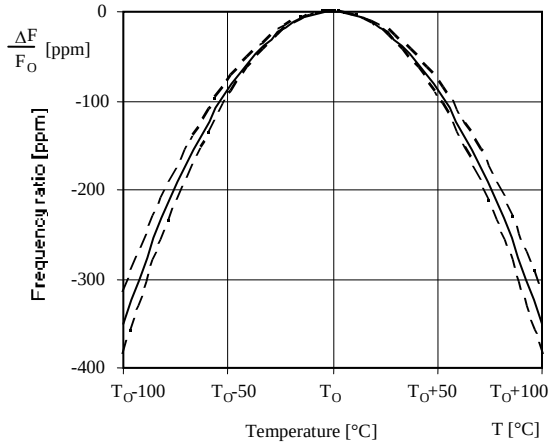


Figure 1: Crystal thermal behaviour

T_O – Turnover temperature [°C]
F_O – Crystal frequency when T_O [Hz]

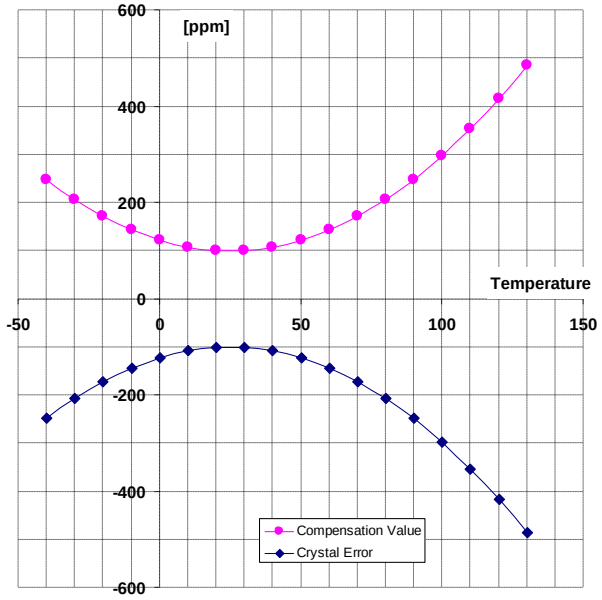
The following formula expresses a compensation value to be used during frequency correction.

$$COMP\_val = Qcoef \times (T - To)^2 - XtalOffset$$

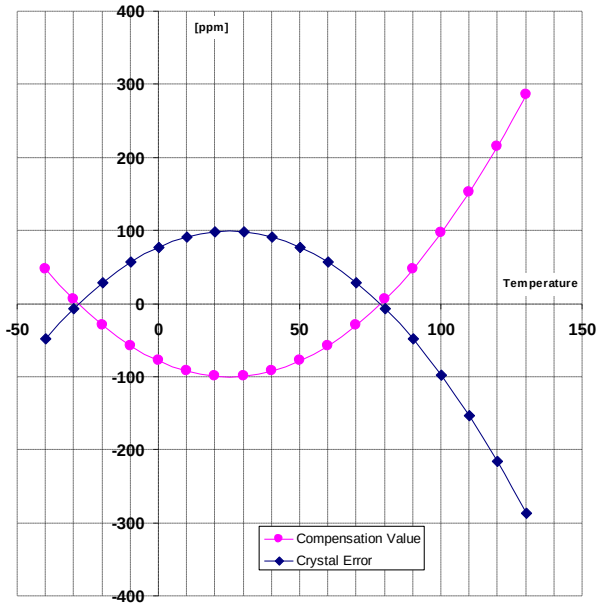
Qcoef	– Thermal quadratic coefficient [ppm/°C^2]
T	– Actual temperature [°C]
T_O	– Turnover temperature [°C]
XtalOffset	– Crystal offset at T_O [ppm]
COMP_val	– Compensation value result [ppm]

The oscillator frequency is adjusted according to the equation above by using coefficients located in the EEPROM control page and the temperature.
The actual temperature can be obtained from the internal thermometer or from Temp register updated externally by an application.
The principle of the frequency compensation is based on adding/removing of pulses.

Example 1: Qcoef=0.035; T_O=25; XtalOffset=–100



Example 2: Qcoef=0.035; T_O=25; XtalOffset=+100



4.4 Crystal Calibration

In order to compensate temperature dependency of the used crystal, correct values of XtalOffset, Qcoef and T_O parameters shall be stored in EEPROM Control Page. User is advised to follow these steps in order to compute the parameters in a correct way:

1) Supply the chip from V_{CC} pin.

2) Set FD0 = FD1 = '0'. Set CLKOE pin to '1'. This provides the uncompensated frequency signal from the crystal oscillator directly on pin CLKOUT.

3) Measure output frequency f_O at different temperatures (at least five measurements in equidistant points in the whole desired temperature range are recommended). Please note that quartz crystal needs few minutes to stabilise its frequency at a given temperature.

4) Compute frequency deviation f_{err} in ppm of output frequency f_o from the ideal (target) frequency f_L = 32.768Hz in all measured points as follows:
$$f_{err} = 10^6(f_o-f_L)/f_L .$$

5) Find a quadratic regression of the measured dependency in form:
$$f_{err} = -c_1(T - c_2)^2 + c_3 \text{ or } f_O = aT^2 + bT + c.$$

6) Then real values of the searched parameters can be obtained from the following relations:
$$Qcoef_{real} = c_1 = -a,$$
$$T_{0\_real} = c_2 = -b/(2a),$$
$$XtalOffset_{real} = c_3 = c - b^2/(4a).$$

7) The values to be stored in EEPROM Control Page have to be corrected in the following way:
$$Qcoef = 4096*(1.05*Qcoef_{real}),$$
$$T_0 = T_{0\_real} - 4,$$
$$XtalOffset = 1.05*XtalOffset_{real}.$$

5 Memory Mapping

Address			Description	Range	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Page	Addr	Hex										
[6..3]	[2..0]											
Control Page												
00000	**000**	**0x00**	OnOffCtrl		Clk/Int	TD1	TD0	SROn	EERefOn	TROn	TiOn	WaOn
				Default	1	0	0	1	1	0	0	1
	001	**0x01**	IRQctrl					SRIntE	V2IntE	V1IntE	TIntE	AIntE
				Default				0	0	0	0	0
	010	**0x02**	IRQflags	----				SRF	V2F	V1F	TF	AF
	011	**0x03**	Status	----	EEBusy		PON	SR	VLOW2	VLOW1		
	100	**0x04**	RstCtrl	----				SYSRes				
Watch Page												
00001	**000**	**0x08**	Watch Seconds	0 – 59 BCD		Seconds Tens			Seconds Units			
	001	**0x09**	Watch Minutes	0 – 59 BCD		Minutes Tens			Minutes Units			
	010	**0x0A**	Watch Hours	0 - 23 BCD 1 - 12 BCD		S12/24	pm/2	Hours Tens	Hours Units			
	011	**0x0B**	Watch Date	1 – 31 BCD			Date Tens		Date Units			
	100	**0x0C**	Watch Days	1 – 7 BCD						Days Units		
	101	**0x0D**	Watch Months	1 – 12 BCD				Months Tens	Months Units			
	110	**0x0E**	Watch Years	0 – 79 BCD		Years Tens			Years Units			
Alarm Page												
00010	**000**	**0x10**	Alarm Seconds	0 – 59 BCD	SecEq	Seconds Tens			Seconds Units			
	01	**0x11**	Alarm Minutes	0 – 59 BCD	MinEq	Minutes Tens			Minutes Units			
	010	**0x12**	Alarm Hours	0 - 23 BCD 1 - 12 BCD	HourEq		pm/2	Hours Tens	Hours Units			
	011	**0x13**	Alarm Date	1 – 31 BCD	DateEq		Date Tens		Date Units			
	100	**0x14**	Alarm Days	1 – 7 BCD	DayEq					Days Units		
	101	**0x15**	Alarm Months	1 – 12 BCD	MonthEq			Months Tens	Months Units			
	110	**0x16**	Alarm Years	0 – 79 BCD	YearEq	Years Tens			Years Units			
Timer Page												
00011	**000**	**0x18**	Timer low byte	0-255	-	-	-	-	-	-	-	-
	001	**0x19**	Timer high byte	0-255	-	-	-	-	-	-	-	-
Temperature Page												
00100	**000**	**0x20**	Temp	-60-195 °C	-	-	-	-	-	-	-	-
EEPROM Data Page - Configuration Registers												
00101	**000**	**0x28**	EEData	----	EEPROM user data (2 bytes)							
	001	**0x29**										
EEPROM Control Page - Configuration Registers												
00110	**000**	**0x30**	EEctrl	----	R80k	R20k	R5k	R1.5k	FD1	FD0	ThEn	ThPer
				Default	0	0	0	0	0	0	1	0
	001	**0x31**	XtalOffset	±121	sign	-	-	-	-	-	-	-
				Default	-	-	-	-	-	-	-	-
	010	**0x32**	Qcoef	----	-	-	-	-	-	-	-	-
				Default	-	-	-	-	-	-	-	-
	011	**0x33**	TurnOver	4-67 °C			-	-	-	-	-	-
				Default			-	-	-	-	-	-
RAM Page (User data RAM)												
00111	**000-111**	**0x38-0x3F**	RAMdata	----	8 bytes of data							

Table 8

Unused bit (Read as zero; write has no influence)

Notes and Settings:

- Only pages 0 to 7 are used. Unused pages are for test purposes. The application should not write into unused pages and addresses.
- The crystal offset must be set to within ± 121 ppm.
- Zero values are read from unused addresses.
- Watch, Alarm, Timer pages have to be set by an application before use.
- The bit 7 (MSB) of the Alarm registers (SecEq, MinEq.) have to be set to '1' to perform the comparison. (See paragraph 8.3)

6 Definitions of terms in the memory mapping

Control Page - Register *OnOffCtrl*

Clk/Int	Selects if clock or interrupt is applied onto the $\overline{IRQ}$/CLKOUT pin ('0' = $\overline{IRQ}$ output; '1' = CLKOUT output) – CLKOUT output is the default state after reset
TD0, TD1	Selects decrement rates for Timer (32 Hz after reset)
SROn	Enables Self-Recovery function (ON after reset)
EERefOn	Enables Configuration registers refresh each 1 hour (ON after reset)
TROn	Enables Timer Auto-reload mode ('0' – reload disabled; '1' – reload enabled)
TiOn	Enables Timer (OFF after reset)
WaOn	Enables 1 Hz clock for Watch (ON after initialisation)

Control Page - Register *IRQctrl*

SRIntE	Self-Recovery interrupt enable
V2IntE	VLOW2 interrupt enable
V1IntE	VLOW1 interrupt enable
TIntE	Timer interrupt enable
AIntE	Alarm interrupt enable

Control Page - Register *IRQflags*

SRF	Self-Recovery interrupt flag (bit is set to '1' when Self-Recovery reset is generated)
V2F	VLOW2 interrupt flag (bit is set to '1' when power drops below Vlow2)
V1F	VLOW1 interrupt flag (bit is set to '1' when power drops below Vlow1)
TF	Timer interrupt flag (bit is set to '1' when Timer reaches ZERO)
AF	Alarm interrupt flag (bit is set to '1' when Watch matches Alarm)

NOTE: *Flags can be cleared by '0' writing.*

Control Page - Register *Status*

EEBusy	EEPROM is busy (bit is set to '1' when EEPROM write or Configuration Registers refresh is in progress) (Read Only)
PON	Power ON (bit is set to '1' at Power On; clear by '0' writing)
SR	Self-Recovery reset or System reset detected (clear by '0' writing)
VLOW2	Voltage level V_{CC} or V_{Back} below Vlow2 level (clear by '0' writing)
VLOW1	Voltage level V_{CC} or V_{Back} below Vlow1 level (clear by '0' writing)

Control Page - Register *RstCtrl*

SYSRes	System reset register; writing '1' will initiate restart of the logic (Watch, Alarm and Timer parts excluded). After the restart, status bit SR is set. The register is cleared after restart of the logic.

Watch Page - Registers *Watch Seconds, Watch Minutes, Watch Hours, Watch Date, Watch Days, Watch Months, Watch Years*

Watch information (BCD format)

S12/24	12-hours or 24-hours format selection; 12-hours: S12/24 = '1', 24-hours: S12/24 = '0'
PM/2	S12/24 = '0' PM/2 represents value '2' of tens, S12/24 = '1' PM/2 = '1' represents PM (afternoon), PM/2 ='0' represents AM (morning)

Alarm Page - Registers *Alarm Seconds, Alarm Minutes, Alarm Hours, Alarm Date, Alarm Days, Alarm Months, Alarm Years*

Alarm information (BCD format)

PM/2	S12/24 = '0' PM/2 represents value '2' of tens, S12/24 = '1' PM/2 = '1' represents PM (afternoon), PM/2 ='0' represents AM (morning)

Timer Page - Registers *TimLow, TimHigh*

TimLow	Timer value (Low byte)
TimHigh	Timer value (High byte)

Temperature Page - Register *Temp*

Temp	Temperature (range from -60° C to 190°C with 0°C corresponding to a content of 60d)

EEPROM Data Page - Register *EEData*

EEData	General purpose EEPROM data bytes

EEPROM Control Page - Register *EEctrl*

R80k, R20k, R5k, R1.5k	Selects trickle charger resistors between V_{High} and V_{Back}
FD0, FD1	Selects clock frequency at $\overline{IRQ}$/CLKOUT pin.
ThEn	Enables thermometer ('0' = disabled; '1' = enabled)
ThPer	Selects thermometer activation period ('0' = 1 second; '1' = 16 seconds)

EEPROM Control Page - Register *XtalOffset*

XtalOffset — Crystal frequency deviation at Turnover temperature T_O in ppm. Example: value 63d is related to 60 ppm.

$$XtalOffset = 1.05 * XtalOffset_{real}$$

where $XtalOffset_{real}$ is real value of crystal frequency deviation at Turnover temperature of the used crystal in ppm.

Note: *Coefficient 1.05 (exactly 1.048576) is the result of the internally used frequency compensating method.*

EEPROM Control Page - Register Qc*oef*

Qcoef — Thermal quadratic coefficient of the crystal. Example: value 151d is related to 0.035 ppm/°C²,

$$Qcoef = 4096 \times 1.05 \times QCoef_{real},$$

where $Qcoef_{real}$ is real value of thermal quadratic coefficient of the crystal in ppm/°C².

EEPROM Control Page - Register *TurnOver*

TurnOver — Turnover temperature of the crystal (values 0 to 63d are related to temperature 4 to 67 °C). Example: value 21d is related to 25°C.

$$T_0 = T_{0\_real} - 4,$$

where T_{0_real} is real value of Turnover temperature of the crystal in °C.

RAM Page - Register *RAMdata*

RAMdata	General purpose RAM data bytes

7 Serial communication

Depending on the EM3027 version, the serial communication is performed in I2C or SPI mode.

A serial communication with the EM3027 starts with a "Transmission START" and terminates with the "Transmission STOP".

"Transmission START"
I2C – START condition
SPI – CS goes to '1'

"Transmission STOP"
I2C – STOP condition
SPI – CS goes to '0'

When the "Transmission START" is detected, a copy of the content of the addressed Watch-, Alarm-, Timer- and Temperature-register is stored into a cache memory. Data for a following read access are provided from this cache memory.
Data in the cache memory are stable until the "Transmission STOP".

During a write access, data are written into the cache memory.
When the "Transmission STOP" of a WRITE transmission is detected, the content of modified registers in the cache memory is copied back into the Watch-, Alarm, Timer- and/or Temperature-register.

7.1 How to perform data transmission through I2C

The I2C protocol is a bidirectional protocol using 2 wires for master-slave communication: SCL (clock) and SDA (data). The two bus lines are driven by open drain outputs and pulled up externally. MSB is sent first.

The communication is controlled by the master. To start a transmission, the master applies the START condition and generates the SCL clocks during the whole transmission. The master terminates the transmission by sending the STOP condition.

The first byte contains the 7 bit slave address and the R/W bit. The slave address must correspond to the fixed slave address of the EM3027. After each byte, the receiver outputs an acknowledge bit ACK to confirm correct recept of the byte by a '0' level.

At a WRITE transmission (R/W = 0), the master sends slave address, register address and data bytes.

In the EM3027, the upper 5 bits of a register address form a "page address", the 3 lower bits are an auto-incrementing sub-address. The "page-address" is defined by a WRITE transmission. During a transmission, the 3 lower address bits are internally incremented after each data byte.

At a READ transmission (R/W = 1), the slave sends data and the master gives the ACK bit(s). The "page-address" shall be defined by a WRITE transmission, completed with the STOP condition.

The 3 lower address bits are incremented when an ACK is received.

If ACK is not received, no auto-increment of the address is executed and a following read outputs data of the same address.

The EM3027 works as slave. Its slave address is fixed to '1010110'.

I2C: Write transmission

	Slave Address	R/W										
S	**1010110**	**0**	**ACK_s**	**Address**	**ACK_s**	**Data Byte (1)**	**ACK_s**	**Data Byte (n-1)**	**ACK_s**	**Data Byte (n)**	**ACK_s**	**P**

I2C: Read transmission

	Slave Address	R/W						Slave Address	R/W					
S	**1010110**	**0**	**ACK_s**	**Address**	**ACK_s**	**P**	**S**	**1010110**	**1**	**ACK_s**	**Data byte (1)**	**ACK_m**	**Data byte (n)**	**ACK_m**	**P**

S ... start condition sent by the master
R/W ... read/write select ('0': master writes data)
ACK_s ... acknowledge from the receiver (slave)
P ... stop condition
ACK_m ... acknowledge from the receiver (master)

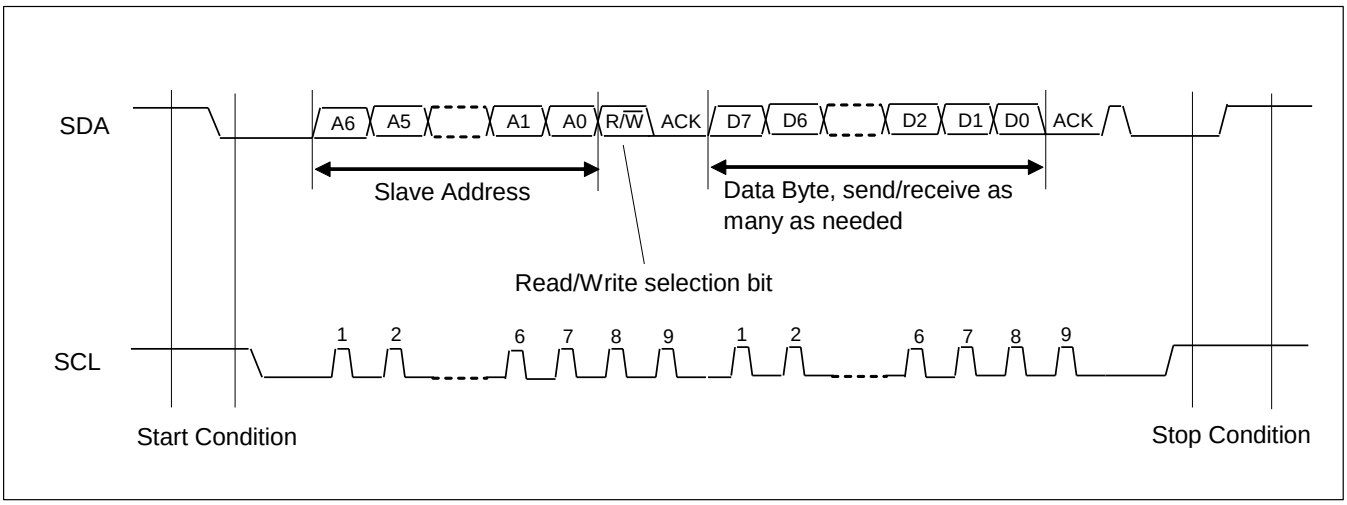


Figure 2: I2C Communication

Noise suppression circuitry is implemented rejecting spikes shorter than 50ns on SCL and SDA bus lines.

7.2 How to perform data transmission through SPI

The SPI interface connects master and slave circuits.

4 connections are used: CS = Chip Select, SCK = Serial Clock, SI = Serial Data Input and SO = Serial Data Output.

SPI is a byte oriented protocol with MSB first mode. Data are changing on SCK falling edge and sampled on rising edge.

A transmission is started by the master by rising the CS input of the selected slave to '1'. The transmission is terminated by the master by putting '0' level the CS input.

The first bit is the R/W bit, R/W = '0' means a WRITE transmission, where the master sends the data via the SI line. R/W = '1' defines a READ transmission, where the slave outputs the data on the SO line.

The following 7 bits of the first byte form the address of the register in the EM3027, where the data are written or read. (MSB is first bit at position 2 in this address byte.) The not transmitted 8th bit of the register address is set internally to '0'.

In the EM3027, the upper 5 bits of an address form a "page address", the 3 lower bits are an auto-incrementing sub-address. The "page-addres'' is defined by a WRITE transmission. During a transmission, the 3 lower address bits are incremented internally after each byte.

During a WRITE transmission, the master defines the register address and sends then data bytes, using the auto-increment of the lower address part (bit 2 to 0) within the EM3027.

The page address is fixed until a new transmission is started.

SO data output of EM3027 is in Hi-Z state during the WRITE transmission.

If READ transmission is initiated, data are output after the address byte by the EM3027.

The lower part of the address (bit 2 to 0) is automatically incremented after each data byte. The page address is not changed until a new transmission is started.

SO is in Hi-Z while the address byte is sent. During data output by SO, the SI input has no influence.

When CS is at '0' level, SO is Hi-Z and SCK, SI can be left floating.

SO and SI can be connected together to form a 3-wire interface with CS, SCK and Serial Data Input/Output.

The EM3027 works as slave. The CS input has a pull-down resistor of 100 kΩ.

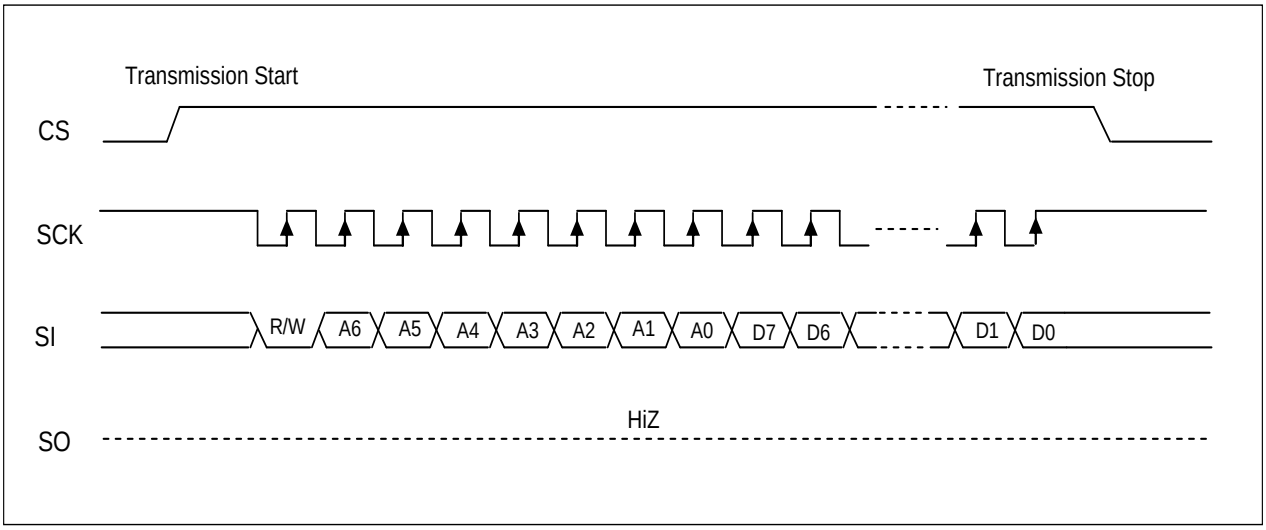


Figure 3: SPI Write Transmission

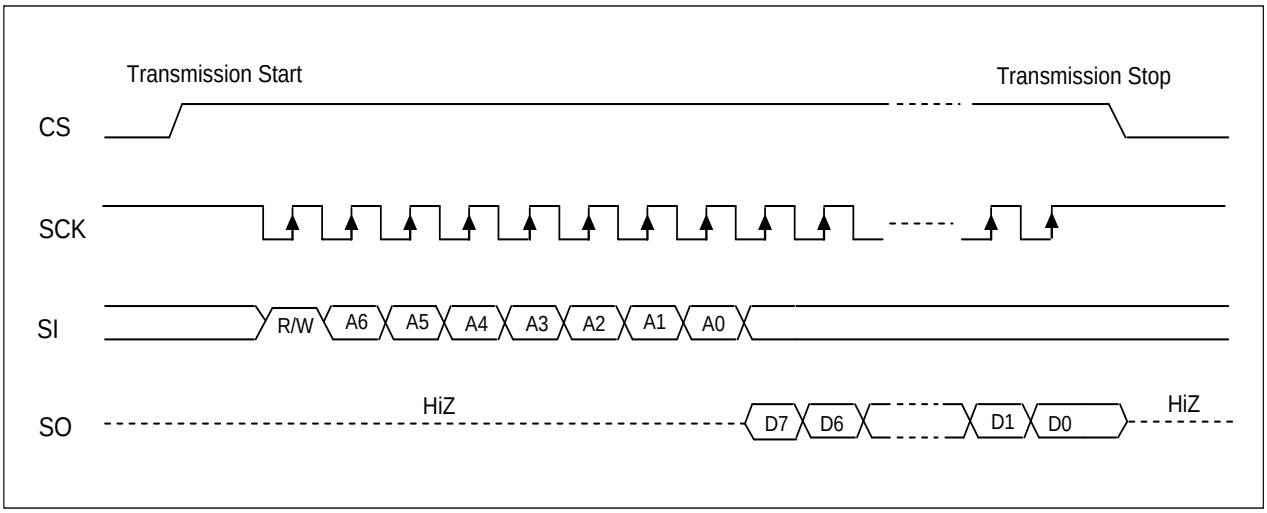


Figure 4: SPI Read Transmission

8 Functional Description

8.1 Start after power-up

A The chip is in reset state when the supply voltage is below an internal threshold level (PON in Status register 0x03 goes to '1'). When the supply level is higher than this threshold voltage, the reset is released.

B When the supply voltage is higher than the oscillator start-up voltage, the basic clocks for Watch and control logic become active after the oscillator start time.

C With clocks present, the voltage detector starts in fast mode to measure the supply voltage. When a voltage higher than Vlow2 is detected, the fast detection mode is stopped and the EEPROM read is enabled.

D Configuration registers are loaded with the configuration data read from the EEPROM (Addresses from 0x28 to 0x33).

E If thermometer is enabled (ThEn='1' and VLOW1='0'), temperature is measured and compensation value for frequency correction evaluated.

F The EM3027 starts its normal function, depending on the supply voltage level applied.

8.2 Normal Mode function

The chip has following functions in Normal Mode:

1. **Voltage detection** – The voltage detection is executed each second.
2. **Temperature measurement** – It is executed, if thermometer is enabled (ThEn='1') and VLOW1='0'.
3. **Frequency compensation** – The compensation of the oscillator frequency works continuously.
4. **Configuration Registers refresh** – The EEPROM is read each hour to refresh the content of the configuration registers (supply voltage must be above Vlow2 for EEPROM read).
5. **Watch/Alarm** – The Watch function is continuously active, whereas the Alarm function depends on its activation.
6. **Timer** – Is active when enabled.
7. **Self-Recovery system** – Is enabled by default (can be disabled by the application).
8. **Serial interface** – The communication works if $V_{CC} > V_{CC\_min}$ and $V_{CC} > V_{Back}$.

8.3 Watch and Alarm function

The Watch part provides timing information in BCD format. The timing data is composed of seconds, minutes, hours, date, weekdays, months and years. The corresponding values are updated every second.

The Watch part setup is provided by Write transmission into the Watch Page (Address 0x08h to 0x0Eh). After the transmission, the Watch is restarted from the setup values after one second.

The Alarm function is activated by setting and enabling the alarm registers (Address 0x10h to 0x16h). Each Alarm byte has its own enable bit. It is the bit 7. Recommended combinations of enabled bits are described in the table below.

SecEq	MinEq	HrsEq	DateEq	DaysEq	MonthEq	YearEq	Al_period
1	0	0	0	0	0	0	min
1	1	0	0	0	0	0	hrs
1	1	1	0	0	0	0	day
1	1	1	1	0	0	0	month
1	1	1	1	0	1	0	year
1	1	1	0	1	0	0	week

Table 9: Alarm Period Selection

- Both Watch and Alarm parts must be set by an application before use
- The bits SecEq to YearEq enable the comparison of the corresponding registers

8.4 Timer function

The 16-bit count down timer can be enabled/disabled by TiOn bit.

The timer input frequency is selected by TD1, TD0 bits according to the following table:

TD1	TD0	Timer frequency
0	0	32 Hz
0	1	8 Hz
1	0	1 Hz
1	1	0.5 Hz

Table 10: Timer Frequency Selection

The timer can run in Zero-Stop or Auto-Reload mode (TROn bit: '0' = Zero-Stop mode, '1' = Auto-Reload mode).

When TROn = '0', then it is possible to read current value of the timer. If TROn = '1', then last written value is read from cache memory. The value in the cache memory is used as the new value for reloading (Auto-Reload mode).

Frequency selection (TD1, TD0) and mode selection (TROn) can be written only when the timer is stopped (TiOn = '0'). Timer values (TimLow, TimHigh) can be written only when the timer is stopped (TiOn = '0' and TROn = '0').

NOTE: *The "Timer Page" can also be used as a general purpose register when the timer function is not used.*

8.5 Temperature measurement

The integrated thermometer has a resolution of 1°C.

The thermometer is disabled when ThEn = '0' and enabled when ThEn = '1'. By default, the thermometer is enabled. Thermometer period is selectable by ThPer bit according to the table below:

ThPer	Period in Seconds
0	1 s
1	16 s

Table 11: Thermometer Period

The thermometer is automatically disabled when VLOW1 status bit is at '1'.

When the thermometer is disabled (ThEn = '0'), the Temp register can be written. Temp register uses a cache memory to keep stable value during a whole transaction (read/write).

8.6 Frequency compensation

There is a frequency compensation unit (FCU) inside EM3027. FCU compensates quartz crystal native frequency in dependency on actual compensation value (COMP_val).

FCU is always running.

During chip power-up, if ThEn = '1' and VLOW1 = '0' temperature measurement is enabled and COMP_val is computed. Otherwise, COMP_val is set to 0 ppm.

In Normal mode, new compensation value is computed each 32 seconds. The only exception is when ThEn = '1' and VLOW1 = '1'. In this case, temperature measurement and COMP_val computation are blocked and FCU uses the last computed compensation value.

For the evaluation of COMP_val, actual content of Temp register (0x20) is used. The compensation value is computed according to the equation described in **paragraph 4.3**.

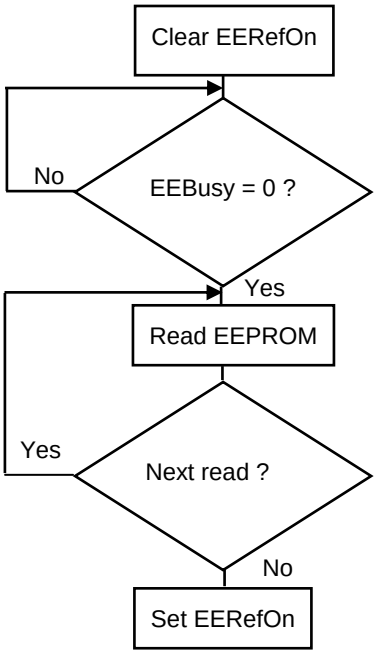
Content of Temp register is updated either after a temperature measurement (when ThEn = '1' and VLOW1 = '0') or after Temp register write transaction (when ThEn = '0'). After power-up content of Temp register is undefined.

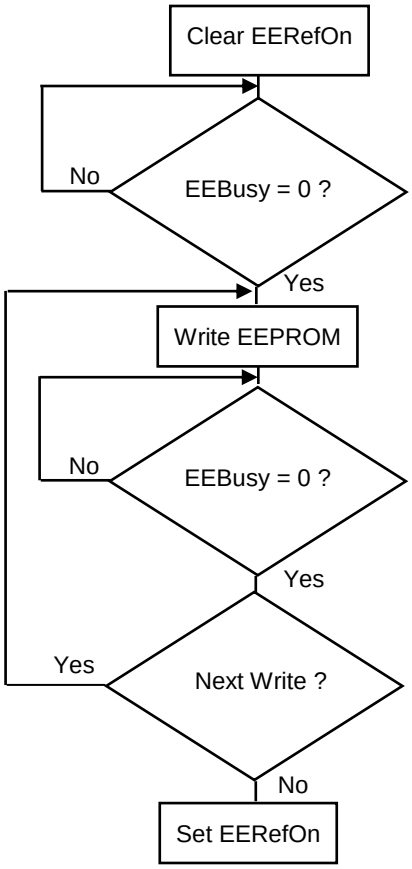
If thermometer is disabled (ThEn = '0') user is advised to periodically update Temp register with actual ambient temperature in order to have correct input data for COMP_val computation.

8.7 EEPROM memory

Before any EEPROM access (read/write), the bit EERefOn has to be cleared by the application to prevent from access collision with the Configuration Registers.
Then the application has to read EEBusy bit and if EEBusy = '0', then EEPROM access can be started.
After the write command (at "Transmission STOP") the current state of EEPROM writing is monitored by EEBusy register bit at '1'. EEBusy goes to '0' when EEPROM writing is finished.

NOTE: V_{CC} *must be applied during the whole EEPROM write (i.e. until EEBusy = '0') and must be higher than* V_{prog}.





After EEPROM write command, EEBusy bit is set to '1' for a time period depending on that how many bytes of EEPROM Data or Control page were written:

EEPROM Write Operation	EEBusy bit set to '1' for [ms]
Any write operation into EEPROM Data page (one or two bytes within one transaction)	35
Single byte write operation into EEPROM Control page	97
Multiple byte write operation into EEPROM Control page (two, three or four bytes within one transaction)	<135

8.7.1 EEPROM Control Page

This part is composed of 4 bytes purposed for miscellaneous function control and for crystal compensation constants.

EEctrl byte contains: trickle charger selectors (R80k, R20k, R5k, R1.5k); output clock frequency selector (FD1, FD0); thermometer enable and thermometer period selector.

8.7.2 Clock Output

Output clock frequency is selected by FD1, FD0 bits in EEctrl register.

FD1	FD0	Select Clock Output	Description
0	0	32.768 kHz	From crystal oscillator, without frequency compensation
0	1	1024 Hz	With frequency compensation
1	0	32 Hz	
1	1	1 Hz	

Table 12: Output Clock frequency selection

8.7.3 Configuration Registers

All the configuration data from EEPROM (i.e. EEctrl, XTalOffset, Qcoef, TurnOver, EEData) is hold in configuration registers.

Data from EEPROM is loaded to these registers during power-up sequence and is refreshed each hour, if 'Configuration Registers refresh' feature is enabled (EERefOn = '1').

Regular refresh of Configuration Registers prevents their content to be corrupted by strongly polluted electrical environment (EMC problems, disturbed power supply, etc.).

It is recommended to enable 'Configuration Registers refresh' feature.

8.7.4 EEPROM User Memory

Two bytes of the memory are dedicated for the application (addresses 0x28 and 0x29).

8.8 RAM User Memory

RAM user memory size is 8 bytes (addresses 0x38 to 0x3F). The state of the RAM data after power-up is undefined.

8.9 Status Register

The purpose of EEBusy bit is to inform the user about current status of the EEPROM operations.

EEBusy – status of EEPROM controller (if EEBusy = '1', then Configuration Registers refresh or EEPROM write is in progress)

The purpose of the following status bits is to record status of power supply voltage and Self-Recovery system/System reset behaviour.

PON – status of Power-ON
VLOW1 – status of Vlow1 voltage detection
VLOW2 – status of Vlow2 voltage detection
SR – status of the Self-Recovery system/System reset

If one of these status bits is set, it can be cleared only by writing '0', there is no automatic reset if the set condition disappears.

8.10 Interrupts

There are five interrupt sources which can output an interrupt on ($\overline{\text{INT}}$ and/or $\overline{\text{IRQ}}$/CLKOUT) pins. The request is generated when at least one of IRQflags goes to '1' (OR function).

AF – interrupt is provided when Watch time reaches Alarm time settings and comparison is enabled
TF – interrupt is provided when Timer reaches ZERO
V1F – interrupt is provided when supply voltage is below Vlow1 (when VLOW1 status bit is set)
V2F – interrupt is provided when supply voltage is below Vlow2 (when VLOW2 status bit is set)
SRF – interrupt is provided when Self-Recovery system invoked internal reset (when SR status bit is set)

Each interrupt source has its own interrupt enable (AIntE, TIntE, V1IntE, V2IntE, SRIntE). When the interrupt enable is '1' then the appropriate interrupt source is enabled.

Interrupt flags (IRQflags) are cleared by ‘0’ writing into the appropriate bit. In case of V1F, V2F and SRF bits, it is necessary to clear also the corresponding status bits (Status) after interrupt bit.

8.11 Self-Recovery System (SRS)

The purpose of the Self-Recovery System (SRS) is to generate an internal reset in case the on-chip state machine goes into a deadlock. The function is based on an internal counter that is periodically reset by the control logic. If the counter is not reset on time, this reset will take place. It is executed after two voltage monitoring periods at the latest, i.e. 2s or 32s (ThPer bit).

A possible source of a deadlock could be disturbed electrical environment (EMC problem, disturbed power supply, etc.).

SRS sets status bit SR and resets the internal logic, except Watch, Alarm and Timer parts (i.e. time informations are not affected). Furthermore, if the SRS interrupt is enabled (SRIntE='1'), the SRF flag is set after the internal chip reset. Note, that SROn = '1' and SRIntE = '0' after the reset.

After the internal reset, the device starts with the power-up sequence (see paragraph 8.1).

SRS is automatically enabled after power-up (SROn bit). It can be disabled by writing '0' into the SROn bit in the Control Page.

8.12 Register Map

The address range of the EM3027 is divided into pages. The page is addressed by the five most significant bits of the address (bits 6 … 3). The three low significant bits of the address provide selection of registers inside the page. During address incrementing the three low significant bits (2 … 0) are changed. The page address part is fixed during the whole data transmission.

8.13 Crystal Oscillator and Prescaler

The 32.768 kHz crystal oscillator and the clock divider provide the timing signals for the functional blocks. The prescaler block is responsible for frequency division of the 32.768 kHz clock signal from the crystal oscillator. Divided frequency is then distributed between other blocks inside the chip, including Watch, Timer and control logic.

Two capacitors C_{IN} and C_{OUT} are integrated on chip – see Figure 5.

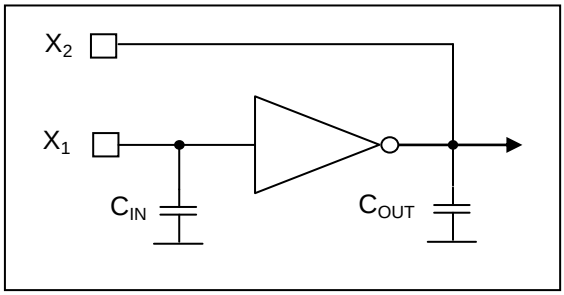


Figure 5: Oscillator Capacitors

9 Power Management

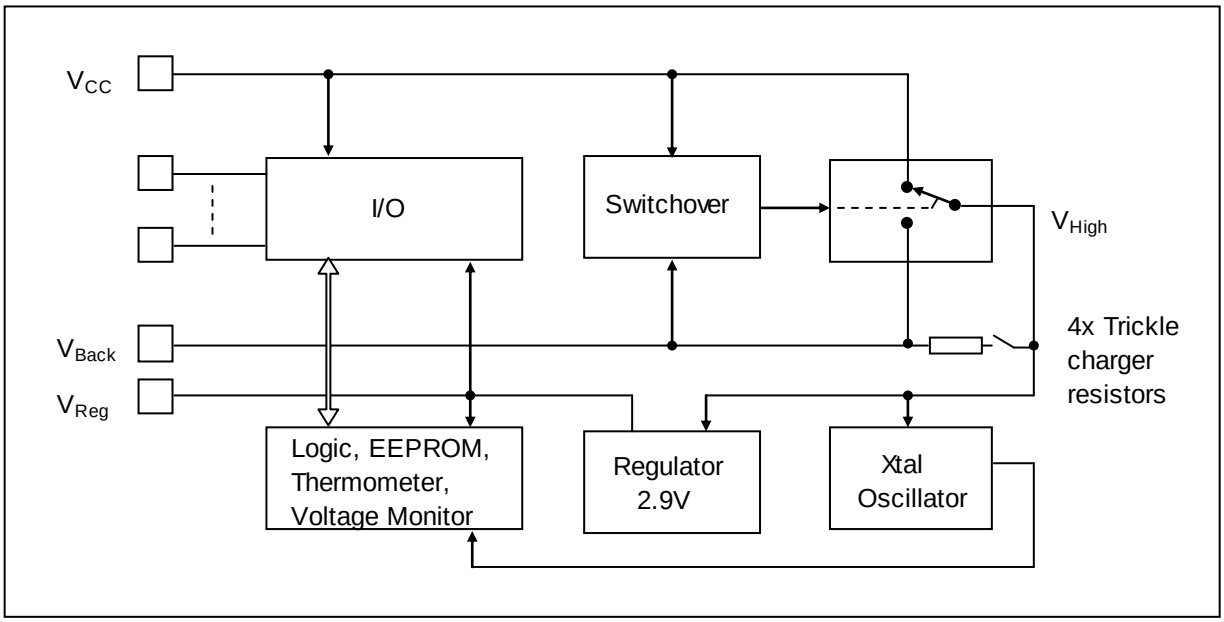


Figure 6: Power Management

9.1 Power Supplies, Switchover and Trickle Charger

The device can be supplied from the V_{CC} pin or from the V_{Back} pin.

The switchover block implemented inside the chip compares V_{CC} and V_{Back} voltages and connects the higher of them to the internal V_{High} net that supplies the chip.

Nevertheless, the communication pins (SCL, SDA or CS, SCK, SI, SO) are supplied from the V_{CC} pin. For that reason, when serial interface (I2C or SPI) is used, the chip has to be supplied from V_{CC}. (i.e. $V_{CC} > V_{Back}$).

By setting of a trickle charger bit in register EEctrl, a resistor can be inserted between V_{Back} and V_{High} voltage. In this way, a rechargeable battery or a super-cap can be charged from the V_{CC} voltage, as long as $V_{CC} > V_{Back}$.

There are 4 selectable resistors connected in parallel with typical values of 80kΩ, 20kΩ, 5kΩ and 1.5kΩ. One or more resistors can be selected by EEctrl bits setting.

If a Lithium battery shall be connected to V_{Back} pin, a protection resistor of value up to 1kΩ can be connected in series with it. In this way, in case of EM3027 device damage resulting in short between both supply pins, charging current from the V_{CC} supply can be reduced to its allowed maximum level as required by UL1642 standard.

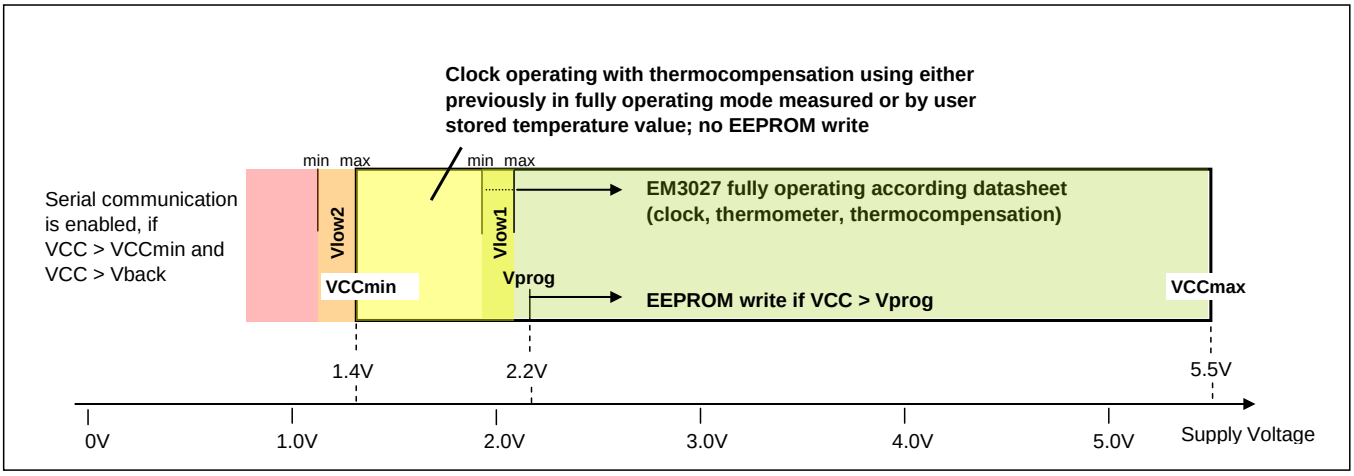


Figure 7: EM3027 operating Voltage Areas

9.2 Low Supply Detection

The supply voltage level is monitored periodically versus Vlow1 and Vlow2 levels. The monitoring rate is one second. When the voltage monitoring is running, a higher current consumption for few milliseconds occurs.

At the power-up of the device, as long as the supply voltage stays below Vlow2, the monitoring rate is accelerated. To enable normal operation, the chip must be supplied with a voltage above Vlow2, to enable the readout of initialization data from EEPROM and to stop the higher current consumption.

When the supply voltage drops from the normal range (from 2.1V to 5.5V) below Vlow1, the VLOW1 status bit is set to '1' by the voltage monitoring system.

When bit VLOW1 is at '1', the thermometer is disabled and the automatic computation of the thermal compensation value (COMP_val) for frequency correction is inhibited. In this case, the last computed compensation value is used.

To leave the VLOW1 status, the supply voltage must be increased above the Vlow1 level and a '0' value must be written into the VLOW1 status bit via the serial interface.

When the supply voltage drops below the Vlow2 level, the VLOW2 status bit is set by the voltage monitoring system.

The VLOW2 status bit disables the read out of the EEPROM.

To leave the VLOW2 status, the supply voltage must be increased above the Vlow2 level and a '0' value must be written into the VLOW2 status bit via the serial interface.

Below Vlow2 level, device functionality is not guaranteed and register contents can be corrupted. Therefore, if VLOW2 status bit is set, it is recommended to perform system reset by writing of '1' into SYSRes bit in RstCtrl page and afterwards update content of Watch, Alarm and Timer registers.

10 AC Characteristics

10.1 AC characteristics – I2C

V_{SS} = 0V and T_A=-40 to +125°C, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Vcc ≥ 3.0V			400	kHz
		Vcc >1.8V			300	
		Vcc>1.4V			100	
Bus Free Time Between STOP and START Condition	t_{BUF}	Vcc ≥ 3.0V	0.6			µs
		Vcc >1.8V	0.8			
		Vcc>1.4V	1.0			
Hold Time (Repeated) START Condition	$t_{HD:STA}$	Vcc ≥ 3.0V	0.3			µs
		Vcc >1.8V	0.4			
		Vcc>1.4V	0.5			
LOW Period of SCL Clock	t_{LOW}	Vcc ≥ 3.0V	1.3			µs
		Vcc >1.8V	1.7			
		Vcc>1.4V	4.5			
HIGH Period of SCL Clock	t_{HIGH}	Vcc ≥ 3.0V	0.6			µs
		Vcc >1.8V	0.7			
		Vcc>1.4V	0.9			
Setup Time START Condition	$t_{SU:STA}$	Vcc ≥ 3.0V	0.3			ns
		Vcc >1.8V	0.4			
		Vcc>1.4V	0.5			
Data Hold Time	$t_{HD:DAT}$	Vcc ≥ 3.0V	0.3			ns
		Vcc >1.8V	0.4			
		Vcc>1.4V	0.5			
Data Setup Time	$t_{SU:DAT}$	Vcc ≥ 3.0V	0.3			ns
		Vcc >1.8V	0.4			
		Vcc>1.4V	0.5			
Data Valid Time	$t_{VD:DAT}$	Vcc ≥ 3.0V	1.2			µs
		Vcc >1.8V	1.5			
		Vcc>1.4V	4.0			
Data Valid Acknowledge Time	$t_{VD:ACK}$	Vcc ≥ 3.0V	0.9			µs
		Vcc >1.8V	1.1			
		Vcc>1.4V	3.5			
Rise Time of Both SDA and SCL Signals	t_R	Vcc ≥ 3.0V			200	ns
		Vcc >1.8V			300	
		Vcc>1.4V			1000	
Fall Time of Both SDA and SCL Signals (See note 1)	t_F	Vcc ≥ 3.0V			200	ns
		Vcc >1.8V			300	
		Vcc>1.4V			400	
Setup Time (Repeated) STOP Condition	$t_{SU:STO}$	Vcc ≥ 3.0V	0.3			ns
		Vcc >1.8V	0.4			
		Vcc>1.4V	0.5			
Length of spikes suppressed by the input filter on SCL and SDA	t_{SP}				50	ns
Capacitive Load For Each Bus Line	C_B				200	pF
I/O Capacitance (SDA, SCL)	$C_{I/O}$				10	pF

Table 13: I2C AC characteristics

Parameters are guaranteed by design. They are not tested in production.

Calculation of external pull–up resistor

The following conditions have to be met:

Rise time is equal to 0.847 R_{PU} (C_B + N * $C_{I/O}$) $\Rightarrow$ $R_{PU} < t_{R\ max} / (0.847\ (C_B + N\ C_{I/O}))$, where N is total number of I/O pins connected to the corresponding bus line.
(t_R in ns, C in pF, R in kΩ)

The minimum value of the pullup resistor value can be calculated with the I_{OL} value of the SDA output:
$R_{PU} = (Vcc - V_{OL}) / I_{OL}$

(I_{OL}: see Table 7, page 5, Output Parameters; e.g. 5mA at V_{CC} = 5.0V, with V_{OL} = 0.8V)

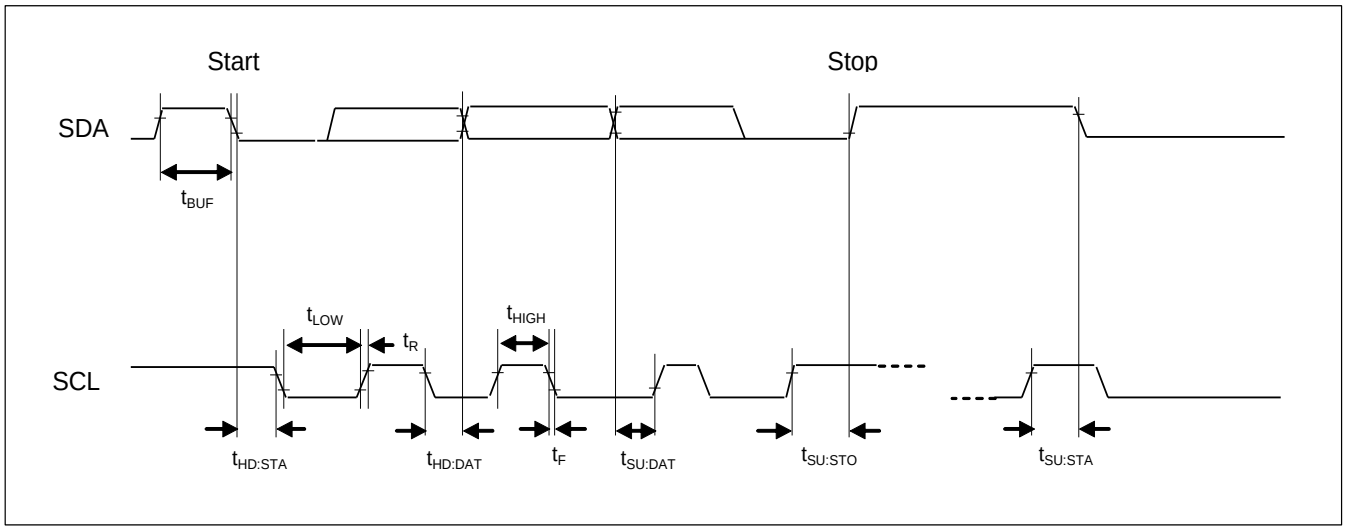


Figure 8: I2C Timing

10.2 I2C Specification compliance

EM3027 device with I2C serial interface was designed in compliance with Philips Semiconductors I^2C-bus specification UM10204 (Rev. 03 – 19 June 2007), Fast-mode class (up to 400kbit/s). Device address consists of 7 bits. Clock stretching is not supported.

Brief manual to I2C interface read and write transmissions is to be found in §7.1.

There are, however, the following discrepancies between I2C specification and EM3027 interface:

1) Falling time on SDA driven by EM3027 can be shorter than 20 + 0.1* C_B ns. (C_B is total capacitive load for SDA bus line in pF) In other words, slope control of falling edges on SDA is missing.

2) Some timing parameters differ from the original I2C specification – refer to Table 13.

10.3 AC characteristics – SPI

V_{SS} = 0V and T_A=-40 to +125°C, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCK Clock Frequency	f_{SCK}	Vcc ≥ 3.0V			1	MHz
		Vcc >1.8V			600	kHz
		Vcc >1.4V			200	
Data to SCK setup	t_{DC}	Vcc ≥ 3.0V				ns
		Vcc >1.8V	20			
		Vcc >1.4V				
SCK to Data Hold	t_{CDH}	Vcc ≥ 3.0V	200			ns
		Vcc >1.8V	300			
		Vcc >1.4V	500			
SCK to Data Valid	t_{CDD}	Vcc ≥ 3.0V			350	ns
		Vcc >1.8V			650	
		Vcc >1.4V			1300	
SCK Low Time	t_{CL}	Vcc ≥ 3.0V	400			ns
		Vcc >1.8V	700			
		Vcc >1.4V	1500			
SCK High Time	t_{CH}	Vcc ≥ 3.0V	400			ns
		Vcc >1.8V	700			
		Vcc >1.4V	1500			
SCK Rise and Fall	t_R , t_F	Vcc ≥ 3.0V			200	ns
		Vcc >1.8V			800	
		Vcc >1.4V				
CS to SCK Setup	t_{CC}	Vcc ≥ 3.0V				ns
		Vcc >1.8V	100			
		Vcc >1.4V				
SCK to CS Hold	t_{CCH}	Vcc ≥ 3.0V	200			ns
		Vcc >1.8V	300			
		Vcc >1.4V	500			
CS Inactive Time	t_{CWL}	Vcc ≥ 3.0V	200			ns
		Vcc >1.8V	300			
		Vcc >1.4V	400			
CS to Output High Impedance	t_{CDZ}	Vcc ≥ 3.0V			50	ns
		Vcc >1.8V			100	
		Vcc >1.4V			200	

Table 14: SPI AC characteristics

Parameters are guaranteed by design. They are not tested in production.

1) Max. bus capacitance on SO line shall be lower than 100pF when Vcc > 1.8V and lower than 50pF when Vcc < 1.8V.
2) Spikes on SCK signal shorter than 20ns are suppressed.

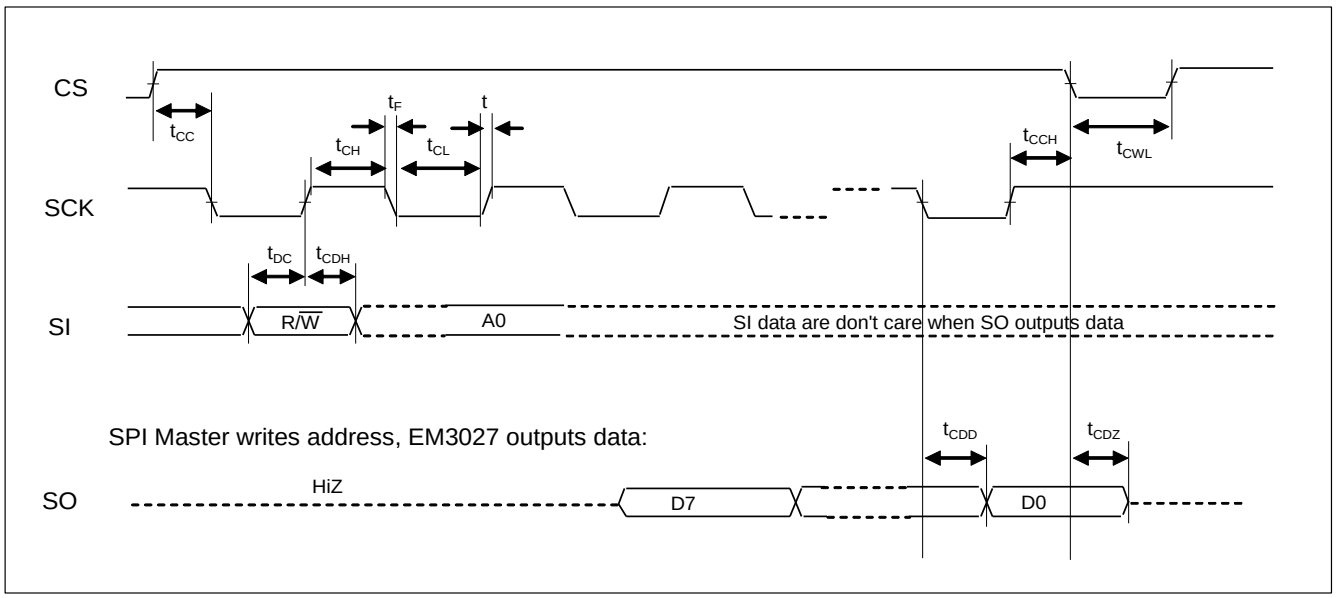


Figure 9: SPI Read Timing

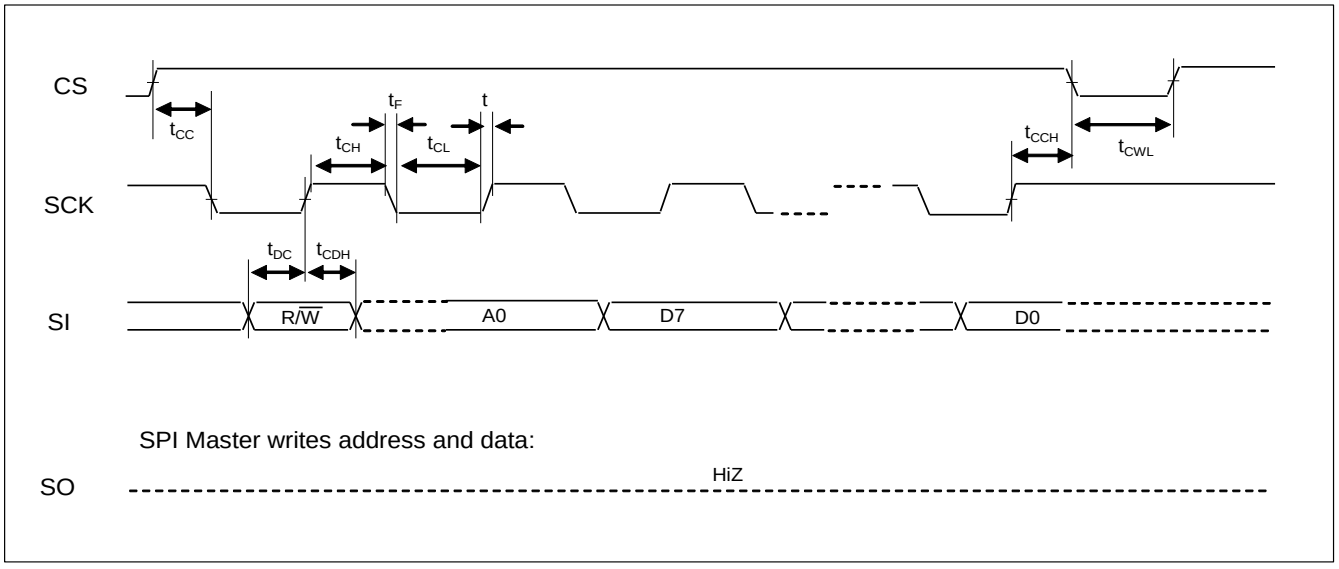
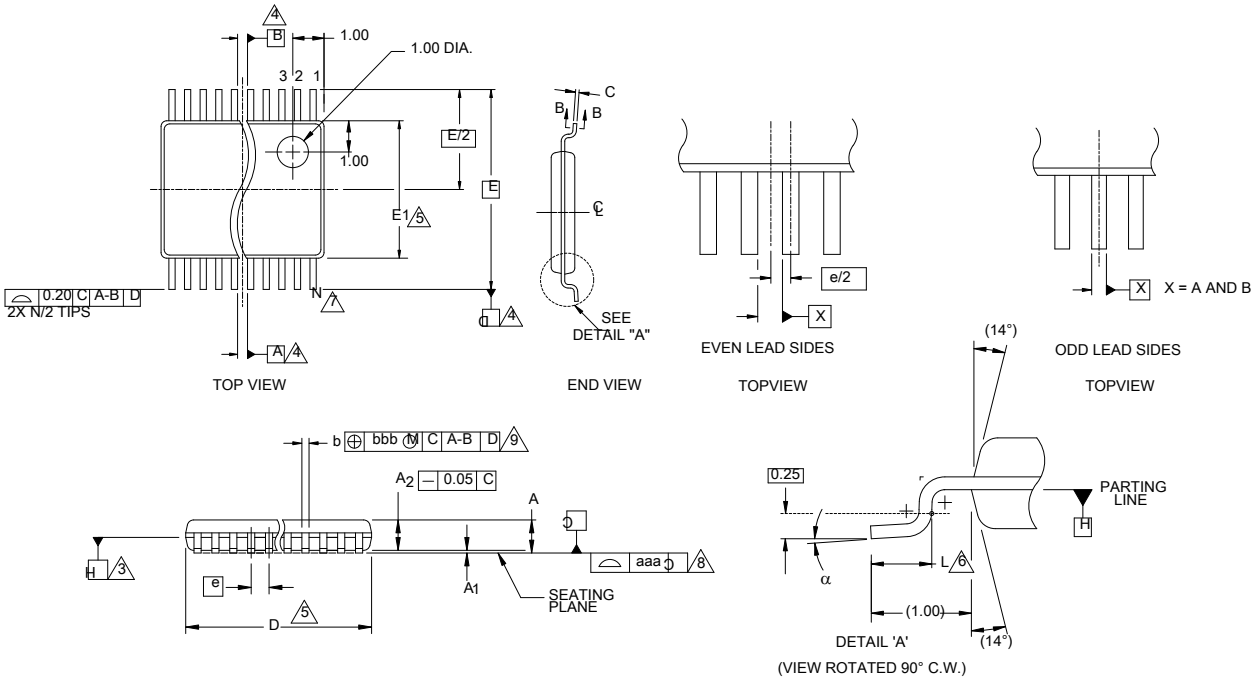


Figure 10: SPI Write Timing

11 Package Information

11.1 TSSOP-08/14

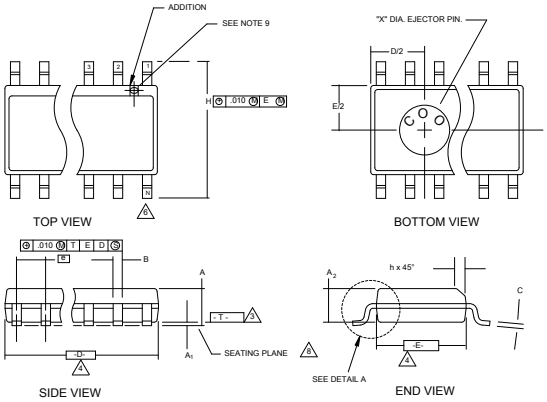


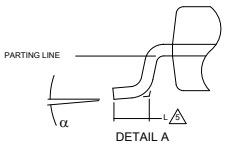
SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARI-ATIONS	5					7
						D			P	P1	N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	MAX.	MAX.	
A	———	———	1.10			2.90	3.00	3.10	1.59	3.2	8
A1	0.05	———	0.15			4.90	5.00	5.10	3.1	3.0	14
A2	0.85	0.90	0.95								
aaa		0.076									
b	0.19	-	0.30	9							
b1	0.19	0.22	0.25								
bbb		0.10									
c	0.09	-	0.20								
c1	0.09	0.127	0.16								
D	SEE VARIATIONS			5							
E1	4.30	4.40	4.50	5							
e	0.65 BSC										
E	6.40 BSC										
L	0.50	0.60	0.70	6							
N	SEE VARIATIONS			7							
P	SEE VARIATIONS										
P1	SEE VARIATIONS										
α	0°	———	8°								

ALL DIMENSIONS IN MILLIMETERS

NOTES:
1. DIE THICKNESS ALLOWABLE IS 0.279±0.0127
2. DIMENSIONING & TOLERANCES PER ASME. Y14.5M-1994.
3. DATUM PLANE H LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
4. DATUM A-B AND D TO BE DETERMINED WHERE CENTERLINE BETWEEN LEADS EXITS PLASTIC BODY AT DATUM PLANE H.
5. "D" & "E1" ARE REFERENCE DATUM AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, AND ARE MEASURED AT THE BOTTOM PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D AND 0.25mm ON E PER SIDE.
6. DIMENSION IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY.
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.076mm AT SEATING PLANE.
9. THE LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.07mm TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND AN ADJACENT LEAD SHOULD BE 0.07mm

11.2 SO-8





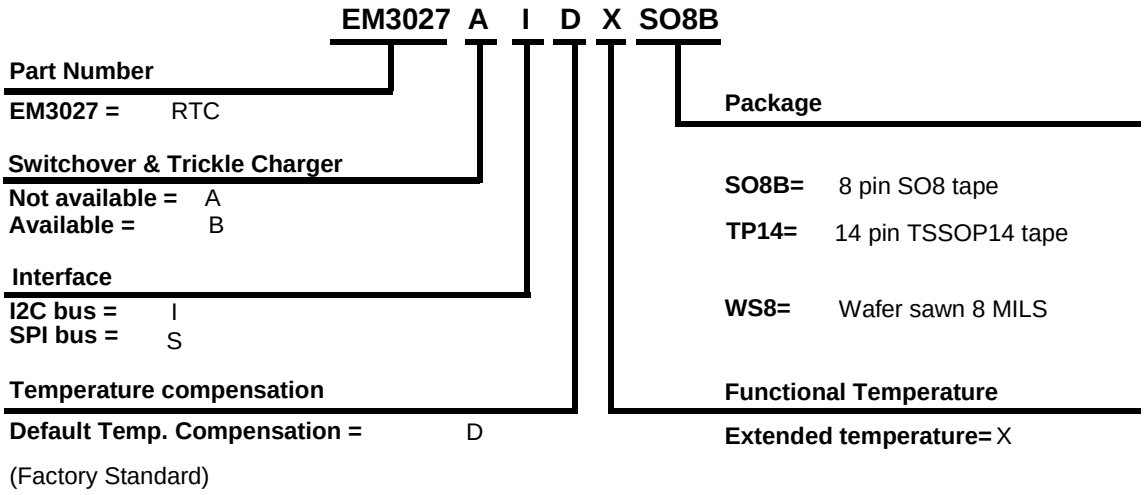
SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE
A	1.55	1.63	1.73	
A_1	0.127	0.15	0.25	
A_2	1.40	1.47	1.55	
B	0.35	0.41	0.49	
C	0.19	0.20	0.25	
D	4.80	4.93	4.98	3
E	3.81	3.94	3.99	
e		1.27 BSC		
H	5.84	5.99	6.20	
h	0.25	0.33	0.41	
L	0.41	0.64	0.89	
N		8		5
α	0°	5°	8°	
X	2.16	2.36	2.54	

THIS TABLE IN MILLIMETERS

NOTES:

1. MAXIMUM DIE THICKNESS ALLOWABLE IS .015.
2. DIMENSIONING & TOLERANCES PER ANSI.Y14.5M - 1982.
3. "T" IS A REFERENCE DATUM.
4. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS, BUT DOES INCLUDE MOLD MISMATCH AND ARE MEASURED AT THE MOLD PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES AT END AND .010 INCHES AT WINDOW
5. "L" IS THE LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
6. "N" IS THE NUMBER OF TERMINAL POSITIONS.
7. TERMINAL POSITIONS ARE SHOWN FOR REFERENCE ONLY
8. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN .003 INCHES AT SEATING PLANE.
9. THE APPEARANCE OF PIN #1 I.D ON THE 8 LD IS OPTIONAL, ROUND TYPE ON SINGLE LEADFRAME AND RECTANGULAR TYPE ON MATRIX LEADFRAME.

12 Ordering Information



Standard Versions

Part Number	Package	Functional Temperature	Interface	Delivery Form	Marking
EM3027AIDXWS8		-40 +125°C	I2C	Sawn 8 mils on Blue foil	
EM3027BIDXSO08B+	SO8	-40 +125°C	I2C	Tape & Reel, 2500 pcs	3027X5
EM3027BIDSSO08B+	SO8	-40 +85°C	I2C	Tape & Reel, 2500 pcs	3027 5
EM3027BSDXTP14B+	TSSOP14	-40 +125°C	SPI	Tape & Reel, 3500 pcs	3027X6
EM3027BSDSTP14B+	TSSOP14	-40 +85°C	SPI	Tape & Reel, 3500 pcs	3027 6

Please contact Sales office for other versions not shown here and for availability of non standard versions.