1 kbit Read/Write, ISO 18000-6C / EPC C-1 G-2 Passive / Battery-assisted Contactless IC

Description

EM4324 is a long range passive / battery-assisted UHF RFID tag IC compliant with the ISO 18000-6C / EPCglobal Class-1 Generation-2 protocol. The chip offers an advanced feature set (EPC+) leading to a performance beyond that of standard Gen2 chips. Battery-assisted, EM4324 offers superior reading range and reliability compared to purely passive RFID solutions. The battery-assisted mode is tailored to harsh environment applications where other passive UHF solutions fail e.g. in the presence of water or metal.

The EM4324 current consumption has been optimized to maximize battery lifetime. Even if the battery is flat, the chip continues to operate and communicate with the reader in passive mode.

The memory size is 1024 bits enabling support of ISO or EPC data structures. Each chip is delivered with a 64-bit Unique Identifier to ensure full traceability.

The EM4324 includes a tamper detection circuit to support E-seal applications. Tamper detection can be implemented using a simple continuity loop, with heat sensitive fuse wire, with sensors having both high and low impedance states, or with external devices controlling an electronic switch such as a MOSFET.

Applications

- Supply chain management
- Tracking and tracing
- Containers identification
- Access control
- Asset control
- E-seals

Features

- ISO 18000-6C compliant
- EPC Class-1 Gen-2 compliant
- 1024-bit non-volatile memory
- 720-bit user's free memory
- 96-bit EPC numbers supported
- 64-bit manufacturer-programmed Unique Identifier (TID / UID)
- Forward link data rates: 40 to 160 kbit/s
- Return link data rates: 40 to 640 kbit/s
- Tamper detection
- Battery assistance mode for unsurpassed reading range and reading reliability
- Rectifier that allows passive operation in case the battery is flat or not present
- Support of near-field mode enabling reading e.g. through water
- Support of parallel-inductance matching for improved matching
- 32-bit password-protected Kill command
- 32-bit password-protected Access command
- Anti-tearing feature to prevent malicious unlocking
- Extended temperature range (–40°C to +85°C)
- Available also in TSSOP-8 package

Typical Operating configuration

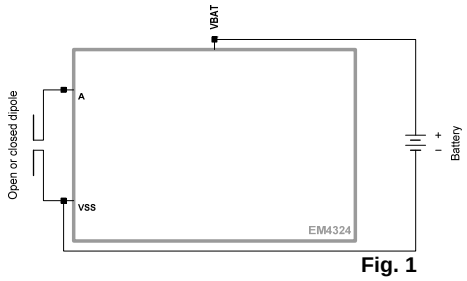


Fig. 1

IC Block Diagram

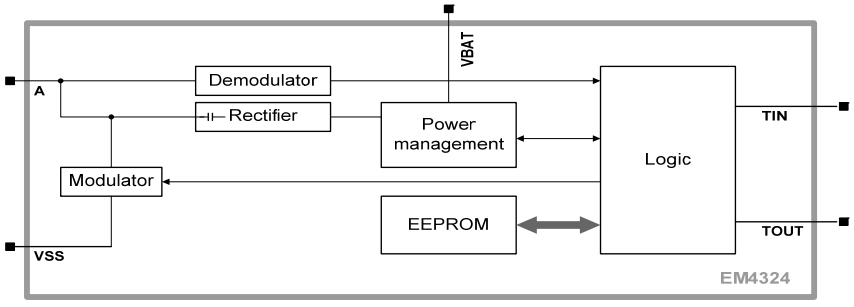


Fig. 2

Absolute Maximum Ratings

Parameters	Symbol	Min.	Max.	Unit
Operating temperature	T_{OP}	-40	85	°C
Storage temperature	T_{STORE}	-50	150	°C
Voltage on pad A	V_{A_ABS}	V_{SS}-0.3	V_{SS}+3.6	V
Voltage on pad VBAT	V_{BAT_ABS}	V_{SS}-0.3	V_{SS}+3.6	V
Voltage on pad VSS	V_{SS}	-	-	V
RF power at pad A	P_{A_ABS}		20	dBm
Voltage on pad TST, TST2, TIN, TOUT	V_{TST_ABS}	V_{SS}-0.3	V_{SS}+3.6	V
DC current into pads except pad A	I_{ABS}	-98	98	mA
DC current into pad A	I_{A_ABS}	-20	20	mA
Electrostatic discharge on pad A[1)]	V_{ESD_A}	-1250	1250	V
Electrostatic discharge on pad VBAT[1)]	V_{ESD_VBAT}	-2000	2000	V

Table 1

Note 1: Human Body Model (HBM; 100pF; 1.5kOhm) with reference to substrate VSS.

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameters	Symbol	Min.	Max.	Unit
Operating temperature	T_{OP}	-40	+85	°C
Battery operating voltage (between VBAT and VSS)	V_{BAT}	1.25	3.3	V
RF power at pad A (antenna impedance conjugate complex to Z_{A_PAS})	P_A		5	dBm
RF carrier frequency	f_A	860	960	MHz

Table 2

Electrical Characteristics

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Battery operating voltage for read	V_{BAT_RD}	V_{BAT} > 1.4V during 100µs at T=25°C when applying V_{BAT}	1.25		3.3	V
Battery operating voltage for write	V_{BAT_WR}		2		3.3	V
Average battery current in Sleep mode	$I_{BAT\_S\_A}$	V_{BAT}=1.5V, T=25°C V_{BAT} = 3V, T=25°C		0.6 0.9	0.9 1.4	uA uA
Average battery current in Ready state	$I_{BAT\_R\_A}$	V_{BAT}=1.5V, T=25°C V_{BAT} = 3V, T=25°C		11 22	25 40	uA uA
Depth to which the carrier is modulated	K_M		65		100	%
Input impedance (between A and VSS) below passive activation threshold[1]; to be used for antenna matching optimized for battery-assisted mode	Z_{A_BAT}	battery-assisted mode P_{DUT}=-27dBm T = 25°C f_A = 868MHz f_A = 915MHz f_A = 956MHz		 11-j164 11-j155 11-j148		 Ω Ω Ω

Table 3

[1] The activation threshold is defined as the RF power level above which the chip starts operating and is equal to or lower than the read sensitivity

Electrical Characteristics (continued)

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input impedance (between A and VSS) above passive activation threshold; to be used for antenna matching optimized for passive mode	Z_{A_PAS}	passive mode (no battery) P_{DUT}=-10dBm T = 25°C f_A = 868MHz f_A = 915MHz f_A = 956MHz		 19-j188 18-j178 17-j170		 Ω Ω Ω
TSSOP-8 input impedance (between A and VSS) below passive activation threshold[2] (impedance only valid for TSSOP-8 package option!)	Z_{A_TSSOP}	P_{DUT}=-27dBm T = 25°C f_A = 868MHz f_A = 915MHz		 21-j145 22-j135		 Ω Ω
Input impedance (between A and VSS) when modulator is on	Z_{A_ON}	battery-assisted mode (V_{BAT}=1.1V) P_{DUT}=-27dBm T = 25°C f_A = 868MHz f_A = 915MHz f_A = 956MHz		 62-j25 61-j26 60-j27		 Ω Ω Ω
Read sensitivity for power matching (complex-conjugate matching) in passive mode	P_{WU_PAS}	Passive mode f_A=868MHz f_A=915MHz		 -9 -8		 dBm dBm
Read sensitivity for power matching (complex-conjugate matching) in battery-assisted mode	P_{WU_BAT}	Battery-assisted mode; 1.2<V_{BAT}<2.0V T = 25°C f_A=868MHz f_A=915MHz		 -27 -27		 dBm dBm
Battery-low voltage	V_{BAT_LOW}		1.15	1.2	1.25	V

Table 4

Timing Characteristics

Parameters	Symbol	Conditions	Min.	Typ.	Max.	Unit
Erase / write endurance	T_{CYC}		10k			Cycles
Retention	T_{RET}	T_{OP} = 55ºC	10			Years
Write time for 16 bits / 1 word	T_{WR}		6.1	7.2	8.3	ms
RF fade control time	T_{FADE}	Battery-assisted mode	40	80	175	ms

Table 5

[2] The activation threshold is defined as the RF power level above which the chip starts operating and is equal to or lower than the read sensitivity

Functional Description

Memory Organization

Memory name	Memory bank	16-bit bank word (decimal)	16-bit physical word (decimal)	Contents
RESERVED	00_2	0	0	Kill password
		1	1	
		2	2	Access password
		3	3	
TID	10_2	0	4	TID / UID
		1	5	
		2	6	
		3	7	
EPC	01_2	0	RAM	CRC-16
		1	8	PC
		2	9	EPC
		3	10	
		4	11	
		5	12	
		6	13	
		7	14	
USER	11_2	0-44	15-59	User data
SYSTEM		45	60	System configuration
		46	61	N/A
		47	62	N/A
		48	63	N/A

Table 6: Memory map

The 64-bit TID / UID is programmed and perma-write-locked during manufacturing and before customer delivery. This guarantees the uniqueness of each device on the market. The custom command GetUID allows fast access of the UID and provides more confidence in the uniqueness.

Memory name bank	SYSTEM / 11_2															
16-bit bank word	45_{10} ($2D_{16}$)															
Bits (MSB first)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
Content	N/A													Tamper Status	Battery Low	N/A

Table 7

Content	Description
Tamper Status	Volatile bit set to 1 when tamper condition is present
Battery Low	Volatile bit set to 1 when the battery is low i.e. when $V_{BAT} < V_{BAT\_LOW}$

Table 8

EEPROM Delivery state

The default configuration is as follows:

- Unique Identification number (UID / TID)
  - Version without tamper detection has value E200'B001'XXXX'XXXXh where XXXX'XXXXh is a 32-bit serial number
  - Version with tamper detection has value E200'B002'XXXX'XXXXh where XXXX'XXXXh is a 32-bit serial number
- EPC at value 0000'0000'0000'0000'0000'0000h
- User data words 0-43 are set to 0000h, User data word 44 is set to an arbitrary value

Commands

Command types

Three sets of commands are defined:

- Mandatory
- Optional
- Custom

Command codes

The table below shows all implemented commands in EM4324. For the description of all mandatory and optional commands, please refer to the EPCglobal Class-1 Gen-2 standard. More detailed information on the GetUID custom command is given further below.

Command code	Type	Function
'00'	Mandatory	QueryRep
'01'	Mandatory	ACK
'1000'	Mandatory	Query
'1001'	Mandatory	QueryAdjust
'1010'	Mandatory	Select
'11000000'	Mandatory	NAK
'11000001'	Mandatory	Req_RN
'11000010'	Mandatory	Read
'11000011'	Mandatory	Write
'11000100'	Mandatory	Kill
'11000101'	Mandatory	Lock
'11000110'	Optional	Access
'11100000 00000000'	Custom	GetUID

Table 9

GetUID custom command

	Command code	RN
# of bits	16	16
Description	11100000 00000000	Prior RN16 or handle

Table 10

The custom command GetUID is implemented as in **Table 10**. It allows an interrogator to read the tag's 64-bit TID / UID with a single command.

A tag in Reply, Acknowledged, Open or Secured state backscatters {'0', TID / UID, RN16, CRC-16} upon a GetUID command with a valid RN16 or handle (see **Table 11**). The state transition and link timing is the same as for the Ack command. The tag reply is analogous to the tag reply upon a Read command. A link timing example is shown in Fig. 3.

	Header	UID	RN	CRC-16
# of bits	1	64	16	16
Description	0	TID / UID	RN16 (prior RN16 or handle)	CRC-16('0'+TID+RN16)

Table 11

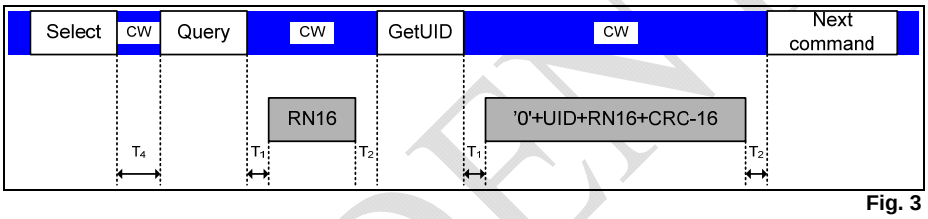


Fig. 3

Battery assistance

The pad VBAT allows supplying the chip with an external battery. In case the battery is flat or not present, the chip is supplied by the RF signal on pad A (passive mode). The chip is in Sleep mode in case the RF signal on pad A is below the sensitivity level and behaves like a passive chip below wake-up i.e. it does not reply to any command. The wake-up from Sleep mode corresponds to a power-up of a passive EPC chip and is triggered by the presence of an RF field above the sensitivity level. The chip implements an RF fade control mechanism to overcome momentary nulls that may occur in the RF field. This allows for more reliable sustained communications when operating at very long ranges. The RF fade control time is the time duration that starts when the RF signal on pad A drops below the sensitivity level and ends when the chip declares a loss of the RF field and transition to Sleep mode.

Near-field mode / parallel resonance matching

By using an inductive coil between the pad A and VSS, it is possible to magnetically couple the chip to an interrogator as used in HF / LF RFID applications. The magnetic / near-field coupling is used to overcome some limitations of electromagnetic / far-field scattering. It is e.g. possible to establish a link through water and other materials that greatly reflect the electromagnetic field but not the magnetic field.

To facilitate the near-field mode an on-chip AC coupling capacitor is implemented so that the coil between the pad A and VSS can be used without the need for an external AC coupling capacitor.

Tamper Detection

Tamper detection is an optional feature. It is included for all packaged devices and is optional for wafers depending upon the version ordered. The pads/pins TIN and TOUT may be connected via a simple continuity loop, with heat sensitive fuse wire, with sensors having both high and low impedance states, or with external devices controlling an electronic switch such as a MOSFET. The connectivity between TIN and TOUT is checked when the device detects an RF field and enters the Ready state to start communications with a reader. If low impedance is detected, then the *Tamper status* bit is set, otherwise it is cleared. A reader may then read User Memory word 45_{10} ($2D_{16}$) to determine if a tamper condition exists.

Chip floor plan

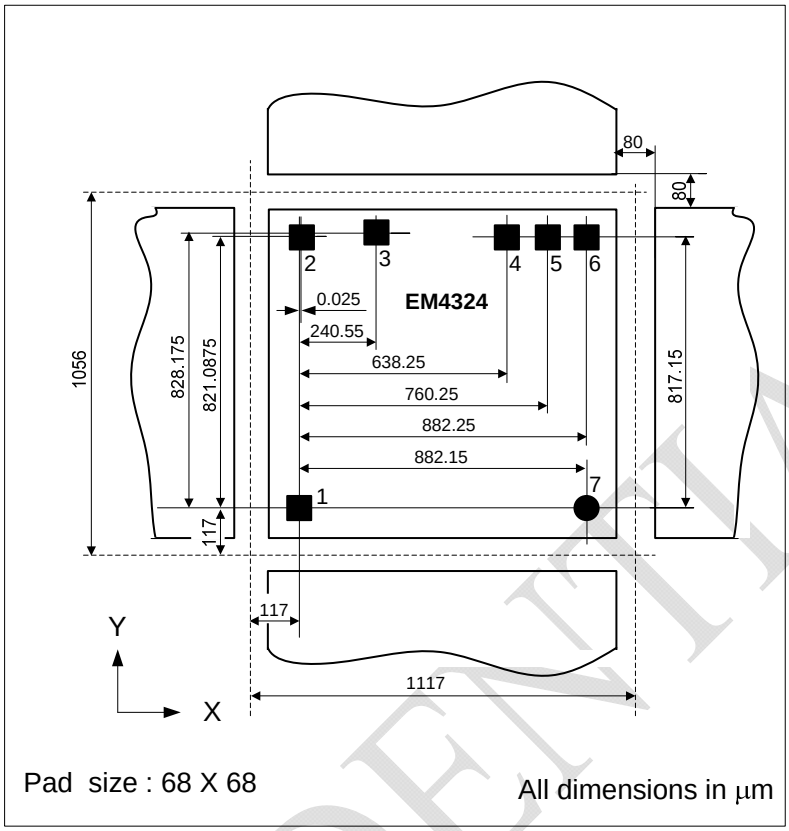


Fig. 4

Pad description

Pad	Name	Description
1	VSS	Antenna and battery-
2	VBAT [2)]	Battery+
3	TST [2)]	N/A - Test purpose only
4	TST2 [3)]	N/A - Test purpose only
5	TIN [3)]	Tamper input
6	TOUT [3)]	Tamper output
7	A	Antenna+

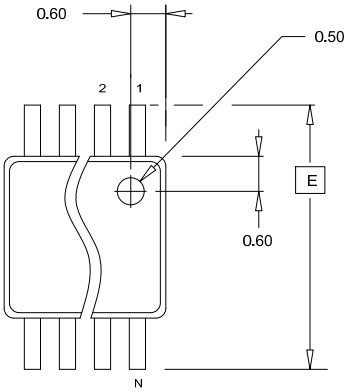
Table 12

Note 2: The pads VBAT and TST can be shorted together to ease inlay assembly
Note 3: The pads TST2, TIN and TOUT can be shorted together to ease inlay assembly (not so for tamper detection versions)

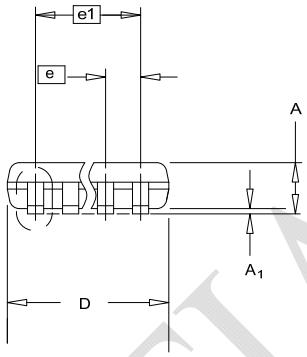
Package information:

EM4324 is available in TSSOP-8 package. More details on package dimensions, pin-out and ordering information are below.

Package dimensions



TOP VIEW



SIDE VIEW

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	———	———	1.10	
A_1	0.05	0.10	0.15	
D	3.00 BSC			
E	4.90 BSC			
e	0.65 BSC			
e1	1.95 BSC			
N	8			

Fig. 5

Note 4: BSC - Basic spacing between centers

TSSOP-8 Pin description

Pin	Name	Description
1	A	Antenna+
2	NC	NC
3	TOUT	Tamper output
4	TIN	Tamper input
5	TST2	N/A
6	TST	N/A
7	VBAT	Battery+
8	VSS	Antenna and battery-

Table 13

Package Ordering Information

Part Number	Tamper Detection	Package	Delivery Form
EM4324V2TP8B+	Yes	TSSOP-8	Tape

Table 14

Ordering Information

The following charts show the general offering. For detailed Part Number to order, please see the table "Standard Versions" below.

Die form

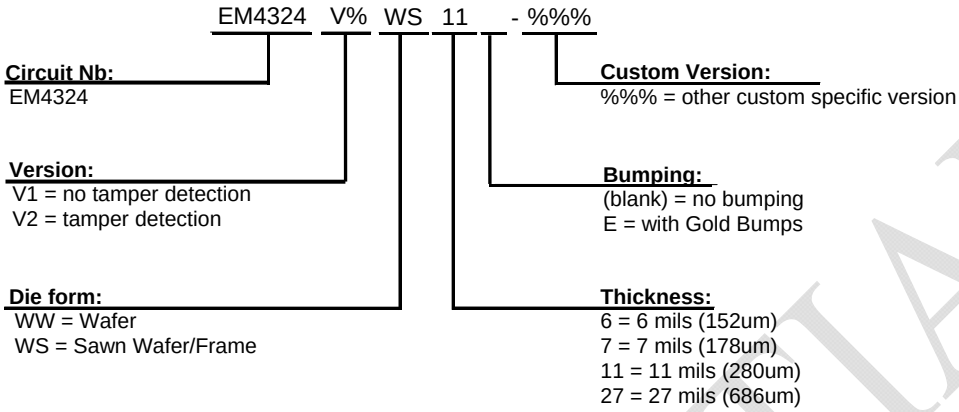


Fig. 6

Remarks:

- For ordering, please, use table of "Standard Version" table below.
- For specifications of Delivery Form, including gold bumps, tape and bulk, as well as possible other delivery form or packages, please, contact EM Microelectronic-Marin S.A.

Standard Versions & Samples:

For samples, please, order exclusively:
The versions below are considered standards and should be readily available. For other versions or other delivery form, please contact EM Microelectronic-Marin S.A.

Part Number	Tamper Detection	Package/Die Form	Delivery Form
EM4324V1WS7E	No	Sawn wafer / bumped die – thickness of 7 mils	Wafer sawn on frame
EM4324V2WS7E	Yes	Sawn wafer / bumped die – thickness of 7 mils	Wafer sawn on frame
EM4324VXYYY-%%%		Custom	Custom

Table 15

Product Support

Check our web site under Products/RF Identification section. Questions can be sent to info@emmicroelectronic.com.