128 bit Read Only Low Frequency Contactless Identification Device

Description

EM4200 is a CMOS integrated circuit intended for use in electronic Read Only RF transponders. It is designed to replace directly the EM Microelectronic-Marin Read Only ICs EM4100/4102 and EM4005/4105.

Comparing to EM4100/4102 and EM4005/4105, the chip provides higher reading range performances and presents on its coil terminals a 250pF resonant capacitor (selectable by mask option).

The 128 bit unique code is stored in laser programmed ROM. Several options are available to use 64, 96 or 128 bits of ROM.

The circuit is powered by an external coil placed in an electromagnetic field and gets its master clock from the same field. By turning on and off the modulation current, the chip will send back the unique code contained in a factory pre-programmed laser ROM.

Features

- Full compatible with EM4100/4102 and EM4005/4105 communication protocols.
- 128 bit laser programmed ROM (64 and 96 bit option available)
- Several options of data rate and data encoding:
  - Manchester 32 and 64 RF clocks per bit
  - Biphase 32 and 64 RF clocks per bit
  - PSK 16 RF clocks per bit (subcarrier RF/2)
  - FSK2 50RF clocks per bit
- Several resonant capacitor integrated on chip (0pF, 75pF or 250pF mask option)
- 100 to 150 kHz frequency range
- On-chip rectifier and voltage limiter
- No external supply buffer capacitor needed
- -40°C to +85°C temperature range
- Very low power consumption and High performances

Applications

- Animal Identification according to ISO11785 (FDX-B)
- Waste management standard (BDE)
- Access Control
- Logistics automation
- Anticounterfeiting
- Industrial transponder

Typical Operating Configuration

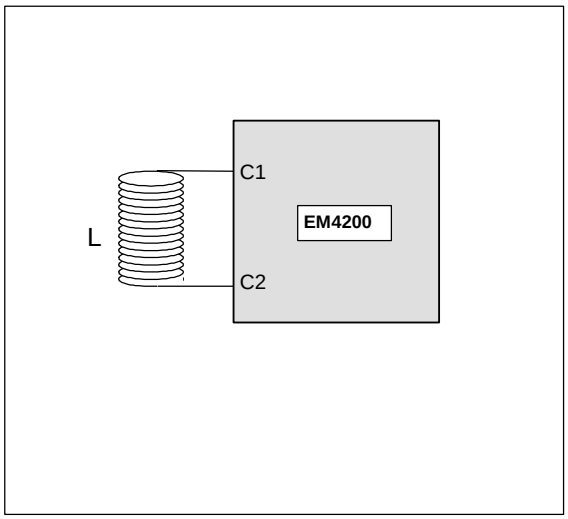


Fig. 1

Absolute Maximum Ratings

V_{SS} = 0V

Parameter	Symbol	Conditions
Input current on COIL1/COIL2	I_{COIL}	-30 to +30mA
Operating temperature range	T_{OP}	-40 to +85°C
Storage temperature range	T_{STORE}	-55 to +125°C
Electrostatic discharge to MIL-STD-883 method 3015 Between Coil1 and Coil2	V_{ESD}	2000V

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Electrical parameters and functionality are not guaranteed when the circuit is exposed to light.

Handling Procedures

This device has built-in protection against high static voltages or electric fields. However due to the unique properties of this device, anti-static precautions should be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

Operating Conditions

V_{SS} = 0V

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature	T_{OP}	-40	+25	+85	°C
AC voltage on coil pins	V_{COIL1}			(note)	V_{pp}
Maximum coil current	I_{COIL1}	-10		10	mA
Frequency on coil pins	F_{COIL1}	100	125	150	kHz

Table 2

Note: Maximum voltage is defined by forcing 10mA on Coil1 – Coil2

Electrical Characteristics

V_{SS} = 0 V, f_{COIL1} = 125 kHz square wave, V_{COIL1} = 1.5V_P, T_{OP} = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Limiter voltage	V_{LIM}	I ($_{COIL2}$ - $_{COIL1}$) = ±10mA	6.9	8.0	9.3	V
Resonance capacitor “Ver 250pF”	C_R		225	250	275	pF
Resonance capacitor “Ver 75pF”	C_R		67.5	75	82.5	pF

Table 3

Note: Statistics show a variation of capacitance within a wafer of ±3%

Timing Characteristics

V_{SS} = 0 V, f_{COIL1} = 125 kHz square wave, V_{COIL1} = 1.5V_P, T_{OP} = -40 to +85°C, unless otherwise specified
Timings are derived from the field frequency and are specified as a number of RF periods.

Parameter	Symbol	Test Conditions	Value	Units
Read Bit Period	T_{rdb}	depending on option	64, 50, 32 and 16	RF periods

Table 4

Block Diagram

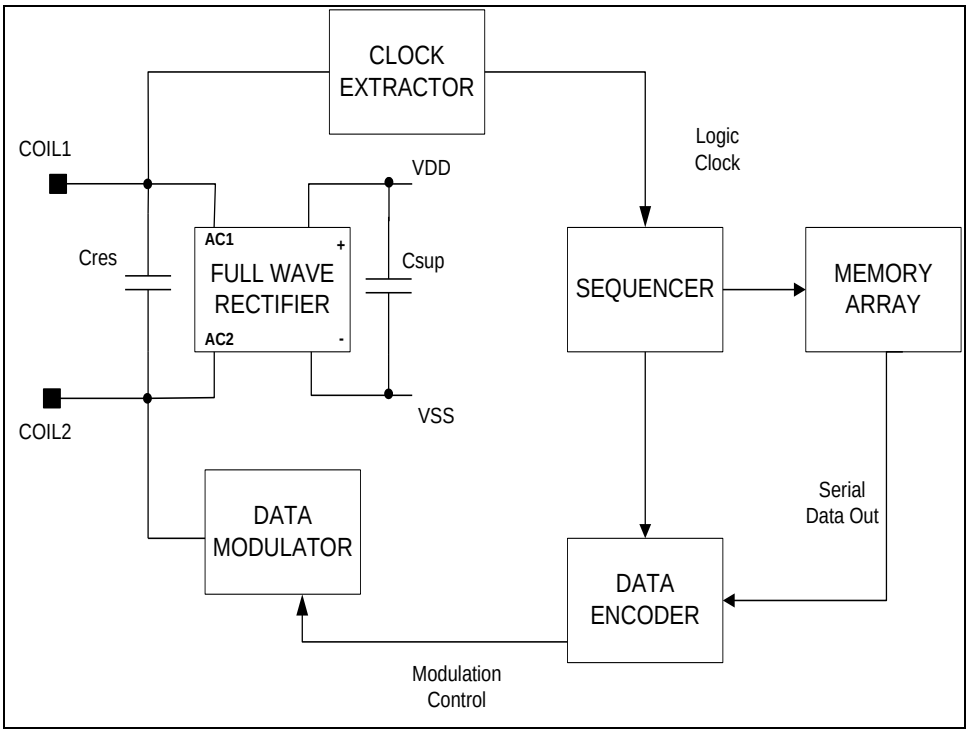


Fig. 2

Functional Description

General

The EM4200 is supplied by means of an electromagnetic field induced on the attached coil. The AC voltage is rectified in order to provide a DC internal supply voltage. When the DC voltage is sufficient the chip sends data continuously. When the last bit is sent, the chip will continue with the first bit until the power goes off.

Full Wave Rectifier

This block integrates an AC/DC converter, which extracts the DC power from the incident RF field. It also acts as limiter, which clamps the voltage on coil terminals to avoid chip destruction in strong RF fields

Clock extractor

One of the coil terminals (COIL1) is used to generate the master clock for the logic function. The output of the clock extractor drives a sequencer.

Sequencer

The sequencer provides all necessary signals to address the memory array and to encode the serial data out. The data rate is set according to data rate option.

Memory

The memory contains 128 bits laser programmed during manufacturing. The bits are read serially and are passed to Data Encoder. There are metal options available to reduce number of bits read from ROM (64 or 96).

Data Encoder

Encoder encodes serial NRZ data before it is transmitted to the Data Modulator. It has several options implemented to give different codes, which are frequently used in RFID (Manchester, Biphase, PSK).

Data Modulator

The data modulator is controlled by the signal Modulation Control in order to induce a high current on COIL2 terminal when this signal is at logic "1". This will affect the magnetic field according to the data stored in the memory array.

Description of encoding options:

Manchester:

In Manchester coding, there is a transition from High to Low or from Low to High in the middle of the bit period. When logic 0 is transmitted first half of bit period the output is Low and second half of bit period it is High. When logic 1 is transmitted, the first half of the bit period the output is High and second half of bit period it is Low.

Data rates of 32 and 64 RF periods per bit are available.

Biphase:

In Biphase coding, there is a transition from High to Low or from Low to High at the beginning of each bit period. In the case logic 0 is transmitted there is additional transition in the middle of bit period. In case logic 1 is transmitted there is no transition in the middle of bit period

Data rates of 32 and 64 RF periods per bit are available.

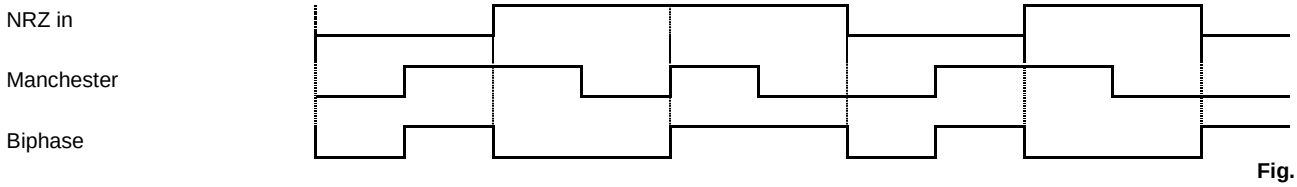


Fig. 3

PSK:

The data rate of PSK mode is set to 16 periods of field frequency (RF/16) while sub-carrier frequency is set to RF/2.

A phase shift occurs every time a logic 0 is read from memory.

When phase change occurs, the current position of the modulator switch is maintained one period of RF field longer. Since number of clocks between phase changes is even, this means that at phase changes a state with two RF periods of modulator switch ON and a state with two RF periods of modulator switch OFF alternate.

Double pulse lockout feature (metal option) delays every second phase change for one RF clock so that all phase changes are done with modulator switch OFF. The results of this feature is that modulator switch ON time is never longer then one period of RF clock which may slightly increase operating distance of transponder.

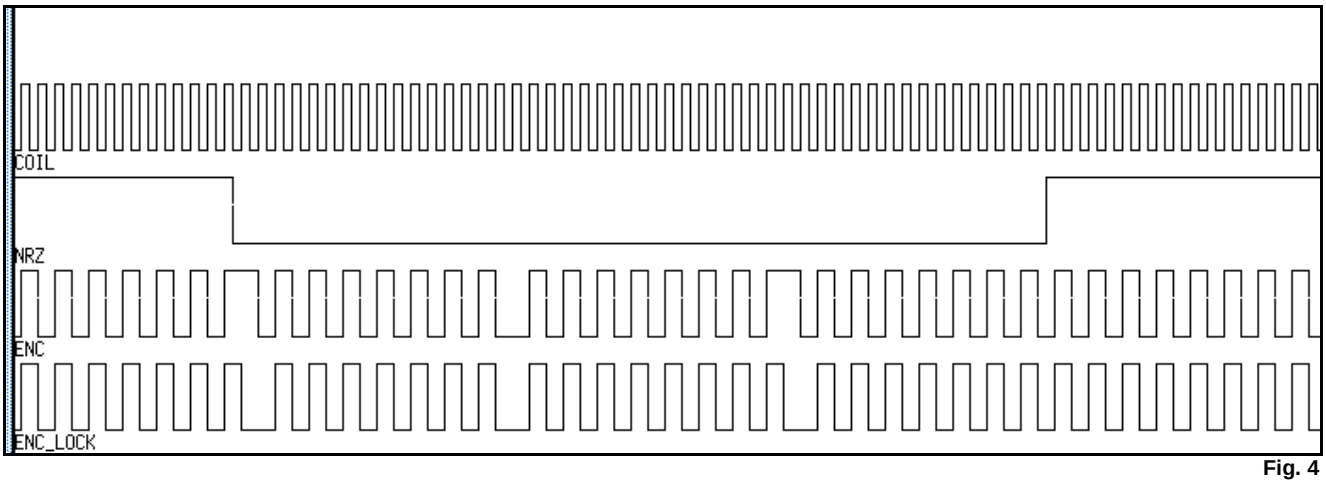


Fig. 4

Figure above presents a logic simulation of PSK code with and without double pulse lockout feature. Signal COIL is clock signal extracted from the RF signal induced on transponder coil. 16 periods of signal COIL presents duration of one bit. Signal NRZ is NRZ data input to PSK encoder. A logic one is followed by three zeros and a transition back to one.

Signal ENC is PSK encoded signal without double pulse lockout feature. A logic high level of this signal puts modulator switch ON. Signal ENC_LOCK is PSK encoded signal with double pulse lockout feature. In case phase change of signal ENC happens during modulator switch ON it is delayed for one clock, in case it happens during modulator switch OFF it remains unchanged.

FSK2:
The state of the memory bit will determine the frequency of the transmitted data.

- A logic 1 is represented by 48 or 52 cycles of amplitude modulated $f_{RF}/8$.
- A logic 0 is represented by 50 cycles of amplitude modulated $f_{RF}/10$.

Code	Logic 1	Logic 0
FSK2	$f_{RF}/8$	$f_{RF}/10$

Table 5

To prevent glitches in the decoded data, $F_{RF}/8$ will toggle between 48 and 52 cycles as shown in figure 5.

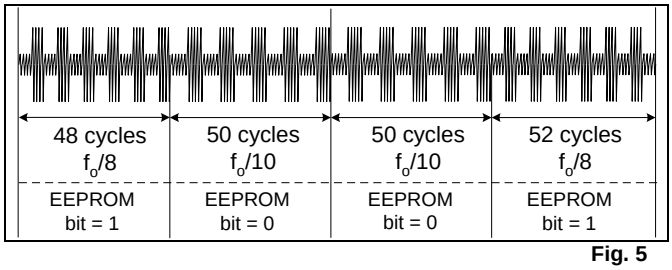


Fig. 5

Description of implemented versions:

ISO11785 FDX-B

For this version data rate is set to 32 RF clocks per bit, data encoding is biphase, 128 bit of ROM are used.

128 bits of ROM are programmed according to ISO11785 standard:

Memory organization
The structure of the 128 bits is as follows :

The header is sent first and is used to identify the start of the sequence. It is composed of 11 bits having a bit pattern which is unique in the data stream:
00000000001

The header is followed by the **Identification code** which is composed of 64 bits organized in 8 blocks of 8 bits. Each block of 8 bits is trailed by a control bit set to logic "1" to prevent that the header is reproduced in the data. The 64 bits of Identification code are organized in following way:

- Bit 64 is transmitted first.
- Bit 1 is a flag for animal "1" or non-animal "0" application.
- Bits 2-15 are a reserved code for future use.
- Bit 16 is a flag for additional data block "1" or no additional
- data block "0".
- Bits 17-26 ISO 3166 Numeric country code
- Bits 27-64 National identification code

The next two 8 bit blocks contain the **16 CRC-CCITT** error detection bits. LSB is transmitted first, and the 2 block are trailed with a binary "1".

Last 3 blocks of 8 bits trailed with a logical "1" represent the extension bits. The extension bits are planned for future extension in which for instance information from sensors or contents of trailing pages may be stored. In the current version the standard coding is **000000001 000000001 000000001** and the flag bit 16 of the identification code is set to"0".

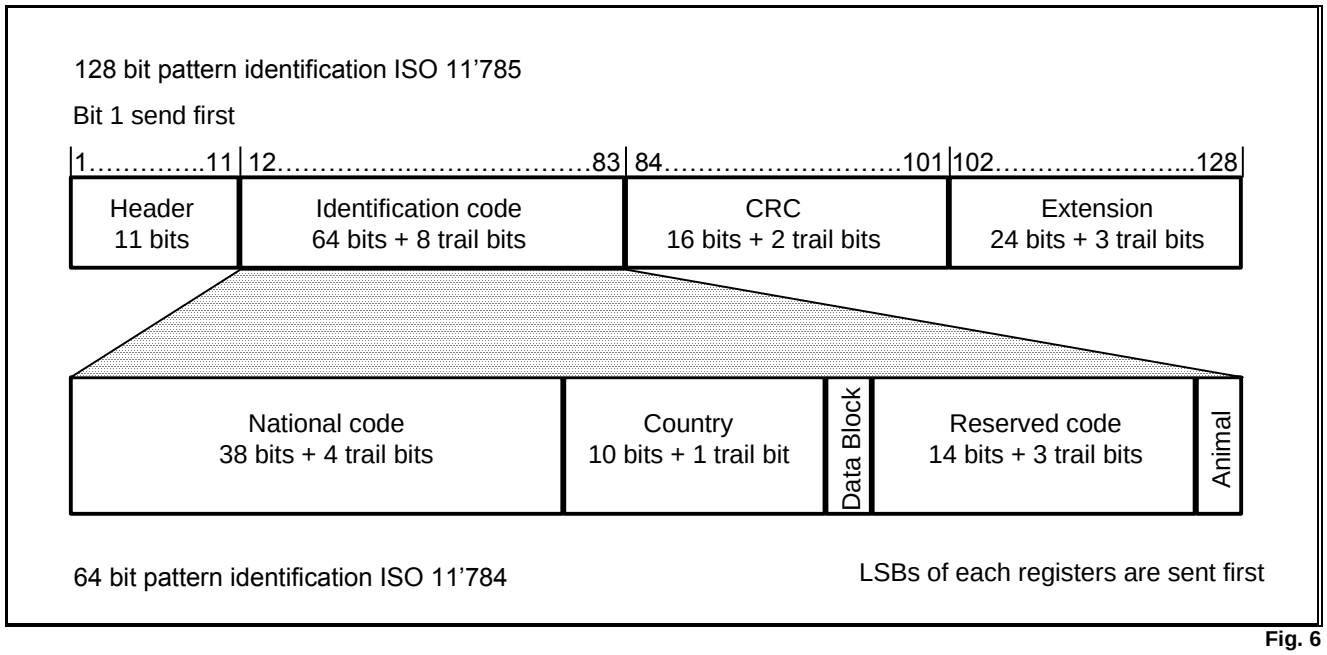


Fig. 6

Manchester 64 (EM4100 compatible)

For this version data rate is set to 64 RF clocks per bit, data encoding is Manchester, 64 bit of ROM are used.

64 bits of ROM are divided in five groups of information. 9 bits are used for the header, 10 row parity bits (P0-P9), 4 column parity bits (PC0-PC3), 40 data bits (D00-D93), and 1 stop bit set to logic 0.

1	1	1	1	1	1	1	1	1	9 header bits
8 version bits or customer ID				D00	D01	D02	D03	P0	
				D10	D11	D12	D13	P1	
				D20	D21	D22	D23	P2	
32 data bits				D30	D31	D32	D33	P3	
				D40	D41	D42	D43	P4	
				D50	D51	D52	D53	P5	
				D60	D61	D62	D63	P6	
				D70	D71	D72	D73	P7	
				D80	D81	D82	D83	P8	
				D90	D91	D92	D93	P9	10 line parity Bits
				PC0	PC1	PC2	PC3	S0	
				4 column parity bits					

Table 6

The header is composed of the 9 first bits which are all mask programmed to "1". Due to the data and parity organisation, this sequence cannot be reproduced in the data string. The header is followed by 10 groups of 4 data bits allowing 100 billion combinations and 1 even row parity bit. Then, the last group consists of 4 event column parity bits without row parity bit. S0 is a stop bit which is written to "0"
Bits D00 to D03 and bits D10 to D13 are customer specific identification.

PSK 64 (EM4100 compatible)

For this version data rate and encoding are set to PSK, 64 bits of ROM are used, double pulse lockout feature is enabled. 64 bits of ROM are organised according to customer definition.

EM4200 Pad Location

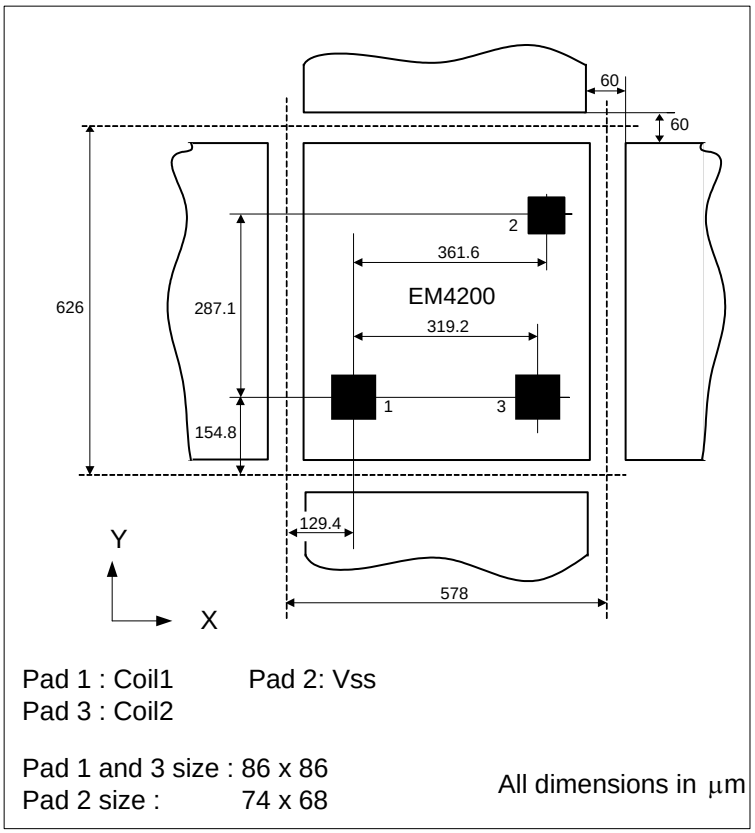


Fig. 7

Packaging information

2 leads Plastic Package: EMDFN-02

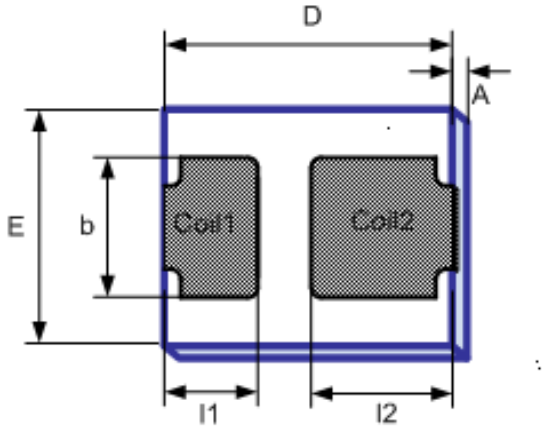


Fig. 8

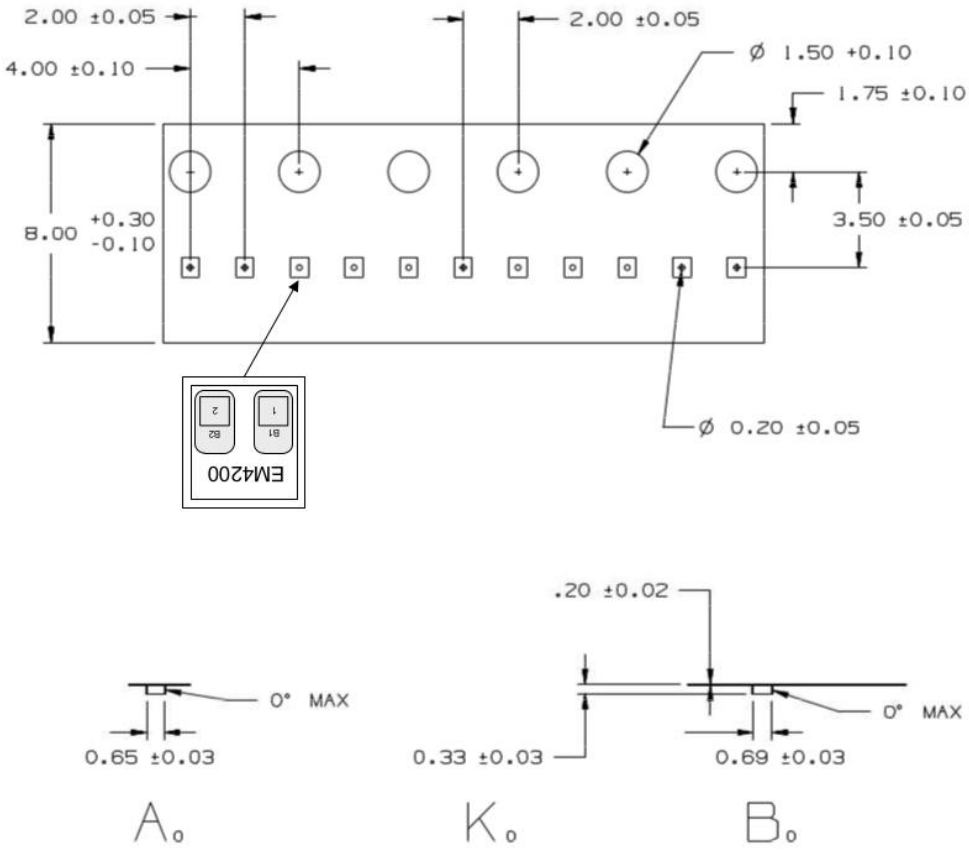
Package mechanical dimensions:

	A	D	E	B	l1	l2
Size	0.76	2.20	1.78	1.07	0.71	1.08
Tolerance	0.10	0. 15	0.15	0.05	0.05	0.05

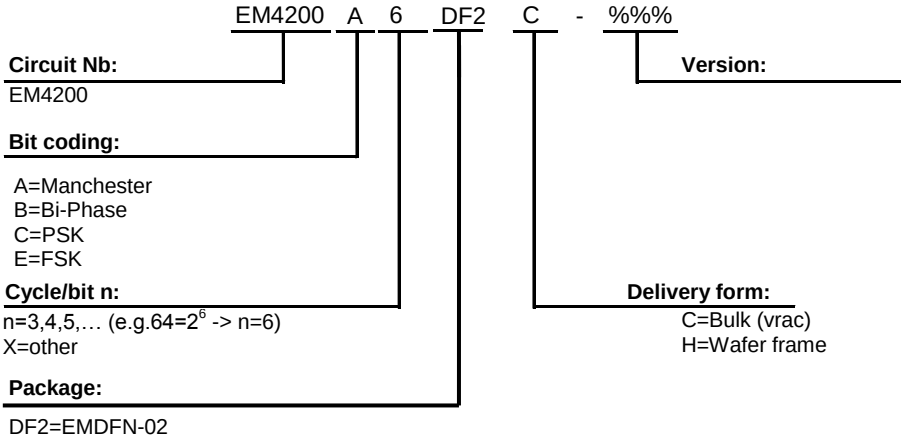
Table 7

Note: all dimensions in mm.

Blister tape: Die positioning in Microtape



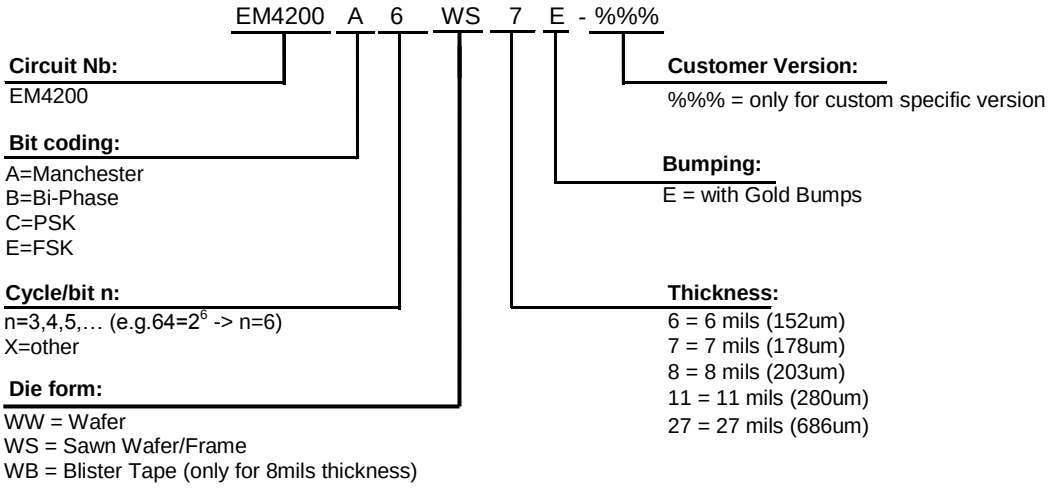
Ordering Information – Package IC



Part Number	IC Data Encoding	Data Length	IC Cres	Delivery Form
EM4200A6DF2C-001+	Manchester – 64RF	64 bits	250pF	Loose form
EM4200B5DF2C-006+	Biphase – 32RF	128 bits	250pF	Loose form

Table 8

Ordering Information – Die form



Remarks:
For a sawn or un-sawn wafer delivery, the good dies are recognized using an electronic wafer map given by EM. No ink dots are applied to the wafer.
For other delivery forms or packages, please contact EM Microelectronic-Marin S.A.

Standard Versions & Samples:
The versions below are considered standards and should be readily available. For other versions or other delivery form, please contact EM Microelectronic-Marin S.A.

Part Number	IC Data Encoding	Data Length	IC Cres	Package	Delivery Form
EM4200A6WS7-001	Manchester – 64RF	64 bits	250pF	Sawn wafer	Wafer on frame
EM4200A6WB8E-051	Manchester – 64RF	64 bits	250pF	Bumped die	Blister Tape
EM4200B5WS7-006	Biphase – 32RF	128 bits	250pF	Sawn wafer	Wafer on frame
EM4200XXYYY-%%%	Custom	Custom	Custom	Custom	Custom

Table 9